

30-Day Design Cycle With XC8100 FPGA Family

Design engineers at SIXNET (Clifton Park, NY), a manufacturer of industrial control equipment, faced a daunting challenge: to build a new I/O module (from concept to installation at a customer's site) within eight weeks.

The device, a digital counter board, was required to provide position and/or velocity information for eight independent incoming signals. The digital count signals can be used singly to provide total count or velocity information, or in pairs to provide quadrature-decoded position information. Typical applications are flow metering (where a small turbine pulses at a rate proportional to the flow of a liquid) and position measurement (where a quadrature decoder tracks the motion of precision machinery).

All previous designs at SIXNET had employed 22V10 (or smaller) PLDs, using equation-based design entry as the primary development tool. While time restrictions dictated the use of programmable logic, severe space limitations drove the need for a more highly-integrated, single-chip solution. The SIXNET design team quickly narrowed its choices to a competitor's SRAM-based FPGA or the Xilinx XC8100 FPGA family.

The main elements of the design include registers to capture and synchronize incoming data, state machines for quadrature decoding, and eight 16-bit counters and latches used for position and velocity measurement. The outputs of the counters and state machines are multiplexed and output on an 8-bit bus. The clock frequency is a modest 4 MHz.

SIXNET engineers quickly discovered that it would be difficult to fit the design using the relatively large logic blocks of the SRAM-based FPGA. The counter logic is register-intensive, requiring very little logic between flip-flops, resulting in substantial "wasted" logic in each logic block. Similarly, the wide multiplexers were not a "good fit," requiring the use of many blocks, but with relatively low utilization of the logic in each block. (These problems

would have been even more prevalent in the combinatorial-intensive architecture of a CPLD device.)

The same design was easily implemented in a less-expensive XC8103 FPGA. In the XC8100 FPGA architecture, each fine-grained logic cell can implement either combinatorial or sequential logic, allowing high utilization regardless of the unequal mix of combinatorial functions and flip-flops. The counters were implemented as ripple counters, both to minimize area and avoid switching noise; the flexible clocking structure of the XC8100 architecture enabled this approach. An internal quad latch with output enable — a primitive in the XC8100 library — was used to latch and multiplex the eight counters onto a common bus, eliminating the multiplexing logic needed with the competitor's product.

The design was entered and implemented on a PC using a Viewlogic schematic editor and the Xilinx XACTstep™ Series 8000 development system, respectively. "The transition from equation entry to Viewlogic schematics was easy," claims Dave Ellis, vice president of Engineering at SIXNET. "It was just like doing the schematic for a printed circuit board. The XC8100 tools were very easy and intuitive to use. We were able to complete the design phase from concept to a working board in less than four weeks, including learning the Viewlogic and XC8100 design tools." The controller fits on a compact 3.3"x4.3" circuit board.

In conclusion, Mr. Ellis noted, "The Xilinx XC8103 was by far the most cost-effective solution for our needs." ♦

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