

INSTALL

44

Q Can I use XACTstep v6 with Windows 95?

Windows 95 is not officially supported by the XACTstep v6 release, but many users have been successfully working with this combination. You will, however, run into this problem: when exiting the Design Manager, the error message "This program has performed an illegal operation and will be shut down." will appear. Simply choose Close; this message is benign.

The Viewlogic PROseries tools are not supported in Windows 95. Windows NT is not supported by XACTstep or PROseries.

Q How can I find out more information about my Windows Configuration?

There are two Windows utilities on the XACTstep CD-ROM (the following instructions assume that C:\ is the hard drive and D:\ is the CD drive). Choose File➤Run from the Program Manager and select D:\XBBS\UTILS\XINFO\XINFO.EXE to run XINFO. XINFO will analyze the current configuration of your PC, and report DOS and Windows environment settings, amount of memory available, and a list of hints and recommendations. The other program, XMEM, is run by selecting D:\XBBS\UTILS\XMEM\XMEM.EXE from File➤Run. This dynamic program will keep you updated with the status of RAM, memory below 1 Meg, and USER and GDI percentages. These tools are designed to help you debug memory or configuration issues you may come across.

Q I followed the instructions from the article "Executing from the XACTstep CD-ROM" from the last issue of XCELL (#19, 4Q95) but I still get errors. What am I doing wrong?

The article assumed that the XACTstep SETUP program had been previously run. In other words, it assumed that some Windows environment settings had already been configured. Here's what you'll need to do:

1. Install the correct version of Win32s, which is 1.25.142.0. You can verify this by looking at the file: C:\WINDOWS\SYSTEM\WIN32S.INI or by checking XMEM or XINFO. If you do not have this version, exit Windows and run the batch file from the XACTstep CD-ROM: D:\XBBS\UTILS\RMWIN32S.BAT. Then re-enter Windows and choose File ➤Run and select D:\WIN32S\DISK1\SETUP.EXE to install the proper version of Win32s.
2. Install the necessary Windows drivers. If you are only using the XACTstep tools, do the following:


```
copy D:\XACT\WINDOWS\SYSTEM\*. * C:\WINDOWS\SYSTEM
mkdir C:\WINDOWS\ASYM
mkdir C:\WINDOWS\ASYM\RUNTIME
copy D:\XACT\WINDOWS\ASYM\RUNTIME\*. *
C:\WINDOWS\ASYM\RUNTIME
```

If you are using the PROseries tools, you will also need to do the following:

```
copy D:\PROSER\WINDOWS\*. * C:\WINDOWS
copy D:\PROSER\WINDOWS\SYSTEM\*. * C:\WINDOWS\SYSTEM
```
3. Install the DAIKON.386 device driver. You have already copied this driver in Step 2, but now you need to edit the C:\WINDOWS\SYSTEM.INI file. Open this file and add the line:


```
DEVICE=DAIKON.386
```

after the [386Enh] header. After you quit and re-enter Windows, you'll be all set.

Design
Manager/Flow
Engine**Q When using Viewlogic schematics, what can I do to avoid problems in the translation phase of the Design Manager?**

There are several problems that can stop the design from translating. The .WIR files must be present for the translation process to complete. If they are missing, the design can be brought up to date by running check -p <design> from a DOS prompt or selecting Tools ➤check ➤project from PROcapture. The parttype must be specified either in the design or in the Translate Options dialog box; WIR2XNF requires a parttype to be specified. The path to the design must not contain a period, other than in the name of the design file.

Continued on the next page

Design Manager/Flow Engine (con't)

Q How do I change options that aren't listed in the Options dialogs?

Select **Utilities** ➔ **Template Manager** from the Design Manager's menu. Select the desired template and click on the Customize... button. In the Custom Template Dialog, type in the program name and the desired option. For example, to force XNFPREP to ignore xnf locations in the interior of the chip, the following line would be used:

```
xnfprep ignore_xnf_locs=true
```

When any custom options are used, an asterisk will appear next to that template.

Q I am running the Flow Engine from the Design Manager and it hangs. My PC is still working (I can move my mouse), but the Flow Engine seems to have stopped. What has happened?

The problem is that the DOS process underneath the Windows application has become disconnected. The Flow Engine is still running in Windows, but there is nothing running in DOS to tell it when it is done. Try the following suggestions one at a time:

1. Disable 32-bit File Access and reduce the cache size by using the Control Panel ➔ 386Enhanced ➔ Virtual Memory ➔ Change. (Windows 3.1.1 only)
2. Disable SmartDrive write caching by using the /X option.
3. Disable 32-bit Disk Access, also found in the Virtual Memory settings.

If these changes do not fix the problem, call the Technical Support Hotline at 800-255-7778.

Q Selecting Design ➔ Implement seems to give one Flow Engine while the Tools ➔ Flow Engine gives a different one. What's the difference?

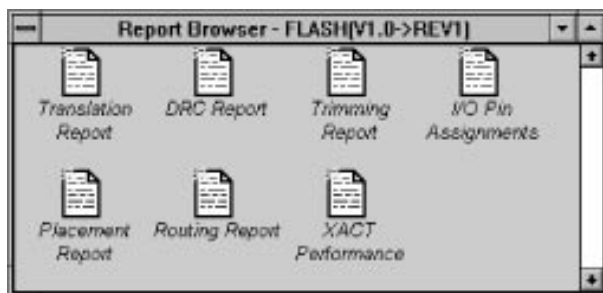
The one under Design ➔ Implement is an automatic version of the Tools ➔ Flow Engine. Use the first to perform automatic runs; use the latter to set advanced options or stop the flow at a certain point.

Q The Flow Engine appeared to hang in bitstream phase. How do I get it to finish?

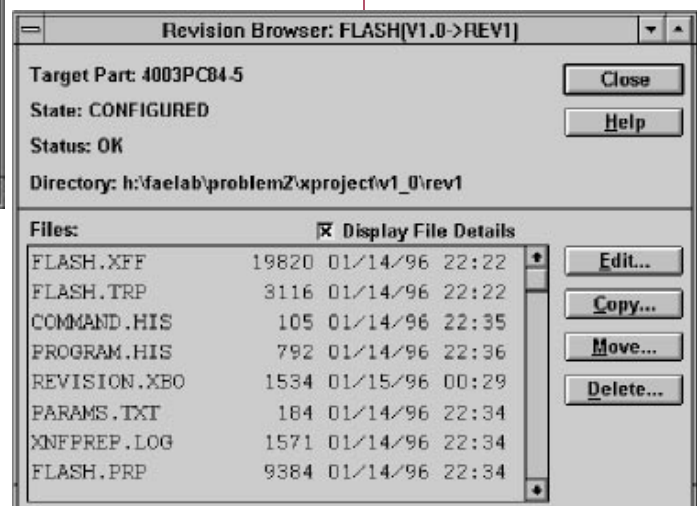
This is a problem we have traced to 32-bit file access in Windows for Workgroups v3.1.1. In the Windows control panel under Enhanced ➔ Virtual Memory... ➔ Change>>there is a "Use 32 Bit File Access" checkbox. Turn this off, restart Windows, and the Flow Engine should complete successfully.

Q What's the difference between the report browser and browse revision?

The report browser is a graphic interface that allows access to the most commonly needed report files, such as I/O pin locations, trimming report, etc. Design ➔ Browse Revision allows access to all the files in a selected revision through a listing of the files. (See figures.)



Report Browser



Revision Browser

Technical Questions and Answers
continued on the next page

Mentor Graphics

NOTE: A more elegant solution was in development at press time. For further information, send an e-mail to xdocs@xilinx.com with “send 692” as the subject line.

Q I have several external signals connected to PAD symbols that I merge into or bus-rip out of a single bus connected to a bussed I/O buffer symbol (e.g., IBUF8, OBUF8, etc.). I have done this so that I can place LOC properties on the individual PAD symbols (since they cannot be placed on IPAD8s, OPAD8s, etc.). However, when I compile the design, I discover that the LOC constraints have not been followed, and no warning has been issued by any programs. In fact, these LOC properties do not exist in any of the XNF files output by Men2XNF8! What’s happening?

The Mentor translation process involves two programs, ENWrite and EDIF2XNF. ENWrite (a Mentor program) generates an EDIF netlist which EDIF2XNF translates to a set of XNF files. When signals are bussed in a Mentor schematic, ENWrite creates a construct called a “net bundle” in the EDIF file. Although all the information about the associated LOC properties is included as part of the net bundle, EDIF2XNF expects to see a separate, independent construct for each of these nets when it looks for associated properties. Therefore, when EDIF2XNF translates these net bundles from the EDIF file, it leaves off the pin-location constraints that were placed on the input and output signals. This problem is solved by simply bus-ripping the signal path internally (i.e., after the IBUFs or before the OBUFs).

Q Some LOC properties on the pads in my design are not passed to subsequent stages in the design compilation. I’ve noticed that these LOC properties are displayed as purple text in Design Architect, instead of the normal gold color. What does this mean?

A purple property in Design Architect means that the property is attached to the *pin* on the PAD symbol, whereas a gold property means that it is attached to the *net* attached to the pin. Because the PAD symbols in the Mentor libraries are defined as ports, any properties attached to these symbols (i.e., shown in purple) will not be passed to the EDIF file during Men2XNF8, and thus will not be passed to subsequent stages of the compilation.

Usually, LOC properties on Xilinx PAD symbols will transfer to the attached net and will therefore appear gold; however, sometimes the property gets stuck on the PAD pin. The workaround is to select the *net vertex* connected to the offending pin, then add the LOC property to the net vertex. This new property should show up in gold, and thus will be passed to the compilation tools. In any case, beware of purple LOC properties!

Q When running the Check function in Design Architect, I get these warnings:

```
Warning: Unable to evaluate property "model" on I$30
Unable to resolve expression symbol lca_technology
Warning: Unable to evaluate property "__qp_prim" on I$30
Bad Triplet CASE Control Expression
Unable to resolve expression symbol lca_technology
```

What do these warnings mean and how can I fix them?

All Xilinx simulation models in Mentor have a variable associated with them called “lca_technology.” Normally, this parameter is set whenever a library component is instantiated, but a number of situations can cause Design Architect to lose this parameter. If this happens, Check will not be able to evaluate any properties that use this parameter; however, the lca_technology parameter does not need to be set until the design is simulated or translated to an XNF netlist, at which point the lca_technology parameter is filled in appropriately. Therefore, these warnings can be safely ignored.

You can recover the value of lca_technology and unclutter the Check report of these warnings by selecting Check → Parameters → Set. In the dialog box, enter **lca_technology** as the parameter name, and set the value to the appropriate device family (e.g., **xc3000** or **xc4000**). After doing this, re-execute Check Sheet.

Synopsys

Q Can Input and Output flip-flops be inferred in XC4000E designs?

Synopsys can infer input and output flip flops in an XC4000E design. However, if a flip flop has its clock enable (or reset pin) connected, then Synopsys cannot infer it as an IOB flip-flop, and it will be implemented as an XC4000E CLB flip-flop. For a flip-flop to be inferred as an IOB flip flop by Synopsys, its clock enable (and reset pin) must not be connected to anything. You must, therefore, instantiate IOB flip-flops that have their clock enable pin connected.

Q Can Synopsys infer an input flip-flop with the “NODELAY” attribute?

The Synopsys (XSI) For FPGAs manual states on page B-9 and B-10 that input latches and flip flops with the NODELAY attribute may be inferred. This is not true. All Input flip flops and input latches with a NODELAY attribute must be instantiated.

Input Flip-Flops:

For the XC4000/A/H/D family, the “fast” input flip-flops are IFD_F and IFDI_F

For the XC4000E family, the “fast” input flip-flops are IFDX_F, IFDXI_F, and IFDXI_U

Input Latches:

For the XC4000/A/H/D family, the “fast” input latches are ILD_1F and ILDI_1F

For the XC4000E family, the “fast” input latches are ILDX_1F and ILDXI_1F

Q Do I require any additional settings for XC3000 or XC5200 designs in Synopsys?

There is one additional setting that you should include into your .synopsys_dc.setup file, if you are using the FPGA Compiler to synthesize XC3000 or XC5200 designs. Include the following line in your .synopsys_dc.setup file:

```
fpga_improved_delay_mapping = 1 ♦
```

Technical Support Resources

In addition to field application engineers (FAEs) and technical support engineers (TSEs) located all over the world to provide direct support, Xilinx has several automated services to provide answers to your queries: an e-mail server, an automated FAX system, a bulletin board system, and special interest e-mail groups.

The **XDOCS** e-mail system provides 24-hour-a-day, 7-day-a-week access to the same database that the TSEs use. It is updated daily with bugs, workarounds, and helpful hints. Via e-mail, users can search for a specific record, or use keywords to trigger a search of the database; XDOCS will send the requested information by return e-mail. Users can receive periodic updates regarding new additions to the system.

To subscribe to XDOCS, send an e-mail to xdocs@xilinx.com with “help” as the only word in the subject header.

The **XFACTS** automated FAX system (408-879-4400) provides the same information as XDOCS, but uses a phone/FAX interface instead of e-mail. Using a touch-tone telephone, users can request documents that are sent to their FAX machine.

The **technical support group** also has an e-mail alias: hotline@xilinx.com, and a bulletin board that is updated with utilities such as new package files as they become available.

Due to the growth in interest in specific application areas, Xilinx has established a set of e-mail addresses to provide support for questions related to these topics (*see margin at right*).

If you have any questions or comments regarding these systems, or if there are other support methods that you would like to see implemented, give us a call or send a FAX; the numbers are given in the margin at right. ♦

Synopsys (con’t)

HOTLINE SUPPORT

United States

Customer Support Hotline:

800-255-7778

Hrs: 8:00 a.m.-5:00 p.m. Pacific

Customer Support Fax Number:

408-879-4442

Avail: 24 hrs/day-7 days/week

E-mail Address:

hotline@xilinx.com

Electronic Tech. Bulletin Board:

408-559-9327

Avail: 24 hrs/day-7 days/week

Customer Service*:

408-559-7778

ask for customer service

**Call for software updates, authorization codes, documentation updates, etc.*

Europe

UK, London Office

telephone: (44) 1932 349402

fax: (44) 1932 333530

BBS: (44) 1932 333540

e-mail: ukhelp@xilinx.com

France, Paris Office

telephone: (33) 1 3463 0100

fax: (33) 1 3463 0109

e-mail: frhelp@xilinx.com

Germany, Munich Office

telephone: (49) 89 99 15 49 30

fax: (49) 89 904 4748

e-mail: dlhelp@xilinx.com

AUTOMATED SUPPORT

Xilinx World Wide Web Site

<http://www.xilinx.com>.

XDOCS e-mail document server

for instructions, send an e-mail to xdocs@xilinx.com with “help” as only item in the subject header.

XFACTS fax document server-

Call 1-408-879-4400.

Specific Question E-mail:

Digital Signal Processing dsp@xilinx.com
PCI-bus pci@xilinx.com
Plug and Play ISA PnP@xilinx.com
PCMCIA card pcmcia@xilinx.com
Async. Transfer Mode atm@xilinx.com
Reconfig. Computing .. reconfig@xilinx.com