

JTAG Support in the XC9500 CPLD Family

The new XC9500 family of CPLDs can mitigate the effects of rapidly rising testing costs for loaded PC boards by simplifying the manufacturing process. Caused by the increasing complexity of IC's and the use of packaging technologies that restrict access to interconnections, along with the handling requirements of most complex programmable logic devices, increased testing costs have been a significant challenge to manufacturers.

The XC9500 family allows you to automatically program and test multiple devices and PC boards in-system, using the industry standard JTAG interface. This greatly simplifies the production, test, and maintenance of complex systems. With this capability you can even make engineering changes to CPLDs on your production boards in the field, and those changes can be fully verified.

The XC9500 CPLD family simplifies testing because you can use software to verify the functionality of devices and their

interconnections; complex and expensive PC board test/probing systems are no longer required. Device handling problems are also minimized since XC9500 devices are programmed in-system, alleviating the lead integrity problems associated with external programming methods. The XC9500 family includes seven devices that range from 800 to 6,400 equivalent gates, with pin-to-pin delays as fast as 5 ns.

JTAG Overview

JTAG, also known as IEEE Standard 1149.1, uses a simple 4-wire interface known as the Test Access Port (TAP) to access a boundary scan serial shift register and control logic embedded within a device. Each XC9500 I/O pin is connected to one stage of the boundary scan shift register, allowing the pin to be stimulated and sampled. Output sampling can even occur during normal device operation. By shifting in a test stimulus and instructions,

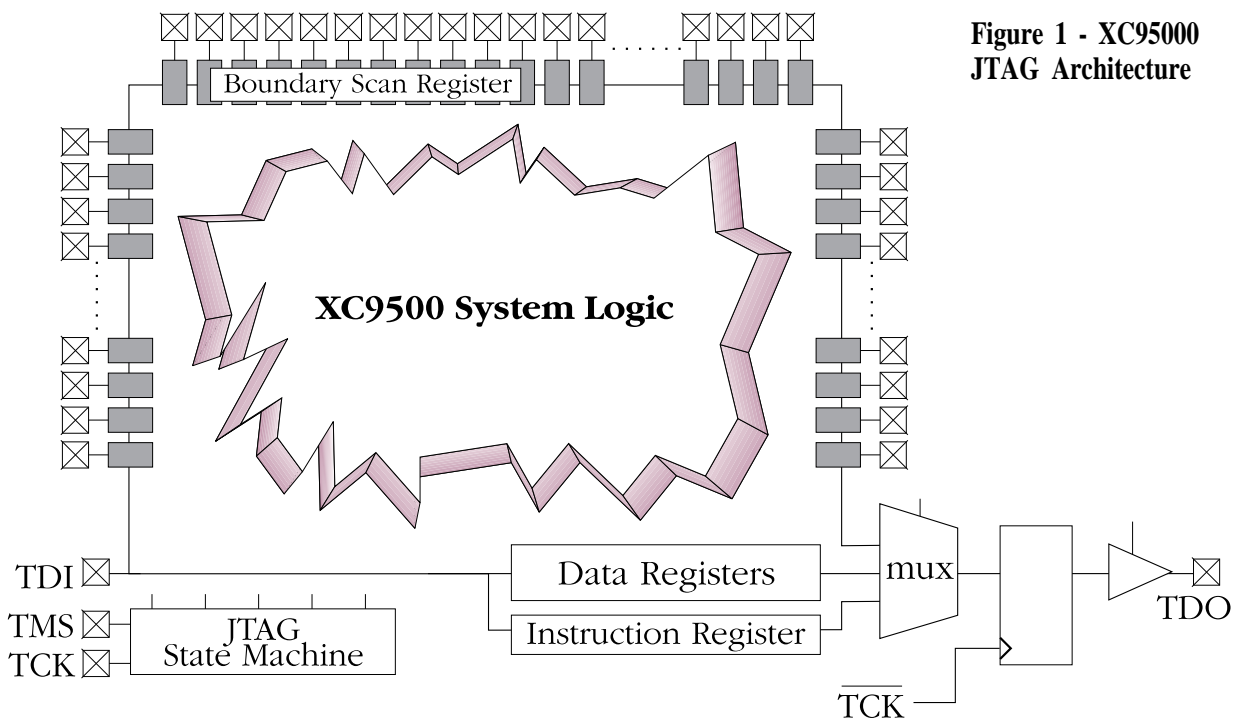
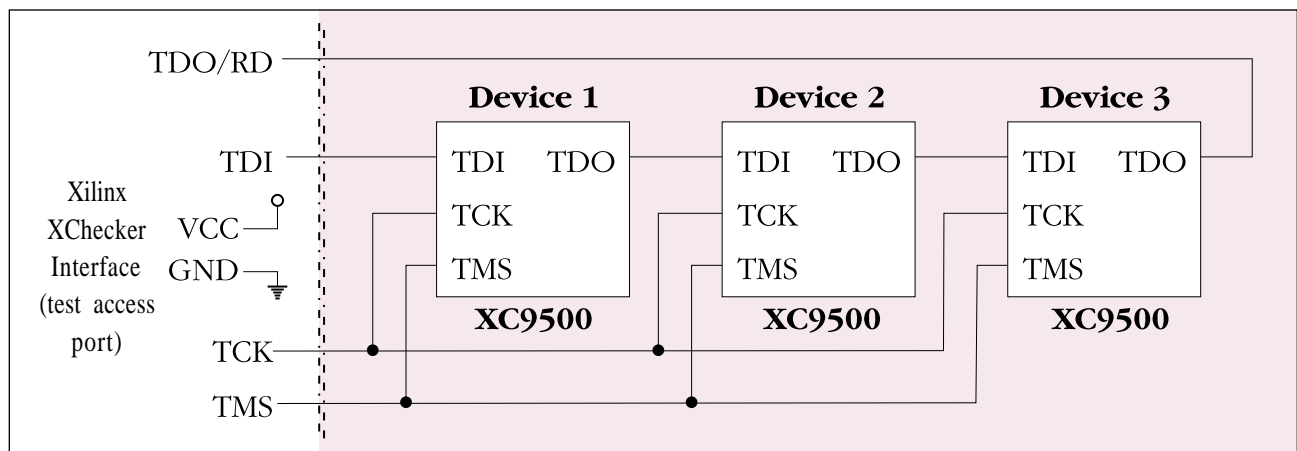


Figure 1 - XC9500 JTAG Architecture



and then shifting out the result, you can effectively and automatically test devices and their interconnections on a PC board.

Figure 1 shows the XC9500 JTAG architecture. JTAG allows multiple devices to be daisy-chained and accessed via the TAP. This simplifies board layout, minimizes hardware overhead and reduces test software requirements. **Figure 2** illustrates a typical daisy-chain arrangement.

Xilinx has extended the TAP to include in-system programming capabilities. Just four dedicated pins are needed for both programming and testing any number of devices.

JTAG Operations

The XC9500 devices support standard and optional JTAG operations, including:

- **SAMPLE/PRELOAD** - Allows output sampling and input stimulus preloading while the device is fully operational.
- **EXTEST** - Allows testing of device interconnections, independent of internal device operations.
- **BYPASS** - Bypasses a device by effectively connecting TDI to TDO.
- **IDCODE** - Used to identify the system, to verify that a system is “alive,” and to select specific test sequences. It can be used for system debug, manufacturing test, field diagnostics, and upgrades.
- **USERCODE** - Used to identify the contents and version of a system. This is essential for on-line diagnostics, field upgrades and the specification of test sequences or programs to be used

during manufacturing. Also used during prototyping and manufacturing for version control.

- **INTEST** - Facilitates functional verification, independent of system interconnections. This is essential for prototyping and for low-cost manufacturing test because it can immediately identify functional errors in your design.
- **HIGHZ** - Facilitates interconnect test in systems with busses. It allows unique enabling and disabling of drivers on bussed lines and can also be used to isolate and diagnose interconnect failures.

These operations are fully-compatible with the IEEE 1149.1 JTAG standard and all third party JTAG test systems.

Xilinx provides everything you need for developing, programming and automatically testing XC9500 devices. This support is available for SUN, HP 9000 and IBM-compatible PC platforms.

In summary, the XC9500 CPLD family is the first to feature full in-system programming and test capabilities. This family of high-speed, high-density devices will help you produce complex designs more efficiently, and those designs will be easier to program and verify. Circuit board manufacturing and maintenance costs are reduced since production designs can be modified and tested without retooling or using expensive board testers. ♦

Figure 2 - Daisy Chain Operation