

New XC7000 Core Software in XACTstep v6

The Xilinx XC7000 core software delivered in XACTstep v6 contains new features and enhancements of existing features that address user productivity and design performance for Xilinx CPLD designs.

Productivity Improvements

Automatic Device Selection - The software automatically implements the design in the smallest device possible using device type, package type and speed constraints entered by the designer

XACT-Performance™ - Timing-driven optimization collapses logic to meet user-specified critical timing requirements.

Static Timing Analyzer - Provides a complete pin-to-pin timing report of the design, including detailed internal path analysis

Performance Improvements

New Design Optimization Algorithms - New design optimization and partitioning algorithms better utilize the XC7300 architecture *without user intervention*. Designs fit in smaller devices, take about 10% fewer macrocells and run about 10% faster than before.

Multiple-Pass Optimization, Partitioning and Mapping - The software will try a different optimization and partitioning strategy if necessary to achieve a first-time fit, *without user intervention*.

Schematic and VHDL Design Entry

Xilinx provides an open design environment that allows designers to choose from a variety of schematic entry, VHDL synthesizer and simulation tools, such as those from OrCAD, Viewlogic, Men-

tor Graphics, Exemplar and Synopsys. When combined with the appropriate library and interface software, XACTstep v6 provides a complete environment for the processing of Xilinx XC7000 CPLD designs

ABEL-HDL Entry

XABEL owners can continue to embed macros in their schematics or enter complete chip designs for the XC7000 family and use XACTstep v6 to complete the design implementation. This core software is included in the new Xilinx XABEL-CPLD package, a complete ABEL-HDL based tool designed specifically for PAL users who want to use Xilinx XC7000 CPLDs.

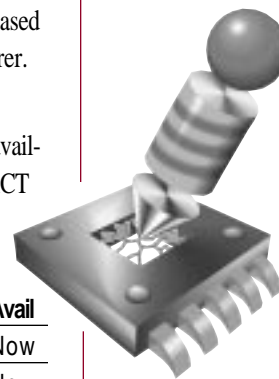
Embedded Third Party Compilers

Xilinx licenses its fitter technology to third-party development tool vendors, giving you the flexibility and versatility of industry-standard design software environments with the speed, density and routability of Xilinx CPLDs. The Xilinx CPLD fitter is fully integrated into the Data-I/O Synario, Logical Devices CUPL and IsDATA LOGiC environments. For price and availability of the XACTstep v6 based fitter, contact the development tool manufacturer.

Product Availability and Pricing

The XC7000 XACTstep v6 core software is available on the PC for immediate delivery. The XACT 5.2 core software is available for workstation platforms. ♦

Part Number	Version	Platform	Pricing	Avail
DS-550-PC1-C	6.0	PC	\$89.95	Now
DS-550-SN2-C	5.2	Sun	\$995	Now
DS-550-HP7-C	5.2	HP	\$995	Now



The table summarizes the supported CAE interfaces. Many other third-party CAE vendors are working on XC8100 solutions that will be released in the first half of 1996.

Now Runs on PC — Version 1.1 adds PC support (DS-8000-STD-PC1-C or DS-8000-EXT-PC1-C). It

runs under Windows 3.1, Windows 95 and Windows NT. The CAE interfaces available on the PC include Viewlogic and Exemplar. Workstation versions are available for SunOS, Solaris, HPPA, and RS6000 platforms. ♦

CAE Tools Supporting XC8100 FPGA Design

Schematic	Synthesis	Simulation	Timing Analysis
Viewlogic ProCapture Mentor Design Architect	Synopsys Design Compiler Synopsys FPGA Compiler Viewlogic ViewSynthesis Mentor Autologic I, II Exemplar	Synopsys VSS Cadence Verilog Viewlogic ViewSim Mentor QuickSim Mentor QuickVHDL Model Tech VITAL VHDL	Synopsys Motive Mentor QuickPath Cadence Veritime