

# Introducing the XC4000EX FPGA Family

## Xilinx Builds on the XC4000 Series to Extend FPGAs up to a Quarter of a Million Gates.

The XC4000 series, including the original XC4000, the XC4000E and now the XC4000EX family, is the ideal solution for high-density, high-performance FPGA needs. First introduced in 1991, the XC4000 series has become the world's most-popular FPGA family; in fact, if it were a free-standing entity, the XC4000 series would be the third largest program-mable logic company in the world.

The new XC4000EX family extends the density and performance leadership of the XC4000 series to new levels. With devices up to 125,000 usable gates, the XC4000 series density range will overlap with the majority of gate array design starts. In addition to increased density, the XC4000EX family features architectural improvements that increase design ease, utilization and performance.

### The XC4000EX family

The XC4000EX family will include seven members ranging from 28,000 to 125,000 logic gates. In a typical system application using on-chip memory, the maximum density rises to 250,000 gates (*see table 1*). These devices are available in a variety of packages that are footprint compatible with the other members of the XC4000EX and XC4000E families. The XC4028EX is available now. The XC4036EX will be available in the first half of this year, with the XC4044EX, XC4052EX and XC4062EX following in the second half. The two largest devices, the XC4085 and XC40125, will be offered in 1997.



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Table 1 - The XC4000EX family

	4028EX	4036EX	4044EX	4052EX	4062EX	4085EX	40125EX
Typical Logic Gates	28,000	36,000	44,000	52,000	62,000	85,000	125,000
Typical System Gates* (Logic + Select-RAM)	56K	72K	90K	110K	130K	175K	250K
Available RAM bits	32,768	41,472	51,200	61,952	73,728	100,352	157,968
CLB Array	32x32	36x36	40x40	44x44	48x48	56x56	68x68
CLBs	1,024	1,296	1,600	1,936	2,304	3,136	4,624
Flip-Flops	2,560	3,168	3,840	4,576	5,376	7,168	10,336
I/O	256	288	320	352	384	448	544
Packages:	HQ208 HQ240 PG299 HQ304 BG352	HQ304	BG432 PG411	BG432 PG411 BG596	PG499 BG596	PG499 BG596	BG596
*30% of CLBs as RAM							

100% Footprint  
Compatible

# XC4000EX

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The XC4000E family is manufactured on a 0.6 micron (drawn) triple layer metal (TLM) process. The XC4000EX FPGAs are based on an advanced 0.5 $\mu$  (drawn) TLM process. This new process enables both increased density and increased performance. The two primary determinants of silicon speed are feature size and interconnect delay. The 0.5 $\mu$  gate length speeds transistor performance, while the silicon size decrease resulting from the smaller geometry dramatically reduces the size of the die, which, in turn, reduces interconnection delays.

The 0.5 $\mu$  technology used for the XC4000EX devices will be replaced by a more advanced 0.35 $\mu$  quad layer metal technology, planned for early 1997. This new technology will allow the manufacture of the two largest members of the XC4000EX family — the XC4085EX and XC40125EX. In addition, all family members will be redesigned in 1997 to leverage the 0.35 $\mu$  technology, resulting in cost reductions and speed improvements.

## Additional Routing Resources

Programmable logic is successful because it allows designers to achieve a faster time-to-volume than conventional approaches. For high density FPGA designs, device routability is a key factor; better

routability enables faster design compilation times and boosts silicon utilization. As device densities increase, both the number of interconnections and the average length of interconnections increase. In order to effectively route designs of more than 100,000 gates, breakthroughs in interconnect topology were necessary.

The XC4000EX family features an enhanced interconnect scheme. As shown in **Figure 1**, the number of interconnect resources has increased substantially compared to the XC4000E and XC4000 architectures. Twelve “quad lines” are added both horizontally and vertically. The quad lines are interconnected by a buffered switch matrix that is spaced every four CLBs. Each buffered switch matrix contains both buffers and pass transistors. The place and route software will use the timing requirements of the design to determine whether it is optimal to use a buffer or pass transistor for each interconnect switch. Because of the buffered switch matrices, quad lines provide the fastest means for routing heavily loaded signals over long distances.

In addition to the quad lines, the number of vertical long lines has increased from six to 10. Buffered programmable splitters are added to these long lines at positions 1/4, 1/2 and 3/4 of the way across the chip. Due to the buffering, XC4000EX long line performance does not deteriorate with larger array sizes. If a long line is split, the resulting partial long lines are independent. The number of global lines also was doubled from four to eight, as described below.

The XC4000EX architecture also offers direct connects that allow efficient and fast connections between adjacent CLBs. These nets allow high-speed data flow from CLB to CLB. Signals routed on the direct connects exhibit minimum interconnect propagation delay and use no general routing resources. Direct connects are ideal for creating sophisticated, high-speed macros.

The XC4000EX devices have additional VersaRing™ routing around the perimeter

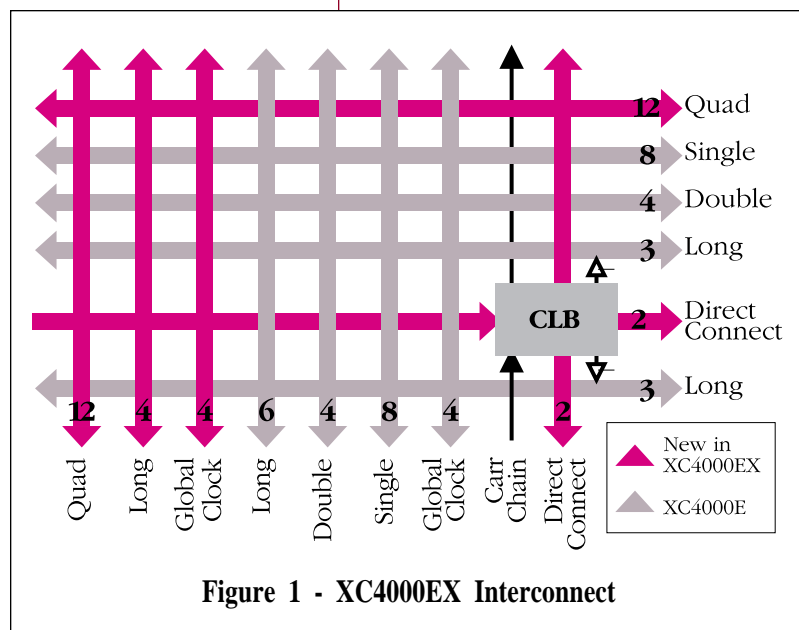


Figure 1 - XC4000EX Interconnect

of the CLB array. The VersaRing feature, first introduced with the XC5000 series, facilitates pin-swapping and redesign without affecting board layout. It avoids the trade-off of high utilization versus pin assignment flexibility by allowing both.

## Global Nets and Buffers

Global nets and buffers are the primary mechanism for distributing clocks and other high fanout control signals throughout a device. The buffers accept signals that are generated on-chip or externally and drive them onto the global nets. The XC4000EX device has three types of global buffers.

- **Global Low-Skew Buffers** - similar to those found on the XC4000, XC4000E and many other devices. The buffers are designed to deliver a low-skew clock signal to the entire chip, and are used for most internal clocking. They must be used when a single clock needs to drive the entire chip. Each XC4000EX device contains eight Global Low-Skew Buffers.
- **Global Early Buffers** - provide faster clock access than Global Low-Skew Buffers, but have a limited distribution capability. Each buffer can only supply a clock signal to 1/4 of the CLBs and 1/4 or 3/8 of the IOBs. Each XC4000EX device contains eight Global Early Buffers.
- **FastCLK™ Buffers** - specifically designed to provide the fastest possible I/O clocks. The only access they have to CLBs is through local interconnect. Using the FastCLK buffers enables near 100 MHz chip-to-chip communication. Each XC4000EX device contains four FastCLK Buffers.

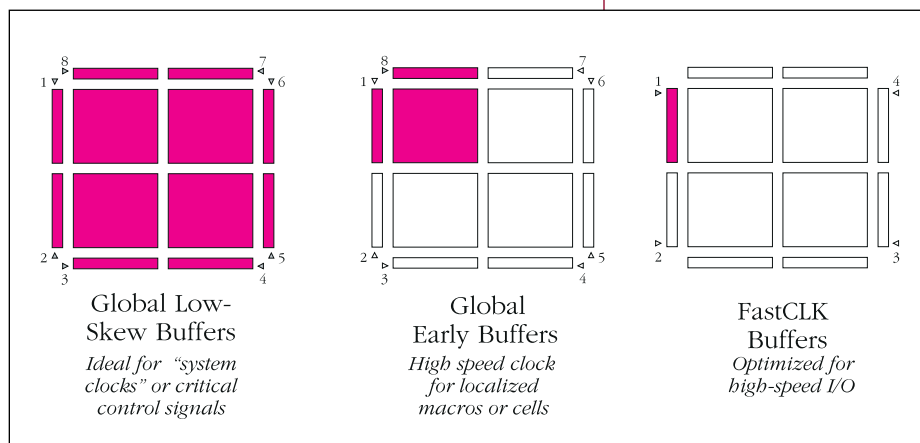
**Figure 2** shows the portion of a device that can be driven in a typical application by the three buffer types. Global Low-Skew and Global Early Buffers can drive

any of eight vertical long lines in each column. These long lines are separate from the vertical long lines used for standard interconnect.

## Development System Support

Software is the key enabling technology for maximizing the power, flexibility, and performance capabilities of the XC4000EX. Xilinx and its Alliance Partners are fully-prepared to support the XC4000EX with the industry's most powerful and versatile suite of design tools. Support for HDL-based, ASIC-like design methodologies is a key part of this strategy.

The recent merger of Xilinx and NeoCad provided a unique opportunity to combine the best software elements from the two companies. The merger took place during the development of the XC4000EX. A software tool, the FPGA Architect, developed by NeoCad, was used to evaluate design trade-offs and



maximize the ultimate performance and routability of the devices.

In summary, the new XC4000EX family extends the capacity, performance and system-integration capabilities of the popular XC4000 FPGA series to unprecedented levels. Both advanced processing technology and architectural enhancements have contributed to these dramatic improvements. The XC4000EX FPGA is the ideal logic device for high-density, high-performance applications. ♦

Figure 2 - XC4000EX Clocking options (shaded area indicates reach of a typical single buffer)