

Applications Update:

PCI, ATM, DSP, Plug & Play, RC

PCI (*Peripheral
Component
Interconnect Bus*)



Product News — Xilinx is now shipping three 100-percent PCI-compliant product families:

- **XC4000E-3** and faster speed grades in plastic quad-flat packages. Gate densities ranging from 5,000 to 13,000 gates. On-chip RAM provides burst FIFOs for the industry's fastest PCI data transfer rate in a programmable device.
- **XC3100A-2** and faster speed grades in plastic quad-flat packages.
- **XC7300-10** and faster speed grades in plastic quad-flat packages.

Application Notes —

- **Xilinx XC4000E PCI System Module Design Guide** describes a fully-verified PCI Target and Initiator macro for the XC4000E family.
- **Fully Compliant PCI Interface in an XC3164A-2 FPGA.**

- **Designing Flexible PCI Interfaces With Xilinx EPLDs.**

Other Projects — Xilinx Applications has developed a **PCI Target and Initiator** macro for use with the XC4000E. This macro provides a single-chip, fully-verified, 100-percent PCI-compliant, 33 MHz solution. Integrated burst FIFOs provide the highest data transfer rate of any programmable logic-based solution.

The fully-verified 100% PCI-compliant Target macro was released to beta-site customers in mid-October. Fully-verified PCI Target and Initiator designs will be released to the general design community by February, with limited release to select customers by the end of 1995.

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Telecom- munications

Product News —

- **XC5200** FPGA family provides an excellent solution for most telecommunications design. It combines good performance with low cost in a flip-flop intensive architecture.

- **XC4000E, XC3100A, and XC7300** are ideal for higher-performance telecommunications applications such as ATM, SONET, etc.

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Digital Signal Processing

Product News—

- **XC4000E** FPGA family in production. The on-chip RAM increases the effective density of many DSP designs. The added performance of XC4000E carry chains boost overall performance.
- **XC6200** FPGA provides an ideal solution for imbedded co-processing designs. The XC6200's fine-grain, regular architecture is useful in systolic array, image processing and computationally-intensive applications. The integrated processor bus interface provides a

high-bandwidth connection to standard microprocessors or DSP processors.

Application Notes — **16-Tap, 8-Bit FIR Filter Applications Guide** describes how to build a filter using Sequential Distributed Arithmetic (SDA).

Other Projects — Implemented a fully-parallel version of the 16-tap, 8-bit FIR filter, providing users with a higher-performance solution (*see Table 1*). An application note will be available next quarter.

Table 1 — Performance of a 16-Tap, 8-Bit FIR Filter Design.

"PROCESSOR"	SAMPLERATE	CLBS
XC4003E-3 using Sequential Distributed Arithmetic (SDA)	8.1 Mhz	68
XC4010E-3 using Parallel Distributed Arithmetic (PDA)	48 Mhz	390
XC4013E-3 using Parallel Distributed Arithmetic (PDA)	55 Mhz	432
50 MHz Fixed-Point DSP Processor	3.125 Mhz	N/A

Conference Papers and Articles —

"A distributed arithmetic approach to designing scaleable DSP chips," Bernie New, *EDN*, August 17, 1995, pages 107-112.

"Using Programmable Logic to Accelerate DSP Functions," Steve Knapp, Designing with Programmable Logic Devices Seminar, October 17-24, 1995, *Asian Electronics Engineer*.

"Using Xilinx FPGAs to Design Custom Digital Signal Processing Devices," Greg Goslin, *Proceedings of DSP*

Deutschland 95, September 25,26, 1995, pages284-294.

"Using FPGAs in Digital Signal Processing Applications," Greg Goslin, ICSPAT'95/DSP World Expo, October 24-26, 1995.

"Using Xilinx FPGAs for Application-Specific DSP Algorithms," Greg Goslin, ICSPAT'95/DSP World Expo, October 24-26, 1995.

"The FPGA as FFT Processor," Les Mintzer, ICSPAT'95/DSP World Expo, October 24-26, 1995.

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Product News —

- **Windows 95** released. Plug and Play is a major feature.
- **XC5200** in production. Though the application note is written for XC4003, the design also fits into the lower-cost XC5204.

Application Note — Plug and Play ISA

Using Xilinx FPGAs describes how to build a Plug and Play interface in an XC4003 FPGA. The same design also fits into the lower-cost XC5204

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Plug and Play - ISA Bus

Product News —

- **XC6200** FPGA provides an ideal solution for reconfigurable co-processing. The XC6200's integrated processor bus interface provides a high-bandwidth connection to standard microprocessors or DSP processors. This interface offers fast configuration (< 1 ms) and fast partial reconfiguration.
- Newer FPGA families include faster configuration methods. The **XC5200** family offers Express Mode which provide eight times faster configuration.

Application Notes — Configuring

FPGAs Over a Processor Bus. Useful to any designer that wants to program an SRAM-based FPGA from the processor bus.

Other Projects — Reconfigurable Computing Developers Program (see page 35)

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Reconfigurable Computing