

XC4000 Drives 3.3 V Devices Safely

Although a variety of 3.3 V components are becoming available, some systems require a mix of 3.3 V and 5 V devices. Xilinx offers several solutions for such mixed-voltage systems. Among these are the 5 V XC4000 and XC4000E FPGA families; their output buffers can safely drive either 5 V or 3.3 V devices.

The XC2000 and XC3000/XC3100 family devices have complementary outputs that require some current-limiting resistor when driving 3.3 V devices in order to protect the inputs and ESD protection circuitry of the 3.3 V device. In contrast, the XC4000 FPGAs have n-channel-only, totem-pole-like outputs that are more gentle driving V_{OH} . The XC4000H and XC4000E devices offer both types of outputs; the totem-pole-like outputs are available in the TTL output mode.

The table lists the worst-case output current for three FPGA families, assuming a 5.0 V supply for the FPGA. (The numbers on page 9-23 of the *Data Book* are typical, not worst-case). For higher or lower supply voltages, adjust the output voltage accordingly, one-to-one; that is, apply the V_{CC} error directly to the output voltage, mV for mV.

The input of a 3.3 V device will have negligible input current until the input

voltage is 0.6 V or more above the nominally 3.3 V supply. Even if an XC4000 output is driving a 3.3 V device with a worst-case supply voltage of 3.0 V, the XC4000 output will forward-bias the input protection diode with less than 1 mA, which is not sufficient to cause harm or latch-up on any reasonably designed CMOS input. Thus, all XC4000 outputs (as well as XC4000E and XC4000H outputs in TTL mode) can directly drive the inputs of 3.3 V logic devices safely without requiring current-limiting resistors. ♦

LOW
POWER

OUTPUT VOLTAGE V_{OH}	MAXIMUM OUTPUT CURRENT		
	XC4000	XC3000A	XC3100A
5.00	65 nA	55 nA	2 μ A
4.50	45 nA	-20mA	-18 mA
4.00	22 nA	-39mA	-34 mA
3.90	zero	-43mA	-37 mA
3.70	-20 μ A	-49 mA	-43 mA
3.50	-1.0 mA	-56 mA	-48 mA
3.30	-3.5 mA	-62 mA	-54 mA
3.00	-9 mA	-71mA	-62 mA
2.50	-24mA	-84 mA	-73 mA
2.00	-46mA	-95 mA	-82 mA
1.50	-72mA	-104 mA	-90 mA
1.00	-100 mA	-110 mA	-95 mA
0.50	-130 mA	-113 mA	-98 mA
0.00	-160 mA	-114 mA	-99 mA

for some telecommunications or industrial applications, where, once configured, the device configuration is maintained for weeks, months or even years.

Xilinx FPGA configuration data is extremely robust and reliable while V_{CC} stays within specification. (See related article on page 32.) As a result, there is no reason to worry about the reliability of Xilinx configuration bits. When required by the

system specification to read back the configuration data and compare it against the content of the original configuration bitstream, the user will have this confidence confirmed. **This readback operation does not interfere with the normal operation of the device.** In fact, it is possible to use logic implemented in an FPGA to process the data obtained during a readback of its own configuration memory. ♦