

Sensitivity to Power Glitches

LOW
POWER

32

Any digital logic device with internal data storage in latches or flip-flops is sensitive to power glitches. This includes every microprocessor, microcontroller, and peripheral circuit. Only purely combinatorial circuits can be guaranteed to survive a severe power glitch without any problem.

Xilinx SRAM-based FPGAs store their configuration in latches that lose their data when the supply voltage drops below a critical value (substantially below 3 V for the 5 V devices). However, all configuration data is extremely robust and reliable while V_{CC} stays above 3 V.

All Xilinx configuration latches are implemented as cross-coupled, complementary inverters with active pull-down n-channel transistors and active pull-up p-channel transistors. Both High and Low logic levels have an impedance of less than 5 k Ω with respect to their supply rail. This impedance is a million times lower than the 5 Gigaohm polysilicon pull-up resistors used in typical SRAMs. Thus, the data in Xilinx latches is far more rugged and reliable than the data in popular SRAMs.

Most digital circuits rely on V_{CC} staying within specification. Xilinx FPGAs have an internal voltage monitoring circuit. Whenever the 5 V supply voltage dips below 3 V, the internal monitoring circuit causes the Xilinx FPGA to stop normal operation. All outputs go 3-state, and the device waits for the supply voltage to rise closer to 4 V, when it either demands (slave or peripheral mode) or initiates (master mode) a reconfiguration. (In the range from 5 V down to 3 V, all CMOS devices maintain their functionality and their data storage, they just get slower as the voltage goes down.)

Xilinx has made sure that the FPGA cannot be corrupted by a power glitch. The most sensitive circuit is the low-voltage detector. It kicks in while all other configuration storage and user logic is still guaranteed to be functional. The voltage monitoring feature in the Xilinx device can even be used to protect other circuitry, or it can be coordinated with external monitoring circuits.

As a result of these careful precautions, we contend that Xilinx FPGAs are safer than all other types of circuitry (except purely combinatorial circuits). A microprocessor can lose the content of its address register, its accumulator or other control registers due to an undetected power glitch, with disastrous consequences to the subsequent operation. A Xilinx FPGA detects the power glitch and always plays it safe by flagging the problem.

No complex system of any kind can function reliably when V_{CC} is unreliable. Xilinx FPGAs do the safest thing possible, whenever such problems occur. ♦

Readback in FPGAs

All Xilinx SRAM-based FPGAs allow an unlimited number of **readback** cycles; that is, the user can read the contents of both the configuration memory and the registers within logic blocks. All the XC2000, XC3000, XC4000, and XC5200 family devices have similar readback mechanisms. (The XC6200 devices have a different readback mechanism).

The readback mechanism originally was intended for internal test purposes, not as a user-accessible function. How-

ever, there are two reasons why a user may want to initiate a readback operation:

- **To read the status of internal data storage elements**, as “a poor man’s In-Circuit-Emulator.” New software in XACTstep™ version 6, the Hardware Debugger, makes this process much easier and more versatile.
- **To verify that the configuration data is unchanged**. This is explicitly required by certain military applications, and it might also be meaningful

XC4000 Drives 3.3 V Devices Safely

Although a variety of 3.3 V components are becoming available, some systems require a mix of 3.3 V and 5 V devices. Xilinx offers several solutions for such mixed-voltage systems. Among these are the 5 V XC4000 and XC4000E FPGA families; their output buffers can safely drive either 5 V or 3.3 V devices.

The XC2000 and XC3000/XC3100 family devices have complementary outputs that require some current-limiting resistor when driving 3.3 V devices in order to protect the inputs and ESD protection circuitry of the 3.3 V device. In contrast, the XC4000 FPGAs have n-channel-only, totem-pole-like outputs that are more gentle driving V_{OH} . The XC4000H and XC4000E devices offer both types of outputs; the totem-pole-like outputs are available in the TTL output mode.

The table lists the worst-case output current for three FPGA families, assuming a 5.0 V supply for the FPGA. (The numbers on page 9-23 of the *Data Book* are typical, not worst-case). For higher or lower supply voltages, adjust the output voltage accordingly, one-to-one; that is, apply the V_{CC} error directly to the output voltage, mV for mV.

The input of a 3.3 V device will have negligible input current until the input

voltage is 0.6 V or more above the nominally 3.3 V supply. Even if an XC4000 output is driving a 3.3 V device with a worst-case supply voltage of 3.0 V, the XC4000 output will forward-bias the input protection diode with less than 1 mA, which is not sufficient to cause harm or latch-up on any reasonably designed CMOS input. Thus, all XC4000 outputs (as well as XC4000E and XC4000H outputs in TTL mode) can directly drive the inputs of 3.3 V logic devices safely without requiring current-limiting resistors. ♦

LOW
POWER

OUTPUT VOLTAGE V_{OH}	MAXIMUM OUTPUT CURRENT		
	XC4000	XC3000A	XC3100A
5.00	65 nA	55 nA	2 μ A
4.50	45 nA	-20mA	-18 mA
4.00	22 nA	-39mA	-34 mA
3.90	zero	-43mA	-37 mA
3.70	-20 μ A	-49 mA	-43 mA
3.50	-1.0 mA	-56 mA	-48 mA
3.30	-3.5 mA	-62 mA	-54 mA
3.00	-9 mA	-71mA	-62 mA
2.50	-24mA	-84 mA	-73 mA
2.00	-46mA	-95 mA	-82 mA
1.50	-72mA	-104 mA	-90 mA
1.00	-100 mA	-110 mA	-95 mA
0.50	-130 mA	-113 mA	-98 mA
0.00	-160 mA	-114 mA	-99 mA

for some telecommunications or industrial applications, where, once configured, the device configuration is maintained for weeks, months or even years.

Xilinx FPGA configuration data is extremely robust and reliable while V_{CC} stays within specification. (See related article on page 32.) As a result, there is no reason to worry about the reliability of Xilinx configuration bits. When required by the

system specification to read back the configuration data and compare it against the content of the original configuration bitstream, the user will have this confidence confirmed. **This readback operation does not interfere with the normal operation of the device.** In fact, it is possible to use logic implemented in an FPGA to process the data obtained during a readback of its own configuration memory. ♦