

# A Unique Product Strategy

by CHUCK FOX ♦ Vice President, Product Marketing

Xilinx is the world's largest supplier of programmable logic — approximately 50 percent larger than the second-largest supplier. We achieved that leading position through a continuing commitment to providing a complete product solution. This encompasses a focus on all three critical areas of the high-density PLD product solution **triangle: components, software and service.**

## Components

In components, we will continue to leverage new deep submicron process technologies aggressively to deliver improvements in speed, density and cost. We will combine this with innovative, targeted product families in all three major technology segments — CPLDs, reprogrammable FPGAs and one-time programmable FPGAs — supported by the industry's only seamless, no-risk cost-reduction path — the mask-programmed HardWire LCA. Each of these high-growth PLD technologies serves unique requirements in the industry.

**Xilinx is the only supplier to deliver leading solutions in all three of these high-growth technologies.** Our strategy is to continue to invest heavily in the research and development of innovative solutions in each area. Recently, we have introduced new solutions in all three.

The **XC6200** family of reprogrammable FPGAs provides extremely fast, in-system configuration speeds (as low as 40 ns/cell) and a unique, high-speed dedicated microprocessor interface. These features are ideal for using FPGAs in high-speed "reconfigurable coprocessing" applications.

The **XC8100** series of one-time programmable FPGAs, featuring the industry's first Sea-of-Gates FPGA architecture, is based on a proprietary metal-to-metal antifuse technology called MicroVia™ that, when combined with a unique, fine-grained cell architecture, delivers a powerful, single-chip FPGA solution optimized for an ASIC-like design flow.

The **XC9500** series of CPLDs is the industry's first 5V FLASH solution, representing the next generation in In-System Programmable (ISP) capability. This CPLD family delivers a superior ISP capability targeted at today's total product life cycle requirements.

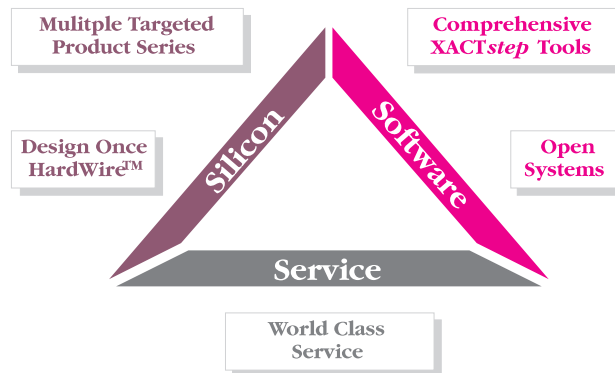
## Software

In software, our **open systems** strategy means we provide seamless integration into all the leading EDA environments, supporting popular front-end HDL, schematic, and simulation systems (as opposed to shipping our own proprietary front-end) as well as supporting industry standards such as EDIF, VHDL, Verilog-HDL and ABEL. We combine this with our comprehensive back-end XACTstep™ tools to provide a completely technology-independent design system supporting all our component

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## Xilinx Total Product Solution



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tions, as well as the traditional “glue logic” found in today’s FPGA designs. **Automatic placement tools** must support the effective placement of these various types of circuit structures, and will need to be augmented by interactive floorplanning tools. XACTstep™ version 6 includes a new version of PPR with improved structured-placement capabilities, as well as the industry’s first FPGA floorplanner. The synthesis tools will need links to the automatic placement and floorplanning tools, allowing for the passing of design constraints and the back-annotation of timing information.

With large designs, design iterations and last-minute changes are even more inevitable than they are today. Thus, the implementation tools should be re-entrant and tolerant of change, so minor logic changes do not cause major alterations in the physical layout. Xilinx pioneered re-entrant FPGA implementation tools with

the Guide option in PPR.

Accurate **simulation** should be available at any point in the design cycle using a common set of simulation vectors. This means that the post-place-and-route timing results need to be back-annotated into the original netlist created by the synthesis program, as opposed to creating a new netlist based on the structure of the FPGA. Once again, this implies a “synthesis-friendly” FPGA architecture, a synthesis compiler capable of efficient technology mapping to that architecture, and a strong link between the synthesis compiler and the “place and route” tools.

Design errors are reduced and design cycles are compressed when users don’t need to re-invent common functions. Many leading ASIC providers give users large, pre-defined macro functions, sometimes called cores or megacells. As FPGA densities increase, users should expect similar **large macro functions** to be

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families. Xilinx is committed to providing the best programmable logic design system in the industry with an integrated solution capable of meeting all of your PLD design requirements.

This quarter, we began shipping a major new version of our leading development software. **XACTstep version 6** delivers six new, Windows®-based productivity tools, providing easy-to-use yet powerful design capability. All Xilinx users under warranty are now receiving their updates. Try it — we guarantee you’ll like it.

## Service

Providing global, world-class manufacturing, technical support, and sales/distribution support is an essential **foundation** of our product strategy. Many PLD companies severely underestimate the importance of service to the user base. You may have already used one of the several, new, automated technical support facilities that we’ve established this year, such as XDOCS, XFACTS or our home page on the World Wide Web.

In summary, our product strategy is simple but unique: provide leading solutions in all three high-growth segments of the programmable logic industry — complex PLDs, reprogrammable FPGAs, and one-time programmable FPGAs — support them with the industry’s easiest-to-use yet powerful XACTstep integrated software solution, and deliver unquestioned world-class service. Let us know how we’re doing. ♦

## Solving the Broad Spectrum of Requirements

