

# Introducing the FastFLASH XC9500

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The new XC9500 family is the second generation of Xilinx CPLDs, developed especially for system designers who require complete in-system programming, test and manufacturing capability. The XC9500 family provides a total product life cycle support solution from initial



prototyping to system integration, manufacturing and field upgrades. It also offers the industry's best pin-locking capability, a necessity for maintaining device pinouts throughout the complete product life cycle.

The innovative FastFLASH technology provides exceptional in-system programmable (ISP) capabilities by offering more than 10,000 program/erase cycles — one or two orders of magnitude more than other comparable CPLDs. This high endurance level allows the XC9500 devices to be used in applications requiring frequent field upgrades and reconfigurations.

In addition, the XC9500 family provides both superior density and performance, with seven devices ranging in density from

800 to 6,400 usable gates, and pin-to-pin propagation delays as fast as 5 ns.

## Product Features

- High-performance
  - 5 ns pin-to-pin logic delays on all pins
  - Maximum external frequency to 145 MHz
- Large density range
  - 36 to 288 macrocells with 800 to 6,400 usable gates
- 5 V in-system programmability (ISP)
  - Endurance of 10,000 program/erase cycles
  - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
- Extensive IEEE 1149.1 boundary-scan (JTAG) support
- Programmable speed/power options on individuals macrocells
- Slew rate control on individual outputs
- User programmable ground pins capability
- Extended pattern security features for design protection
  - Read security bit prevents unauthorized copying of design
  - Write security bit protects against inadvertent user programming/erase
- High-drive 24 mA outputs with 3.3 V or 5 V I/O
- 100-percent PCI compliant (-10, -7 speed grades)
- Advanced 0.6µm CMOS 5 V FastFLASH technology

## Product Life Cycle Support

During the prototyping stage, a device might be reprogrammed hundreds of times while soldered on a printed circuit board (PCB). If the architecture does not support locking the device pinout, an expensive and time-consuming re-layout

# Family *The Industry's Most Complete Solution for In-System Programmable CPLDs.*

of the PCB is necessary. The XC9500 family provides industry-leading pin-locking capability for preserving PCB board layout throughout the design cycle.

When the entire system is assembled for test and debug, all important logic states should be easily accessible, and internal logic implementations within each CPLD should be capable of being checked. Each XC9500 device supports the IEEE 1149.1 boundary scan specification, including INTEST and USERCODE instructions used to access and debug user logic and track pattern revisions, respectively. In addition, both the superior pin-locking and high endurance features of the XC9500 family are critical in facilitating design modifications during the debugging process.

## Full JTAG Support

The XC9500 family expands the manufacturing process capability with the industry's most complete IEEE 1149.1 JTAG support. By integrating device programming with final board testing, the XC9500 technology eliminates the need for stand-alone mark and programming steps. Built-in version control, concurrent programming of multiple devices and in-system board customization all contribute to manufacturing flexibility.

Since the XC9500 family is easily programmed through the JTAG port, field upgrades to the CPLD's configuration are possible. The industry's best pin-locking architecture ensures against changes to the PCB layout.

## Simple Yet Flexible Architecture

Each XC9500 device may be viewed as a subsystem consisting of "36V18-type" Function Blocks and I/O Blocks interconnected by

the FastCONNECT™ switch matrix. As you have come to expect from Xilinx CPLDs, the full FastCONNECT switch matrix provides 100-percent interconnect of all pins and function block outputs to all function block inputs. Additionally, wide function block fan-in (36 total inputs) and flexible product term allocation work with the FastCONNECT matrix to ensure that design changes will not cause changes to the device pinouts.

The XC95108, featuring approximately 2,400 usable gates and up to 160 I/O pins and its software support tools are available now. The remaining six devices in the XC9500 family will become available throughout 1996.

The new XC9500 CPLD family, based on the industry's first 5 V Flash ISP process, provides CPLD users the best solution for addressing their needs throughout the entire product life cycle: design, system integration, volume manufacturing, and field upgrades. ♦

## XC9500 Architecture

