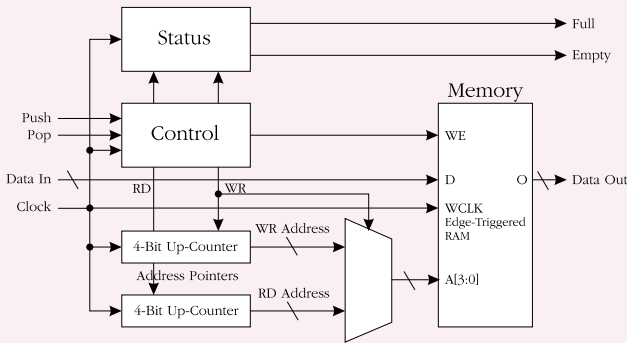
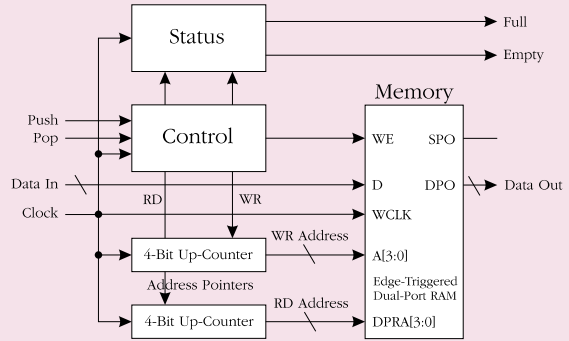


multiplexers was offset by the routing requirements of the increased number of address lines. Although the clock frequency is approximately 60 MHz, the

same as the single-port implementation, simultaneous read and write allows a data transfer rate equivalent to 120 MHz in a single-port FIFO. ♦



**Figure 2:** *FIFO with edge-triggered RAM*



**Figure 3:** *Dual-port FIFO with edge-triggered RAM*

## Mixing 3.3 Volt and 5 Volt Devices

In the past, almost all digital logic devices operated on a 5 volt standard. To reduce chip size and meet the demand for higher integration and reduced power consumption, the semiconductor industry has started the transition to 3.3 V logic. In the future, 3.3 volts is likely to become the dominant supply voltage. For the time being, designers must accommodate both types of ICs in the same design. What are the potential problems?

### 3.3 V Devices Driving Inputs on 5 V Devices

The lowest output High voltage ( $V_{OH}$ ) must be high enough to exceed the  $V_{IH}$  requirements of the 5 V device. This is not a problem if the 5 V device uses TTL-compatible input thresholds, available on all Xilinx devices. If the 5 V device has CMOS input thresholds, a pull-up resistor to 5 V on each such input will assure a sufficiently High input voltage. The resistor should be somewhere between 10 k $\Omega$  and 1 k $\Omega$  in value. The upper limit causes the rising input transition to be slow; the lower limit is set by the output current sinking capability of the 3.3 V device output. In the High state, the voltage will be clamped by the protection diode of the

3.3 V device. With only 1 V across the resistor, this current will be fairly small, but care should be taken that the sum of these pull-up currents does not exceed the 3.3 V supply current, thereby reverse-biasing and raising the 3.3 V supply voltage.

### 5 V Devices Driving Inputs on 3.3 V Devices

The highest output voltage may not force excessive current into the input of the 3.3 V device. If the 5 V device has a truly complementary CMOS output (like all Xilinx FPGAs and CPLDs except the XC4000 family devices), then the input current must be limited by a series resistor of no less than 100  $\Omega$ . This guarantees an input current below 10 mA, flowing through the input protection diode backwards into the 3.3 V supply. Care must be taken to avoid raising the nominally 3.3 V supply voltage above its 3.6 V maximum when a large number of active High inputs drive the 3.3 V device.

If the 5 V device has "totem-pole" n-channel only outputs,  $V_{OH}$  is reduced by one threshold and the series resistor can be reduced or even eliminated, provided the nominally 5 V supply never exceeds 5.25 V. ♦