

Building FIFO Memories in the XC4000E



First-in-first-out memories (FIFOs) receive three significant benefits from the new edge-triggered RAM option of the XC4000E architecture:

- Greatly simplified logic design due to the elimination of timing from the external write enable pulse.
- Fewer data and control logic registers and logic blocks required because synchronization is performed by the WCLK pulse within the RAM.
- An approximate doubling of the overall speed compared with conventional designs.

The remarkable speed improvement results from the elimination of the external write enable signal as the active control. In a traditional FIFO design using level-sensitive RAM, two methods are available to generate the write enable. An external 2x clock can be used to generate a pulse in the third quarter of the FIFO clock period, or the falling edge of the FIFO clock can be used to trigger a glitch on write enable. (The latter method is

settle prior to initialization of the Write Enable pulse.

By redesigning the same FIFO to use edge-triggered RAM, an entire clock pulse is available for data and address lines to settle. For FIFOs of any size, loading on the address lines usually determines the speed of operation for the FIFO. Therefore, the modified FIFO operates at about twice the speed of the level-sensitive version.

Figure 2 shows a block diagram of the edge-triggered FIFO. The divide-by-two on the clock has been removed, along with the logic generating the RAM write enable pulse. The registers on data and control inputs are also no longer necessary.

A FIFO in a PCI (Peripheral Component Interconnect) bus interface must operate at 33 MHz, and is typically 8 or 16 words deep by 32 bits wide. A 16x32 PCI write FIFO was implemented using a portion of a PCI-compliant Xilinx XC4005E-3. Using the level-sensitive RAM mode, PCI performance was met, but not exceeded. Switching to edge-triggered mode, a FIFO was produced that reliably runs at 60-65 MHz, without any manual editing required.

Dual-Port FIFO

To implement a FIFO that can read and write at the same time, use only the DPO output. A[3:0] is the write address, and DPRA[3:0] is the read address. The multiplexer on the address lines can be removed. The arbitration logic in the Control block, which normally selects between a Read and a Write operation when both commands are received simultaneously, can also be removed.

The block diagram for a dual-port edge-triggered FIFO is shown in Figure 3. The original nine logic blocks in Figure 1 are reduced to five.

When the PCI FIFO referenced above was modified to use dual-port RAM, the operating frequency was about the same — the advantage of removing the address

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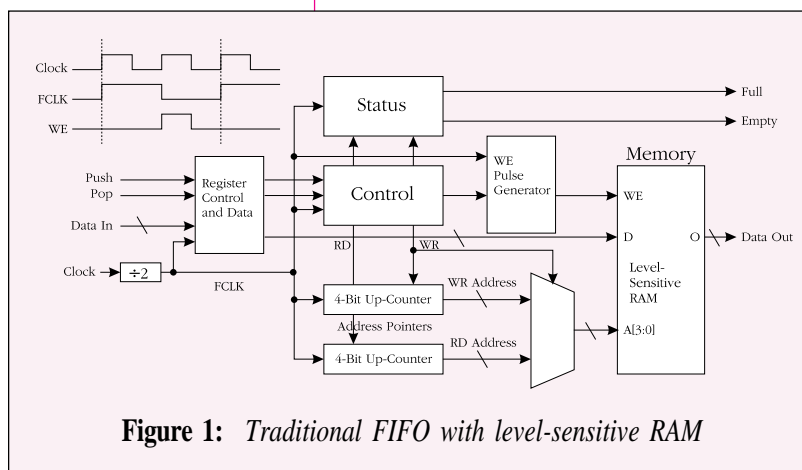


Figure 1: Traditional FIFO with level-sensitive RAM

discouraged because of the risks inherent in internal race conditions.)

A block diagram of a FIFO using an external 2x clock and level-sensitive RAM is shown in Figure 1. Whichever method is used, only half of a FIFO clock period is available for data and address lines to

multiplexers was offset by the routing requirements of the increased number of address lines. Although the clock frequency is approximately 60 MHz, the

same as the single-port implementation, simultaneous read and write allows a data transfer rate equivalent to 120 MHz in a single-port FIFO. ♦

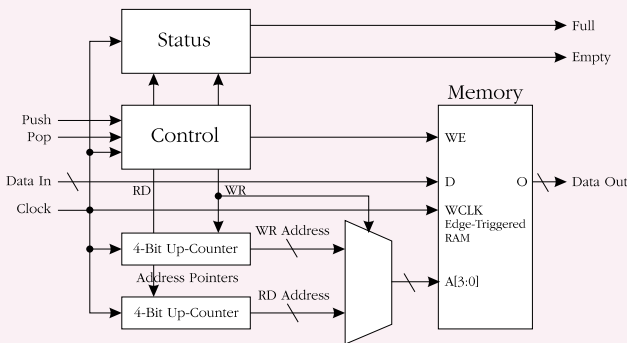


Figure 2: *FIFO with edge-triggered RAM*

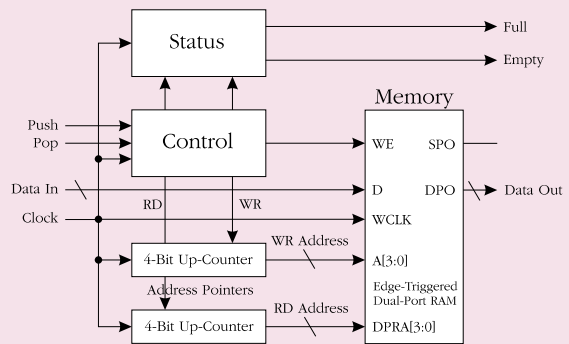


Figure 3: *Dual-port FIFO with edge-triggered RAM*

Mixing 3.3 Volt and 5 Volt Devices

In the past, almost all digital logic devices operated on a 5 volt standard. To reduce chip size and meet the demand for higher integration and reduced power consumption, the semiconductor industry has started the transition to 3.3 V logic. In the future, 3.3 volts is likely to become the dominant supply voltage. For the time being, designers must accommodate both types of ICs in the same design. What are the potential problems?

3.3 V Devices Driving Inputs on 5 V Devices

The lowest output High voltage (V_{OH}) must be high enough to exceed the V_{IH} requirements of the 5 V device. This is not a problem if the 5 V device uses TTL-compatible input thresholds, available on all Xilinx devices. If the 5 V device has CMOS input thresholds, a pull-up resistor to 5 V on each such input will assure a sufficiently High input voltage. The resistor should be somewhere between 10 k Ω and 1 k Ω in value. The upper limit causes the rising input transition to be slow; the lower limit is set by the output current sinking capability of the 3.3 V device output. In the High state, the voltage will be clamped by the protection diode of the

3.3 V device. With only 1 V across the resistor, this current will be fairly small, but care should be taken that the sum of these pull-up currents does not exceed the 3.3 V supply current, thereby reverse-biasing and raising the 3.3 V supply voltage.

5 V Devices Driving Inputs on 3.3 V Devices

The highest output voltage may not force excessive current into the input of the 3.3 V device. If the 5 V device has a truly complementary CMOS output (like all Xilinx FPGAs and CPLDs except the XC4000 family devices), then the input current must be limited by a series resistor of no less than 100 Ω . This guarantees an input current below 10 mA, flowing through the input protection diode backwards into the 3.3 V supply. Care must be taken to avoid raising the nominally 3.3 V supply voltage above its 3.6 V maximum when a large number of active High inputs drive the 3.3 V device.

If the 5 V device has “totem-pole” n-channel only outputs, V_{OH} is reduced by one threshold and the series resistor can be reduced or even eliminated, provided the nominally 5 V supply never exceeds 5.25 V. ♦