

Improved Synthesis Support for EPLDs

Synthesis users have plenty of reasons to try the new and improved XACTstep version 6. This latest version of the Xilinx core software has been optimized for synthesis, providing significant improvements in speed and density among several new features that make EPLD designs easier to develop. Improvements include:

- **Logic Optimization** - XACTstep EPLD implementation tools automatically produce shorter cycle times, shorter setup times, and reduced pin-to-pin delays. The EPLD fitter now uses refined algorithms for flattening gate level logic produced from synthesis, resulting in better overall speed and density. Table 1 details performance improvements seen in actual customer designs.
- **Timing Driven Optimization** - XACT-Performance™ optimizes designs based on user-specified timing requirements. The software now supports path-timing constraints for EPLDs in the same manner as for any other ASIC technology; for HDL-based designs, these timing specifications are expressed directly through the synthesis tool interface. Timing specifications are automatically transmitted to the XEPLD fitter using the same TIMESPEC attributes currently used for Xilinx FPGAs. The task of producing high-performance designs is now a lot easier.
- **Full Timing Analyzer** - XACTstep version 6 includes a new timing analyzer that can create a variety of reports to meet specific needs. These reports can provide summaries of the full system or just specific paths and path types. This new EPLD timing analyzer is now compatible with the Xilinx FPGA timing analyzer. Timing reports

are easier to read with more detailed information.

Xilinx is committed to providing the best synthesis support in the programmable logic industry with on-going support and development for many third-party synthesis tools, including:

- Synopsys - FPGA Compiler, Design Compiler logic synthesis; VSS full-timing simulation.
- Exemplar - Galileo version 3 logic synthesis (new from Exemplar).
- ViewLogic - ViewSynthesis logic synthesis

“Xilinx is committed to providing the best synthesis support in the programmable logic industry with on-going support and development for many third party synthesis tools.”

Table 1: Cycle Time and Density Improvements in XEPLD 6.0

	XEPLD5.1 Device	Macro- cells	tCYCLE		XEPLD6.0 Device	Macro- cells	tCYCLE
1	7336-5PC44	32	28.0ns		7336-5PC44	16	10.4ns
2	73108-7PC84	76	31.0ns		7354-7PC44	25	10.5ns
3	73108-10PQ160	82	31.0ns		73108-10PQ160	75	16.0ns
4	73144-10PQ160	95	49.0ns		73108-10PC84	95	31.0ns
5	None (No Fit)	(142)	-		73144-10PQ160	105	38.5ns

This table is based on customer designs that were expressed in generic VHDL with no instantiations. The designs were processed by the Synopsys FPGA compiler, targeting the Xilinx XC7000 library, to produce XNF netlists. The netlists were processed with the indicated version of the XACT fitter, using default options and no timespecs.

For most designs there is a significant improvement in cycle time, and density is often improved enough to allow use of a smaller device. So, higher performance designs are produced at a lower cost.

- Cadence - Synergy logic synthesis; Verilog timing simulation.
- Mentor Graphics - AutoLogic logic synthesis.
- Data I/O - Synario and ABEL HDL logic synthesis.

Continued on the next page

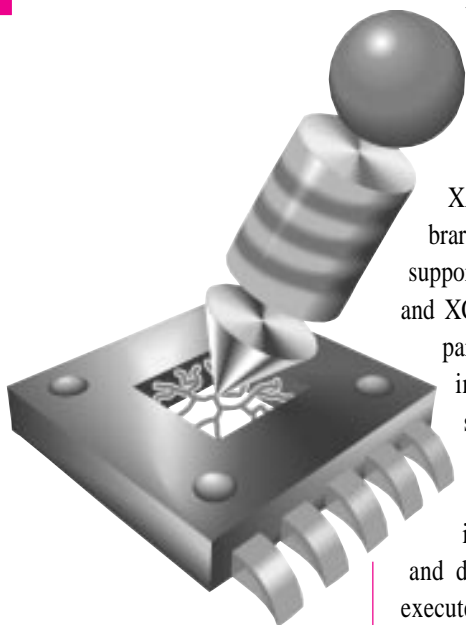
New $X_S A_T C_E T_P$ Advanced Design System

As reported in *XCELL* #17, Xilinx has merged with NeoCAD, Inc. of Boulder, Colorado, a leading supplier of FPGA design software. As a result of the merger, Xilinx recently brought to market a new FPGA design system called the XACTstep™ Advanced package — the first new product offering that leverages the NeoCAD software technology.

The Advanced package features XACTstep Foundry, NeoCAD's core design system for FPGA implementation (formerly called NeoCAD FPGA Foundry), bundled with the XACTstep system from Xilinx (formerly called XACT).

XACTstep Foundry, featuring advanced timing driven placement and routing technology, has a proven track record for helping users achieve maximum utilization and performance for Xilinx FPGA designs.

XACTstep Foundry is netlist and library compatible with XACTstep, and supports the Xilinx XC4000, XC3100/A, and XC3000/A FPGA families. It adds particularly significant value to the implementation of high-density designs, and includes support for the XC4025. XACTstep Foundry includes optional high-level synthesis integration, multi-device partitioning and distributive processing capabilities. It executes on PCs and workstations, including Sun Solaris.



The XACTstep Advanced package is available now. Easy upgrade paths for existing XACT and NeoCAD FPGA Foundry users also are available. **Contact your local Xilinx sales representative for ordering information.** ♦

Update News

The latest revision of XACTstep Foundry (version 7) was shipped this summer to NeoCAD FPGA Foundry owners with a Xilinx configuration and active maintenance contract.

XACTstep version 6 updates are scheduled for first customer ship in October. Most users will receive their updates in the fourth quarter. XACTstep version 6 supports the XC2000, XC3000, XC3100, XC4000, XC5000, and XC7000 component families.

Xilinx is hard at work finalizing a new software technology strategy and release plan leveraging the best software technologies of both Xilinx and NeoCAD. New products integrating the best of XACTstep and XACTstep Foundry, scheduled for introduction in 1996, will result in unparalleled power, functionality and ease-of-use for FPGA designers. Details on these products will become available in the coming months. ♦

Synthesis Support

Continued from the previous page

Tools for both VHDL and Verilog HDL design entry are available. VITAL-compliant simulation models are available for a variety of third-party simulation tools including Cadence Verilog and Model Technologies. In addition, the EPLD physical device models are available from Logic Modeling, a division of Synopsys.

So, no matter what tools are used, Xilinx provides everything needed to produce high-performance EPLD designs with minimal effort.

For product availability or other information, please contact your local Xilinx representative. ♦