

# PCI Compliant $\neq$ PCI Suitable

By BRADLY FAWCETT ♦ Editor

The rapid adoption and proliferation of the PCI (Peripheral Component Interconnect) bus has been one of the computer market's major success stories of the past year.



Originally defined by Intel, PCI has become an industrywide standard controlled by a consortium — the PCI Special Interest Group, or PCI SIG. The high-performance PCI bus can handle the throughput demands of data-intensive applications such as multimedia and high-speed networking.

Full compliance to the PCI SIG specification is a must for systems and boards that will be sold in the general marketplace where interoperability among multiple vendors is required.

To achieve high throughput and ensure interoperability between a wide variety of boards and host systems, the PCI specification includes a strict definition of its electrical interface. IC components that can meet the performance, loading and drive requirements of this electrical interface are said to be "PCI-compliant." By submitting the appropriate paperwork, component suppliers that are members of the PCI SIG can have their compliant devices added to an "Integrators List" that is available to other PCI SIG members.

## Market Pressures and Marketing Tactics

PCI-related designs are a large potential market for high-density CPLDs and FPGAs. The flexibility of a programmable approach is attractive in a PC card market characterized by changing market needs and short product life cycles. These de-

vices are, in fact, finding their way into many prototype and production PCI designs. Thus, programmable logic vendors are working hard to establish themselves as suppliers to this market. One tactic is to submit as many devices as possible for inclusion on the PCI SIG's Integrators List, and then, based on their inclusion on the list, advertise these devices as being "PCI Approved" (or a similar designation).

Designers of PCI boards and systems are advised to be leery of these claims. First, the PCI SIG does not guarantee the compliance of any device or offer any form of approval; submissions to the PCI SIG are strictly on the "honor system" and are not verified independently. (In fact, the component section of the Integrators List specifically states that functional testing is not required to be listed. The PCI SIG disclaims responsibility for any errors in the listings.) The Integrators List is

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considered confidential to PCI SIG members and is for their convenience only. Again, inclusion on the Integrators List does not constitute any endorsement or approval by the PCI SIG.

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## Compliance No Simple Task

Secondly, and more importantly, being "PCI-compliant" does not necessarily mean these devices are suitable for use in a PCI application. Electrical compliance only guarantees that the device meets the bare minimum electrical characteristics. It does not guarantee that the device has the logic capacity, functionality and overall speed to effectively implement a PCI interface design—the device may or may not be suitable for a real-world design.

For example, the PCI specification allows a 10 pF maximum load on a bus signal (except the clock signal, which is allowed a 12 pF maximum load), as well as a maximum trace length of 1.5 inches from the card edge connector to limit trace capacitance. Taken together, these two factors imply that each bus signal attaches to only one IC pin per board (that is, a signal coming from the connector can have only one destination).

Practically speaking, all the interface logic would need to be implemented in a single device in a fairly small package (such as a quad flat pack) so that all the pins can be close to the connector. A simple PCI interface typically requires about 100 I/O, about 4,000 usable gates, and well over 100 registers. The need for a single-chip solution eliminates a lot of the smaller PALs and CPLDs that have found their way on to the Integrators List and are advertised as "PCI-compliant" by their manufacturers.

The internal architectures of some devices do not easily meet the needs of PCI interface design. For example, many PCI bus signals are bidirectional and must be driven by three-state buffers. Some FPGA and CPLD architectures limit the number of different output enables that may be present on the device. Target interfaces require a minimum of four output enables; initiators require at least

six. This is a bare minimum. It does not include the output enables needed for interrupts, controlling byte transactions, or connecting to the back-end logic. Real-world designs require several more output enables. Thus, devices with limited output enable capability are not practical for PCI designs.

## Beyond the Basics

There are, of course, many other issues. Can the device deliver the needed performance to operate at any frequency from 0 to 33 MHz? Do the development tools make it easy to control circuit speed along the critical paths? The PCI bus has to attach to something — what are the requirements of the back-end interface? Compliant electrical characteristics are just the first step in selecting a programmable logic device for PCI interface design. Labeling a product as "PCI-compliant" does not ensure suitability for a particular design.

Xilinx does offer several devices that are both electrically compliant and architecturally suitable for PCI interface implementations. These include the XC3100A and new XC4000E FPGA families, as well as the higher-density members of the XC7300 EPLD family. Xilinx components have already been used in a number of successful PCI designs. In fact, the PCI SIG chose a Xilinx XC3100A FPGA for a board included in their BIOS compliance test kit.

***For more information about programmable logic products for PCI designs, including application notes and reference designs, please contact us via E-mail at [pci@xilinx.com](mailto:pci@xilinx.com) or call your local Xilinx representative.***

Copies of the PCI specification can be obtained from the PCI Special Interest Group, P.O. Box 14070, Portland, OR 97214 (tel: 800-433-5177). ♦



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*P.S. Our thanks to the thousands of engineers who joined us for the Programmable Logic Breakthrough '95 seminars this spring. We know your time is valuable and we appreciate your participation*