

# The High-Performance XC4000E Family

*New Family Achieves 50 Percent Performance Increase Over the Popular XC4000 Family*

Xilinx has begun shipping the new XC4000E family, the successor to the popular XC4000 FPGA family. The XC4000E FPGA family increases performance over the existing XC4000 family by

XC4000E family is based on the XC4000 family architecture, XC4000E devices are backward compatible (i.e., drop-in, with the same bitstream) with the equivalent XC4000 devices.

Unique capabilities and features of the XC4000E FPGAs include:

- Up to 50 percent faster circuit speed (XC4000E-2 as compared to XC4000-4; see table on page 24)
- 60 percent faster carry chain for arithmetic functions
- Lower component prices than the XC4000 family
- Select-RAM memory reduces chip count and design time while increasing RAM performance by up to 2X
- Select-RAM memory is mode-selectable
  - synchronous/asynchronous
  - single-port/dual-port
- 100 percent PCI compliant and suitable



up to 50 percent, and is ideal for high-density, high-performance applications such as microprocessor bus interfacing, digital signal processing, image processing, and high-speed telecommunications.

This dramatic performance improvement results from an improved design, a new 0.5 $\mu$  triple-layer-metal process technology, and the new Select-RAM™ on-chip memory feature. The XC4000E family features eight devices ranging from 3,000 to 25,000 gates, including the XC4020E device, the first 20,000 gate device offered by Xilinx. (Higher-density devices will be announced later this year.) Since the

## Architectural Features of the XC4000E

The architecture of the XC4000E is a superset of the XC4000; XC4000E devices are bitstream and pin-compatible with the equivalent XC4000 family FPGAs. Thus, current designs using XC4000 FPGAs can take immediate advantage of the XC4000E's increased speed by simply inserting new devices into existing XC4000 sockets.

The XC4000E architecture features an enhanced CLB (configurable logic block) with several new modes for configuring on-chip memory (called Select-RAM). As with the XC4000 architecture, the CLB's look-up tables optionally can be used as

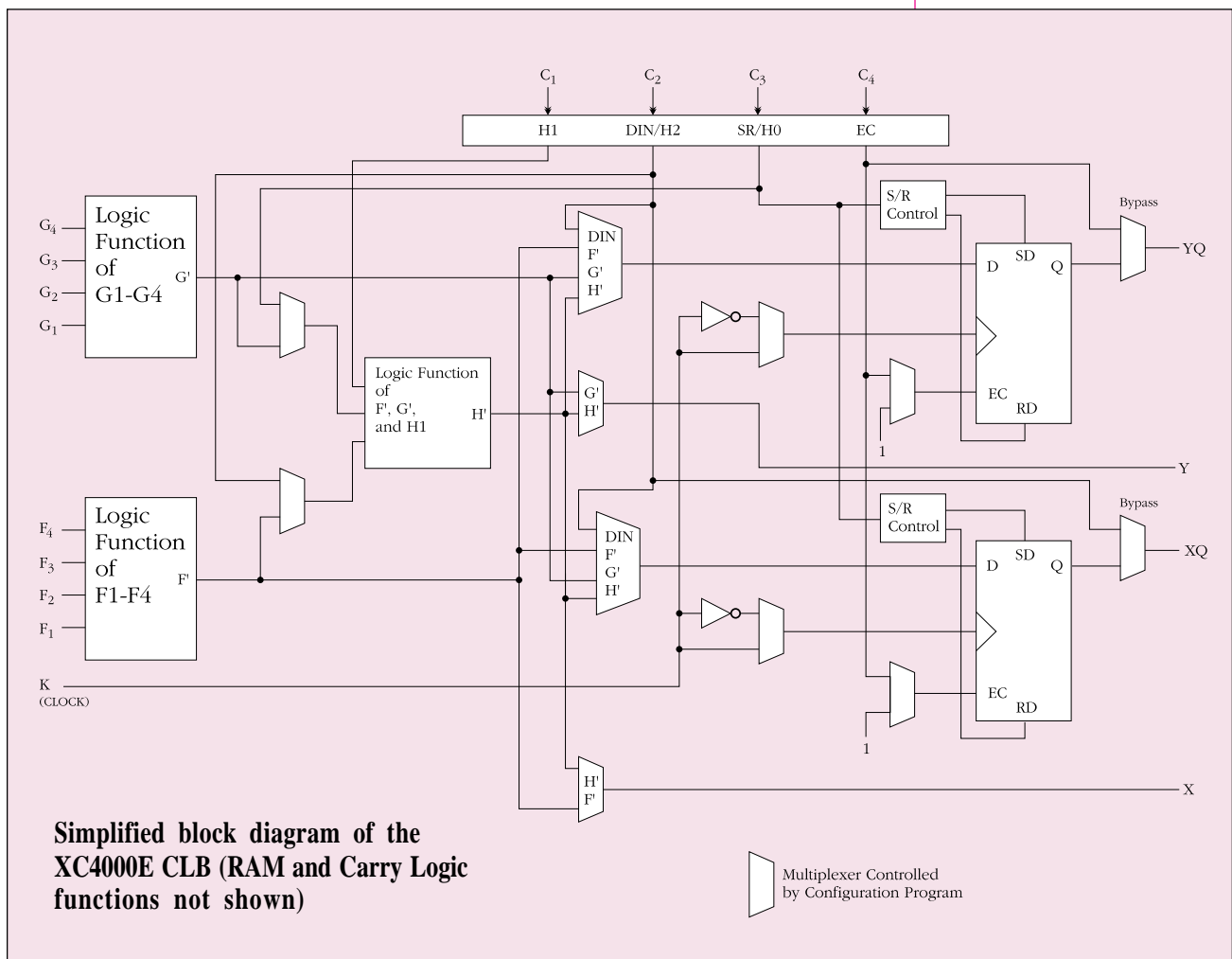
on-chip ROM or RAM memory; memory blocks of any size or width can be constructed from multiple CLBs and located anywhere in the array. The XC4000E extends that flexibility by adding an optional synchronous (edge-triggered) mode that simplifies the timing of the memory interface, and an optional dual-port mode that supports simultaneous read and write functions. Furthermore, the memory cells can be programmed during device operation or initialized as part of FPGA configuration. The synchronous and dual-port RAM modes ease the implementation of embedded configuration registers and on-chip data buffering in applications such as local area networking (LAN) switches, Peripheral Component Interconnect (PCI)

bus interfaces, and asynchronous transfer mode (ATM) controllers.

Additionally, the routing scheme of the XC4000E architecture was redesigned and optimized to improve CLB access and increase routing connectivity through the addition of more routing switches. New paths also were added within the CLB; the H function generator has two additional sources for inputs (*see figure*). This new architecture improves utilization and provides shorter wire lengths, thereby reducing interconnect delay.

Other new features include built-in clock enables for the registers in the I/O blocks, programmable TTL or CMOS input voltage thresholds and output levels, and “Soft Start-Up,” a feature that activates the

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## XC4000E

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output buffers with a slow slew rate at the end of the configuration process to avoid system noise. Once the I/O blocks are activated, slew rates are set to their programmed values.

### Begin Designing TODAY!

Because the XC4000E FPGAs are drop-in compatible with the equivalent XC4000

devices, you can begin exploiting the speed of the XC4000E-3 today using the existing XC4000 support software! Simply download the -3 speed files from the Xilinx bulletin board (in the Software Help area) and begin designing. You'll be able to program your XC4000E-3 the day it arrives. (Of course, this approach does not provide access to the new features of the XC4000E architecture.)

A new module for the new XACTstep system that allows users to take advantage of the enhanced features of the XC4000E family will be available in early 4Q95 at no charge to users with an active maintenance contract.

Table 2 lists the initial members of the XC4000E family and their projected availability.

Favorable reports have come in from early users of the XC4000E family. Jim Simkins, senior engineering specialist at E-Systems, a manufacturer of military and government systems, reports that "There are dramatic speed increases using the XC4025E device — in fact, up to two to three times in several cases. Currently, E-Systems is using an XC4025E device to implement a DSP function that processes 11.5 bops (billion arithmetic and storage operations per second), with an equivalent capacity of 170,000 LSI Logic gates." ♦

**TABLE 1:** *Example benchmarks*

	XC40XXE-2	XC40XXE-4
Data Path	156 MHz	109 MHz
State Machine	69 MHz	55 MHz
16 Bit pre-scaled counter	115 MHz	64 MHz
Address map decoder	71 MHz	50 MHz

**TABLE 2:**

DEVICE	DENSITY RANGE WITHOUT RAM (inusable gates)	DENSITY RANGE WITH RAM*	AVAILABILITY	
			Sampling	Production
XC4003E	2,500 - 3,000	4,000 - 6,000	4Q95	Q196
XC4005E	4,000 - 5,000	7,000 - 11,000	Now	4Q95
XC4006E	5,000 - 6,000	8,500 - 15,000	Now	4Q95
XC4008E	6,500 - 8,000	11,000 - 18,000	Now	4Q95
XC4010E	8,000 - 10,000	14,000 - 22,000	Now	4Q95
XC4013E	10,000 - 13,000	19,000 - 31,000	Now	4Q95
XC4020E	18,000 - 20,000	28,000 - 44,000	4Q95	4Q95
XC4025E	22,500 - 25,000	36,000 - 57,000	Now	4Q95

\*10% - 30% RAM usage

## XC8100 Production

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ProSynthesis, Exemplar, and Motive, as well as VHDL and Verilog models. (Contact your local Xilinx representative for more details or information about other interfaces.)

There are several significant new features in the Series 8000 software. First, all logic and nets, including hierarchy, are maintained by the back-end XC8100 tools, so this information is consistent for simulation and debugging; this feature is called TrueMap™ logic mapping. Second, a new router, called PowerMaze™, routes thousands of gates per second. Third, thanks to a new algorithm, Series 8000 software

can do incremental design within the synthesis environment. Fourth, patented circuitry and software allows every device to be 100 percent testable, including an automatic post-programming verification without test vectors.

### For more information

A data sheet and a product overview are available from your local Xilinx representative and on the Xilinx World Wide Web site. License-free demonstration software also is available. Contact your local Xilinx sales office or representative for the latest availability and pricing information. ♦