

# 155 Mbit/s Codec Uses Xilinx FPGAs

The Satellite Communications Research Centre (SCRC) of the University of South Australia in Adelaide is a space industry development center sponsored by the Australian Space Office.

In May of 1992, the SCRC secured a contract from Intelsat to build a 155 Mbit/s codec in a worldwide competitive bid. Intelsat is the world's largest commercial satellite communications service provider, owned by 120 member nations. The 155 Mbit/s codec was the first major high technology research and development contract awarded to an Australian institution.

The task was to develop and prototype a forward error correcting codec that would allow transmission of the standard 155.52 Mbit/s broadband ISDN data rate over a 72 MHz satellite transponder. The use of Xilinx FPGA technology was key to successfully implementing the codec.

After getting the contract, a group of six engineers, nicknamed Team 155 and led by Dr. Steven S. Pietrobon, spent the next 18 months simulating, designing, building, and testing the codec. The key to the codec was the efficient implementation of a multi-dimensional trellis code. The encoder that added the information required to implement the code was incorporated in an XC4002A. The decoder that removes errors induced by noise in the channel is much more complicated and required two XC4010s. However, this is still much less complex than other coding schemes that require up to nine ASICs or ECL gate arrays and provide inferior performance.

SCRC's previous experience with XC3000 technology and the new features provided by the XC4000 architecture (especially the fast carry logic and on-chip RAM features) allowed Team 155 to put the decoder on two XC4010s in the time available. A standard Reed Solomon code also was used. An XC4003 and XC4005 were used to interface to available Reed Solomon codec chips and provide the interleaving, de-interleaving, and synchro-

nization functions of the codec.

Viewlogic's WorkView and PowerView systems were both used for schematic capture and functional simulation of the FPGA designs; simulation was used extensively to test and debug the design before implementation. The use of X-BLOX™ and the reprogrammability of the Xilinx chips allowed design changes and improvements to be easily made and tested. Xilinx extended support to Team 155 by providing XC4010-5 devices (the fastest at the time)

and the latest software upgrades as they became available. This was especially important during the acceptance tests when the codec was being tested with the modem for the first time. The codec was initially not quite fast enough, resulting in marginal performance. Using recently-arrived software, another route was performed, and a few hours later Team 155 had a faster and accepted codec.

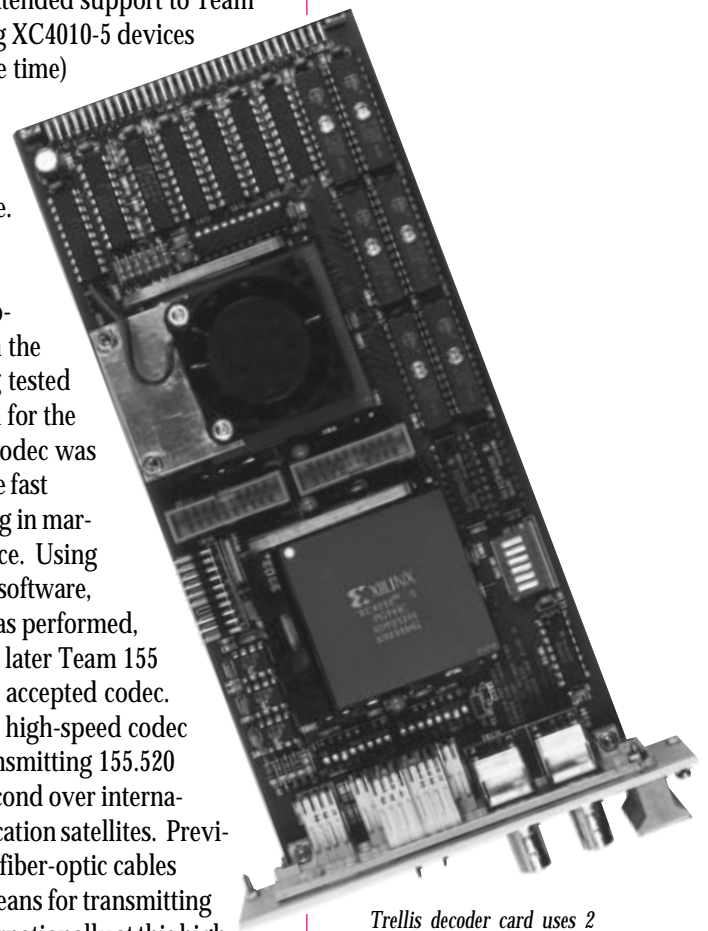
The resulting high-speed codec is capable of transmitting 155.520 Megabits per second over international communication satellites. Previously, undersea fiber-optic cables were the only means for transmitting information internationally at this high data rate.

The codec is currently being licensed to EF Data in Tempe, Arizona, where it is being incorporated into their modems. After delivery of the modems later this year, Intelsat will test this modem/codec with the satellites. The prototype modem/codec has already been successfully tested using a ground-based version of their satellites. ♦



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*Trellis decoder card uses 2  
XC4010 FPGAs*