

Total Cost and Time-to-Volume: The New Reality

By BRADLY FAWCETT ♦ Editor

While designers value the flexibility and convenience of a user-programmable device, the programmable elements and their associated control logic do exact a price in terms of silicon area. Thus, programmable devices generally cost more, on a per-piece basis, than equivalent-density custom and semi-custom ICs, such as masked gate arrays (although this gap is closing).



The choice between a high-density programmable device (an EPLD or FPGA) and a gate array often comes down to simple economics — designers want to use whichever one is most cost-effective for the application. However, determining the true “total cost” of a given technology in a given application is not at all a simple matter. If such an analysis includes only a comparison of unit prices at a given volume, the “break-even” point between FPGAs and gate arrays typically will be only a few hundred to a few

thousand pieces — even if the extra NRE (non-recurring charges) associated with semicustom devices are amortized into the gate array price. But such an analysis falls far short of revealing the true cost of the respective technologies.

Many other factors affect technology costs. These include development tool

costs, inventory costs, quality, vendor service, future component price reductions, design/market risks (i.e., will the design need to be modified after production shipments begin), and the potential for extra engineering and NRE costs due to design re-spins. Many of these costs can go unrecognized in a traditional cost analysis because they occur after the design cycle, or cut across many functional groups.

However, out of all the factors involved (including component costs), the two factors that tend to most heavily weight the programmable device vs. gate array cost analysis are engineering costs and time-to-market. In a typical scenario, studies suggest that these factors can move the “break-even point” between FPGAs and gate arrays to tens or even hundreds of thousands of units.

These factors are directly related. Engineering costs are higher and design cycles longer due to the extra steps required in semicustom IC development, especially exhaustive simulation and test vector generation.

This, combined with the significantly longer lead times required to produce prototypes and production quantities of gate arrays, can significantly increase the time-to-market for that product, as compared to a programmable solution. As many studies have shown, in today’s environment, even a small delay in time-to-market can have a significant

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impact on the overall profitability of a product. A late project's "total cost" will often be substantially higher than that of a project completed quickly.

Yet, it may be more accurate to think in terms of time-to-volume, rather than just time-to-market. Time-to-volume is a new term that reflects a product's total life cycle needs. The key is not only to get the product to market, but to quickly and seamlessly achieve required volume production price points. This is one of the key philosophies behind the Xilinx HardWire product line. FPGA devices can be used for development, debugging, prototyping, and initial production, thus

speeding time-to-market. In higher volume, they can be directly replaced by less-expensive, mask-programmed HardWire devices, with no redesign effort or risk; engineering resources are free to move on to the development of the next product.

Improving time-to-volume is the major thrust of the upcoming XACTstep, version 6 development system release. The focus is on accelerating all phases of the product development flow: design entry, design implementation (for the programmable logic), printed circuit board design, design debug, and product production. (See related article on pages 17-18.) Special attention has been paid to the often-overlooked design debug stage; surveys indicate that more than 50 percent of a designer's time is spent in design debug and change. So look for improved floorplanning tools and re-entrant "guide" options in PPR — to help ease the absorption of design changes late in the development cycle — and improved timing analysis and hardware debugging tools. Our goal is to provide the tools and technologies that will boost your productivity, reduce your total cost and shorten your time-to-volume. ♦

Xilinx ASIC Estimator Available for PC

Calculate the total cost of your project using Xilinx FPGAs, FPGAs and Xilinx HardWire gate arrays, or traditional mask-programmed ASICs. The Xilinx ASIC Estimator operates on IBM-compatible computers and allows you to enter your own specific costs. Download it via the Internet at <ftp://www.xilinx.com/pub/utilities>. The directory contains a `readme.est` file and the executable `estimate.exe`. You may also contact your local Xilinx sales representative for a floppy disk copy. ♦

FINANCIAL REPORT

Record Revenue in Fiscal Year 1995

Xilinx again achieved record revenues in fiscal year 1995 (April 1994-March 1995), reflecting the strength of our product line and the continued expansion of the programmable logic market. Fiscal 1995 revenues totaled \$355.1 million, an increase of 38 percent over fiscal 1994.

For the fourth quarter (ending March 31, 1995), revenues reached a record \$109.2 million, an increase of 45 percent from the same quarter one year earlier and up 20 percent from the immediately preceding quarter. This revenue growth was driven by continued demand for the high-speed XC3100, XC3100A and richly-featured XC4000 FPGA families, along with record revenues for custom HardWire devices. Inter-

national revenues increased 49 percent from the preceding quarter, contributing more than 30 percent of total revenues.

"Xilinx is well-positioned as we enter fiscal 1996. We intend to double our number of architecture offerings and, with the NeoCAD union, we will be able to provide more powerful software solutions," noted Bernie Vonderschmitt, Xilinx CEO. "Looking forward, we remain optimistic about the overall growth of the high-density programmable logic market and our position within this market."

Xilinx stock is traded on the NASDAQ exchange under stock symbol XLNX. ♦