

Full-Featured Floorplanner Boosts FPGA Performance

The new XACTstep, version 6 release contains the industry's first graphics-based hierarchical floorplanner. Use of XACT-Floorplanner can result in dramatic improvement to FPGA performance, allowing designs to run at higher speed, or providing cost-savings by allowing the use of a slower speed grade device.

Floorplanning is particularly effective for designs that have a high degree of structure or a large gate density. Floorplanning can help optimize the use of special FPGA features such as the high-speed distributed RAM capability of the XC4000 FPGA family.

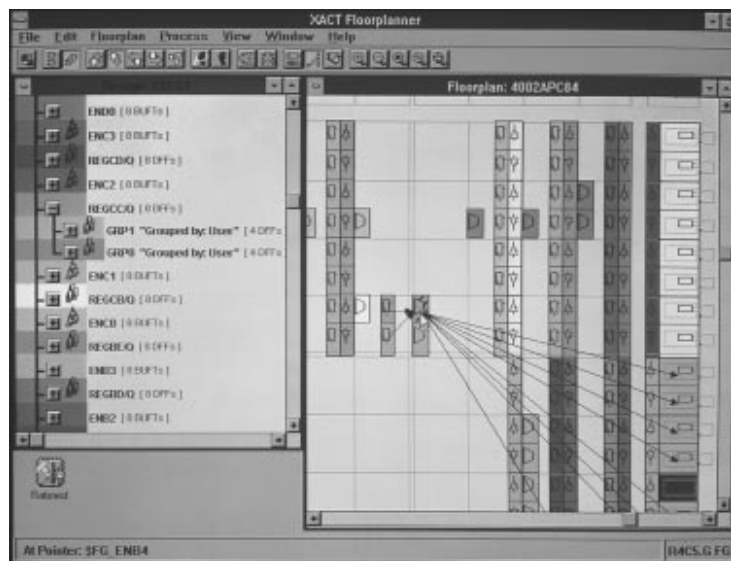
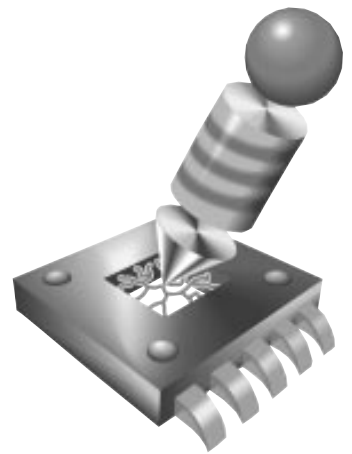
The Floorplanner features a "drag-and-drop" methodology that makes it easy to learn and use. A basic floorplan is created by dragging logic elements from the design and dropping them into locations on a picture of the die. Critically-timed logic can be pre-placed, and overall data flow can be planned. More-detailed floorplans allow the use of proven optimization techniques such as bus interleaving, register grouping and I/O pin alignment.

Many powerful features aid the designer. Users start with a **graphical view** of the designs' hierarchy. Each level of hierarchy is labeled with the original symbol from the schematic or hardware description language description, and is marked with the exact number of required FPGA resources. This view of the hierarchy can be enlarged or reduced to view any level of the design. A search and find utility makes it easy to locate specific logic elements.

When a logic element is "dropped" onto the die, the Floorplanner creates a "ratsnest" view of all its interconnections to previously-placed elements. Logic elements can be assigned to an area of the device so that the automatic "place and

route" tools can then find an optimal placement of that logic within that area. For elements encompassing multiple FPGA resources, the Floorplanner can be directed easily to distribute the elements horizontally or vertically. Thus, logic structures can be aligned to use long line routing and internal three-state buffers efficiently.

For more-detailed floorplans, powerful commands make it easy to align or inter-



leave busses or structured logic elements. Users re-order bits by simply changing the sort order. Complex alignments can be carried out by placing each bit separately.

Once the floorplanner finds the optimal placement for a given logic structure, it can be captured to a **Placement Map** and imposed on similar structures in the design — making it easy to "tile" repeated logic, or re-use portions of a design in future projects.

After completing the floorplan, commands are available to help analyze its efficiency. These commands also can be used to analyze a layout created by the automatic tools.

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Cadence Interface Now Available from Xilinx

“This reflects our continuing commitment to make top-down design methodologies more accessible to Xilinx users.”

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The interface software for linking the Cadence design tools to the Xilinx XACT-Development™ system, including Verilog libraries, can now be purchased directly from Xilinx. Support contracts also are available. This reflects our continuing commitment to make top-down design methodologies more accessible to Xilinx users. These interfaces and libraries are developed by Cadence and require Cadence licenses (except for ES-Verilog). There are several product configurations, as described below:

ES-Verilog (No Charge)

This package includes the Verilog simulation models and XNF2Verilog translator. Interested users who have an in-warranty DS-502 or any “standard package” on workstations can request ES-Verilog directly through Xilinx customer service.

DS-381-SN2 (or HP7)-C

This product includes:

- Concept and Composer schematic symbols
- Verilog-XL and RapidSIM simulation models
- Netlist translators for these Cadence schematic editors and simulators

The software and documentation for the DS-381 package is already included on the Cadence compact disk that holds the other Cadence products (CD “9404” or

later). Therefore, immediate access to DS-381 is available upon purchasing the license to enable it — nothing is shipped to the purchaser. *Please contact your local Xilinx sales representative for more information on how to order this license.*

DS-CDN-STD-SN2 (or HP7)-C

This product includes:

- DS-381 package (as described above)
- Xilinx 3PA package (the core implementation tools for Xilinx FPGAs and EPLDs, including X-BLOX)

Because users already have the DS-381 software and on-line documentation on their Cadence CD, only the 3PA package will be shipped after purchase. *Please contact your local Xilinx representative for information on how to order this package.*

DS-381 Product Evaluation

Any Cadence user with a “9404” or later CD can evaluate Xilinx software for 90 days by requesting a 90 day temporary license from your local Xilinx sales office.

Maintenance Contracts

Cadence customers can now move their support contract for the Cadence interface software to Xilinx by purchasing the SC-381 or SC-CDN-STD support packages. However, no updates are planned until the next release of the XACT® tools (XACTstep, version 6); it is recommended that users maintain their Cadence maintenance contract until then. ♦

Floorplanner

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The **Check Floorplan** command verifies resource allocation, three-state buffer alignment and CLB packing. If errors or warnings are found, a dialog box is used to

navigate to the problem spot with a single click of the mouse. For more-detailed analysis, ratsnest views can be generated for any resource, along with routing congestion maps for any CLB(s).

Whether the design requires a few minutes of basic floorplanning or a detailed analysis and optimization, the Floorplanner can provide a tremendous boost in designer productivity and signifi-

cant improvements in FPGA performance and density.

The Floorplanner can be used for XC3000A, XC3100A, XC4000, and XC5000 FPGA designs. Registered XACT development system owners with active software maintenance agreements will receive the Floorplanner in the XACTstep, version 6 update targeted for August shipment. ♦