



## XC4000-Series FPGAs: The Best Choice for Delivering Logic Cores

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Application Brief

### Summary

Reusable logic cores provide an efficient means of embedding common logic functions in high-density FPGA designs. The rich feature set of the XC4000-Series FPGA devices makes them the ideal choice for core-based system design.

### Xilinx Family

XC4000E, XC4000EX, XC4000XL

## Introduction

Reusable designs, called logic cores, have been available to designers using traditional mask-programmed gate arrays for several years. Typically, these cores are pre-designed, pre-tested implementations of widely-used system functions that can be “dropped” into a design and integrated with the application-specific functions of that design. Examples of functions commonly available as cores (also referred to as “drop-in modules”) include bus interfaces, microcontrollers, and DSP functions such as digital filters. The use of such pre-designed modules accelerates time-to-market and allows the designer to focus his or her time and resources on the system’s unique functions.

Now that Field Programmable Gate Arrays (FPGAs) have reached usable densities in the tens of thousands of gates, FPGAs have become an ideal “platform” for the development and use of logic cores and other intellectual property. Specifically, the Xilinx XC4000-Series FPGAs, consisting of the XC4000E, XC4000EX and XC4000XL family devices, deliver the best combination of performance, density, features, and flexibility to support the use of cores in high-density FPGA design.

Today’s designer can select from a variety of high-density FPGA devices and architectures. However, the successful implementation of system-level designs requires much more than just “raw gates”. The FPGA architecture must include the system-integration features that allow the efficient integration of pre-defined cores and application-specific functions. The XC4000-Series is unique in its incorporation of so many of the features required for the successful implementation and use of logic cores.

## XC4000-Series Product Features

### Scaleable, Broad Product Family

The XC4000-Series is the world’s most-popular and the industry’s broadest FPGA family. Its scalable architecture and design software provide system solutions ranging from 3,000 gates up to 62,000 gates and beyond, offering the ultimate in design flexibility. An XC4000-based logic core can be integrated with the user’s application and migrated

between a wide range of devices, providing the right solution for the design.

### Advanced Packaging, Footprint-Compatibility

The XC4000-Series devices are available in a wide variety of packaging options, including pin grid array, ball grid array, quad flat pack, and thin quad flat pack. Furthermore, there is footprint-compatibility between various XC4000 device densities in the same package plus compatibility with other Xilinx logic technologies.

### Pinout Stability

Often, the design and procurement of the printed circuit board (PCB) is in the critical path for completion of a system design. Thus, designers prefer to fix the pinout of their FPGAs early in the design cycle and maintain that pinout configuration during subsequent design iterations.

The XC4000-Series devices have extra interconnect around the periphery of the device to enhance pinout stability between design revisions. In contrast, other FPGAs can become “unroutable” as a result of even small design changes if the pinouts are locked in place.

### High Quality

XC4000-Series FPGAs are 100%-tested standard products manufactured in high volumes with significantly higher quality than that achievable in most ASIC designs.

### Proven Risk-Free Cost-Reduction Path

For high-volume applications, a thoroughly system-verified FPGA design can be cost-reduced using Xilinx HardWire technology. The HardWire conversion process offers risk-free 100% pin- and function-compatibility with the equivalent FPGA device, preserving the same PC board. Plus, thorough test vectors are generated automatically, saving the engineer from creating complex simulation files. With HardWire technology, the engineer needs to design the

system only once. There is no need to redesign specifically for another technology.

## **XC4000 Architectural Features**

The XC4000-Series silicon provides more than just gates and flip-flops—it provides a system-level solution. The following represent unique XC4000 FPGA features.

### **Flexible Clocking**

Clock structures are important, especially in high-density designs. The XC4000-Series offers up to eight dedicated low-skew, high fan-out clock distribution networks. Any, or all, of the flip-flops can be driven from one of these networks.

However, some applications require more than eight clocks. Each XC4000-Series logic block clock input can be driven by an individual clock signal, allowing literally hundreds of clocks in a single design.

### **Advanced On-Chip RAM (and ROM)**

Many systems require RAM memory, either as standard read/write memory or as FIFOs. XC4000-Series FPGAs provide ample distributed RAM to build small blocks of efficient storage on-chip. On-chip RAM results in better integration and improved system performance.

The XC4000-Series RAM is included in every logic block. Larger memory arrays are built by connecting multiple logic blocks together. Each memory array optimally uses the available device resources. In contrast, FPGAs with large dedicated RAM blocks often suffer from poor efficiency. Not every design uses all of the RAM available in a large block.

Xilinx was first to provide on-chip RAM in a programmable logic device. Since then, other vendors have followed, but do not offer the XC4000's advanced RAM features. XC4000-Series RAM supports true dual-port access, providing superior performance in FIFO and data buffering applications.

The XC4000 software provides a memory compiler to quickly and easily build large RAM arrays. Plus, the memory compiler can also build ROM structures for implementing control stores, system configuration information, or state machine code.

### **Internal Bi-Directional Bussing**

Most system-level designs contain a bi-directional data bus. Consequently, the XC4000-Series provides an efficient internal bussing structure for optimal bi-directional data flow within the device. In other FPGA technologies, busses must be re-implemented using multiplexers. Buses implemented using multiplexers consume more resources, resulting in slower system performance.

## **Numerous and Flexible Output Enables**

Large system designs typically require bi-directional I/O. These three-state outputs are controlled by an output-enable signal. The XC4000-Series FPGAs provide up to one output-enable per I/O for maximum flexibility. These output-enables are plentiful and operate independently of the clock resources. A Global Three-State forces all outputs to high-impedance for test purposes or for power-on reset functions.

### **Definable Power-Up State**

In many applications, the power-up state of the design is important. Enable lines must be held disabled until the remainder of the system is functioning. Counters must power-up in a known state.

The XC4000-Series FPGAs automatically initialize all of the device flip-flops to a specified state on power-up or after a Global Reset. Each flip-flop can be individually programmed to power-up in the set or reset state.

Furthermore, each of the XC4000 I/O pins can be configured with either a pull-up or pull-down resistor, holding them at a pre-determined logic level until driven.

### **Built-in JTAG Support**

JTAG (IEEE 1148.1) test logic is an important consideration for high-density system designs, especially when using aggressive surface-mount technology like Ball Grid Arrays. The XC4000-Series FPGAs have JTAG support built into every device. No additional logic is required.

### **Reprogrammable**

XC4000 FPGAs are infinitely reprogrammable—even in system. Design modifications can be made quickly and easily, without throwing away devices. A design in the field can even be enhanced with new features or design updates.

## **XC4000 Design Software**

Successfully implementing a design requires more than just silicon. Design software is an important consideration in any logic design. Most FPGA development systems include flashy graphical interfaces and are available on multiple platforms. The XC4000-Series software goes the next step and provides a complete design solution.

### **Links to Popular EDA Tools**

The Xilinx design software supports an open-system philosophy. The majority of the world's EDA vendors—such as Mentor Graphics, Cadence, Synopsys, VIEWlogic, Aldec, Data I/O, etc.—have design entry or simulation interfaces supporting the XC4000-Series.

## Predictable, User-Specified Performance Using XACT—Performance

The XC4000-Series FPGA family offers predictable system-level performance while maintaining a flexible device architecture. Other vendors claim predictable performance by locking designers into an overly-restrictive routing architecture.

System-level predictability depends on path analysis, evaluating the time spent in multiple layers of logic blocks and interconnect. Other vendors view predictability as knowing the precise delay of a portion of the path, implemented in silicon. The user cannot specify system-level requirements.

In contrast, the XC4000-Series software provides system-level predictability by allowing the designer to specify the required performance. The XC4000-Series timing-driven place and route software meets or exceeds this requirement, or it reports any missed paths.

## Control Over Placement and Routing

The XC4000-Series software also provides ultimate control over placement and routing of logic on the device. This can be done via various methods.

At the design entry level, the engineer can specify how logic is mapped into logic blocks and where it is placed on the device. Using the XC4000 Floorplanner tool, the designer can also specify partitioning and placement in an interactive, graphical environment.

Ultimate control is offered using “guide” files. A guide file contains all or a critical portion of a design, indicating its placement and routing. With a guide file, a designer can make small modifications or include large additions to an existing design and the software maintains the placement and routing of any unchanged portions. This feature has proved crucial in designs with aggressive critical timing paths. It guarantees repeatability between design revisions.

## Powerful, In-System Verification Tools

Like most ASIC environments, the XC4000-Series design software supports functional and timing simulation plus static timing analysis. However, the XC4000 design environment supports powerful unique, in-system debugging tools. Simulation and static timing analysis demonstrates what happens worst-case. In-system debugging demonstrates what happens in the real system with all of the other components and with the system application software—a

condition nearly impossible to reproduce in a pure simulation environment.

Using the XChecker pod, a designer can download a design into the target system. With XChecker and the Hardware Debugger software, the designer can single-step or burst the system clock, readback the contents of the FPGA’s flip-flops, and plot waveforms of the results.

Additionally, because the XC4000-Series FPGAs are in-system programmable, internal nodes can be viewed dynamically by routing them to unused I/O pins.

## Proven Solution

The hardware and software features discussed above make for a good message. However, theory must be demonstrated in practice before these features have any bearing in reality.

Xilinx has proven that the XC4000-Series FPGAs is an ideal delivery vehicle for logic cores and other intellectual design property. For example, the Xilinx LogiCore PCI Interface is implemented using a Xilinx XC4013E-2 FPGA. It provides a full PCI Target/Initiator interface with about 6,000 gates of programmable logic for the user’s application. The LogiCore PCI Interface uses nearly all of the features described earlier. PCI implementations are difficult, even in ASICs. It is extremely difficult to implement in programmable logic without the XC4000’s system-level and software features.

## Support

### LogiCore Alliance Program

To encourage a growing business for intellectual property providers targeting the XC4000-Series, Xilinx formed the LogiCore Alliance program. The LogiCore Alliance program provides a conduit to help intellectual property providers offer verified design solutions to the industry’s largest installed programmable logic user base.

### World-Class Technical Support

A working design takes more than silicon and software. It sometime takes support, too. Xilinx is committed to providing world-class technical support through its world-wide network of expert field applications engineers, telephone hotline support engineers, World-Wide Web and E-mail links, design center, and training classes.

Table 1: Feature Comparison of High-Density FPGA Families

| Capability                              | Xilinx XC4000 | FLEX 8000 | FLEX 10K | ORCA |
|---|---------------|-----------|----------|------|
| Scaleable, broad product family         | Best          | Good      | Good     | Good |
| Advanced packaging                      | Best          | Good      | Good     | Good |
| Footprint compatibility                 | Best          | Poor      | Poor     | Good |
| Pin-locking stability                   | Best          | Poor      | Poor     | Good |
| On-chip RAM                             | Best          | N/A       | Good     | Good |
| Internal bi-directional bussing         | Best          | N/A       | N/A      | Best |
| Flexible clocking                       | Best          | Poor      | Poor     | Good |
| Definable power-up state                | Best          | Poor      | Poor     | Good |
| Numerous, flexible output enables       | Best          | Poor      | Good     | Best |
| Built-in JTAG support                   | Best          | Poor      | Good     | Best |
| Proven, risk-free cost-reduction path   | Best          | Poor      | Poor     | Good |
| Links to popular EDA tools              | Best          | Good      | Good     | Good |
| Predictable, user-specified performance | Best          | Poor      | Poor     | Good |
| Control over placement and routing      | Best          | Poor      | Poor     | Good |
| Powerful, in-system verification tools  | Best          | Poor      | Poor     | Poor |

Note: Best = Best in category



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