



## XC4000E Select-RAM™: Maximum Configurability

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Application Brief

### Summary

XC4000E Select-RAM™: Maximum Configurability

### Xilinx Family

XC4000E/EX

## Introduction

Configuring FPGA Memory for various design specific needs is a key requirement. Xilinx XC4000E/EX offer a wide variety of configuration options from Address and Data width to Dual-Port operation. Detailed analysis shows that Select-RAM is the most silicon efficient implementation for FPGA memory. Due to the Dual-Port RAM capability it also offers maximum bandwidth for most applications.

In contrast the Altera FLEX 10K memory can be used efficiently only for a few of the configurations. Also, any implementation requiring FIFOs or Dual-Port operation slows down the FLEX 10K memory drastically since it requires emulation of Dual-Port operation.

## Maximum Configuration Flexibility

The new XC4000E CLB can be used as 16X2 or 32X1 memory element. These memory elements can then be cascaded together to form larger memories with various Address and Data options.

Altera's large 2K bit memory blocks are wasteful because all of the memory within a block, is seldom utilized. **Table 1** shows a broad range of desirable memory configurations. It then shows the number of EABs used for different memory configurations. It also shows the %utilization of FLEX 10K

EAB memory for those configurations. A percentage EAB memory utilization at or below 50% is inefficient use of device silicon.

**Table 1** also shows FLEX 10K10 with three EABs can efficiently implement only five of the popular memory configurations. Similarly 10K20 and 10K 30 with six EABs can efficiently implement only four possible configurations. Finally, 10K40, 10K50, 10K70 and 10K100 can efficiently implement five possible configurations.

## Dual-Port Access

FPGA designs frequently implement large FIFOs/RAM Buffers especially in Datacomm and DSP intensive areas. Most FIFO/RAM Buffer functions require Dual Port RAMs along with fast speed. The Xilinx XC4000E Select-RAM now offers Dual-Port RAMs with independent access from both sides.

The Altera FLEX 10K requires emulating dual-port RAM which cuts down the available memory size and speed in half! This makes a 20ns memory operate on certain key timings at a slow 40ns speed, eliminating a number of fast speed applications.

**Table 1: FLEX 10K Memory Implementation: Number of EABs (% EAB Memory Utilization)**

		Memory Width					
		4	8	16	32	64	
Memory Depth	8	1(2%)	1(3%)	2(3%)	4(3%)	8(3%)	10K10 = 3
	16	1(3%)	1(6%)	2(6%)	4(6%)	8(6%)	
	32	1(6%)	1(13%)	2(13%)	4(13%)	8(13%)	10K20 = 6 10K30 = 6
	64	1(13%)	1(25%)	2(25%)	4(25%)	8(25%)	
	128	1(25%)	1(50%)	2(50%)	4(50%)	8(50%)	10K40 = 8 10K50 = 10 10K70 = 9 10K100 = 12
	256	1(50%)	1(100%)	2(100%)	4(100%)	8(100%)	
	512	1(100%)	2	4	8		
	1024	2	4	8			
	2048	4	8		Exceeds 10K Family Limit		
	4096	8					

## Routing Impact On Performance

Due to the limitations of FLEX 10K column interconnects almost all wide signals use the slowest interconnect path in Altera FLEX devices. For any memory width the device implementation in MAX+PLUS II toolset used the slow row-column-row delay path for addresses, data-in and data-out. This addition delay occurs twice once in address path and second time in the data path for each memory access. This slows down the effective memory access time by additional 5 ns.

## Performance

The performance of the XC4000E RAM is superior to the FLEX 10K in a wide variety of sizes and configurations. As shown in Table 2, when configured as single port memory, the Xilinx RAM out performs the Altera memory in the commonly needed scratch pad RAM sizes of 8 to 32 bits deep by 4 to 64 bits wide. Table 3 further shows that the Xilinx XC4000E true dual port memory consistently out performs the Altera FLEX 10K emulated dual port memory.

**Table 2: Xilinx 4KE vs. FLEX 10K Single Port RAM Performance (ns)**

		Memory Width									
		4		8		16		32		64	
Memory Depth		Xilinx	Altera	Xilinx	Altera	Xilinx	Altera	Xilinx	Altera	Xilinx	Altera
	8	13.9	21.6	17.4	21.6	19.5	21.6	21.6	36.5	34.7	36.8
	16	17.6	21.6	16.8	21.6	20	24.7	29.5	36.5	29.8	36.8
	32	19.7	21.6	21.8	21.6	24	25.5	32	36.5		
	64	22.6	21.6	25.1	24.2	31.7	24.7				

**Table 3: Xilinx 4KE vs. FLEX 10K Dual Port RAM Performance (MHz)**

		Memory Width							
		4		8		16		32	
Memory Depth		Xilinx	Altera	Xilinx	Altera	Xilinx	Altera	Xilinx	Altera
	16	115.3	27.62	102.6	27.62	80.4	26.04	54.2	23.47
	32	79.5	27.62	76.6	27.62	58.9	27.62	48	23.26
	64	81.7	25.13	67.1	26.04	62.7	26.18	37.1	23.81
	128	55.7	26.04	52.3	26.04	47.1	27.62	32.5	25.51
	256	43.5	28.09	38.7	26.04				
	512	33.2	27.62						



The Programmable Logic Company<sup>SM</sup>

### Headquarters

Xilinx, Inc.  
2100 Logic Drive  
San Jose, CA 95124  
U.S.A.

Tel: 1 (800) 255-7778  
or 1 (408) 559-7778  
Fax: 1 (800) 559-7114

Net: hotline@xilinx.com  
Web: http://www.xilinx.com

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