



File Download: sw_cadence

Contents of /ftp/swhelp/cadence

Files/Patches/Information on the Xilinx-Cadence Interface

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Filename	Size	File Description
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vconfig.tar	20KB	Two-part patch for Verilog-XL v2.1.2 to fix core dump problem when +neg_tchk option is specified. The two archives are needed to compile a configurable version of Verilog-XL (one that can be linked to PLI routines).
verilogt.z	4044KB	
vlogintd.ps	172KB	Full documentation for ES-VERILOG v5.2.0 Interface to Verilog-XL (PostScript fo For SunOS 4.x
vlogihp7.tar	883KB	ES-Verilog interface for 2K, 3K, 4K, 4KE, 5K and 7K architecturess from XACTstep Core Tools v5.2.1 for work- stations--(HP7)
vlogisun.tar	1043KB	ES-Verilog interface for 2K, 3K, 4K, 4KE, 5K and 7K architectures from XACTstep Core Tools v5.2.1 for work- stations--(Sun4)
pre5cds3.pdf	37 kB	Application note describing workarounds for using the pre- Unified / pre-9404 Cadence Concept and Composer libraries and interface with XACT 5.x. Solution #: 1716 For All Platforms Uploaded: 03-13-97