



File Download: docs_tutorials_modules

Contents of /ftp/doc/tut_modules

Note In order to use any of these modules you will first need to install any of the tutorial interfaces found in /ftp/doc/tut. Please read the enclosed readme.txt files for installation instructions.

Filename	Size	File Description
aldeptut.zip	495KB	Tutorial for using the Foundation design entry software (Schematic and Symbol entry, Simulation, more) For all Xilinx families.
cdmtutor.zip	340KB	Tutorial for the XACT-CPLD Design Manager Interface. (XC9500 family)
ceztutor.zip	405KB	Tutorial for the XACT-CPLD EZTAG 9500 downloading software.
cfetutor.zip	165KB	Tutorial for the XACT-CPLD Flow Engine interface. (XC9500 family)
ctatutor.zip	417KB	Tutorial for the XACT-CPLD Timing Analyzer interface. (XC9500 family)
dmtutor.zip	336KB	Tutorial for using the XACT-Step Design Manager interface. (XC2000, XC3000, XC4000, XC5200 and XC7000 families)
fetutor.zip	165KB	Tutorial for using the XACT-Step Flow Engine interface. (XC2000, XC3000, XC4000, XC5200 and XC7000 families)
fptutor.zip	1,058KB	Tutorial for using the XACT-Step Floorplanner interface. (XC3000, XC4000, XC5200 families)
hddg.zip	703KB	Tutorial for High Density Design Methodologies using FPGAs.
hdtutor.zip	394KB	Tutorial for using the XACT-Step Hardware Debugger to program Xilinx FPGAs.
pftutor.zip	379KB	Tutorial for using the XACT-Step

tatutor.zip	417KB	PROM File Formatter to create PROM files from FPGA bit streams. Tutorial for using the XACT-Step Timing Analyzer to find the timing performance of your Xilinx design. (XC3000, XC4000, XC5200 and XC7000 families)
tbook.zip	435KB	Tutorial for using the XABEL-CPLD Software for the XC7000 and XC9500 families.