



File Download: app_3rdparty

Contents of /ftp/apps/3rdparty

Applications Relating to Third Party interfaces

Filename	Size	File Description
----------	------	------------------

xsiverlg.tar	2974KB	Verilog design examples for "HDL Synthesis FPGAs". tar -xf to extract.
vstbsim.zip	195KB	Board-level simulation with OrCAD VST v1.20