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FOR IMMEDIATE RELEASE

**NEW XILINX SEA-OF-GATE FPGA FAMILY EXPLOITS
INNOVATIVE MicroVia™ TECHNOLOGY**

*Fine-Grained, Programmable-Cell Architecture Delivers Highly Predictable,
Near-100 percent Gate Utilization*

SAN JOSE, Calif., September 11, 1995—Xilinx, Inc., (NASDAQ:XLNX) today unveiled the XC8100 family, a new family of field programmable gate arrays (FPGAs) based on the company's innovative MicroVia antifuse technology and proprietary sea-of-gates (SOG) architecture. Employing a fine-grained, programmable-cell structure and extensive routing resources, the XC8100 family was developed for high gate efficiency and ease-of-use. Using top-down design methods with the synthesis-targeted XC8100 FPGAs, designers can achieve near 100 percent gate utilization and high routability across all application areas.

Developed with an extensible architecture that delivers high gate capacities, initial members of the XC8100 family include four devices that span 1,000 to 9,000 usable gates. To date, the XC8100 family is covered by eight U.S. patents issued in the areas of process and device architecture.

“Synthesis isn't being used just for gate arrays,” said Lee Farrell, vice president and program manager for the XC8100 device cross functional team at Xilinx. “More and more customers are using synthesis—either completely or in conjunction with schematics—for programmable logic. XC8100 sea-of-gates, antifuse-based FPGAs have

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been architected and optimized from the ground up for synthesis users,” he added. According to Farrell, the XC8100 device represents a significant departure from traditional FPGA architectures with its programmable cell and SOG, over-the-cell antifuse routing.

MicroVia Process

The XC8100 family is the industry's first FPGA to utilize the metal-to-metal MicroVia antifuse and three layers of metal. Within the XC8100 family devices, the MicroVia antifuse programming element is stacked on the upper layers of a 0.6 micron, three-layer-metal (TLM) CMOS process. All routing resources are located above the underlying gate logic, bolstering silicon efficiency. The interconnects are programmed for high-speed operation using the MicroVia antifuses, which have a typical on-resistance of less than 50 ohms. The result is an FPGA family that combines very extensive routing with a small die, thereby breaking a traditional trade-off in programmable logic devices (PLDs). And despite the extensive routability, it delivers a die size one half the size of competitive FPGAs.

According to Erich Goetting, R&D director for the program, the XC8100 family is being introduced following a four-year effort by Xilinx to investigate the viability of antifuses as programming elements for FPGAs. “To be successful,” he stated, “antifuses needed the combination of a metal-to-metal fuse element and three layers of metal. Existing antifuse-based FPGAs will have trouble keeping up with this technology.”

New Architecture Features

Key to the XC8100 family's high-gate utilization for any type of circuit or design methodology is the unique Configurable Logic Cell (CLC), which can implement synchronous, combinatorial and three-state logic functions. While existing antifuse FPGA architectures have fixed-cell structures with only programmable interconnects, the XC8100 device's CLC uses MicroVia antifuses to configure SRAM elements within the cell to automatically optimize the CLC configuration. Thus, the type of function

implemented within the programmable CLC is dependent on the type of logic to be implemented, as dictated by the input netlist. Xilinx XC8100 devices can be 100 percent utilized for any type of logic, allowing the designer to achieve all the gate capacity available within the device, even when designing with high-level synthesis-based netlists.

Compared to existing Xilinx FPGAs, the XC8100 architecture has many more cells, each with fewer gates. Each CLC structure represents approximately 3.25 gates. The regular, simple XC8100 architecture also has a very large ratio of interconnects to logic cell inputs and outputs as compared to existing FPGA families. The XC8100 family's abundant routing resources allow users to configure their FPGA without knowledge of the underlying architecture, thus remaining at the HDL level when designing the system.

Additional device features include:

- Low-power CMOS
- 5 V and 3.3 V operation
- Pin compatibility with existing Xilinx FPGAs
- Extensive on-chip test circuitry for 100 percent testability
- On-chip logging of version, programming algorithm
- Flexible buffers for clocks and/or data; drive any cell input
- 24 mA outputs
- Design security
- JTAG boundary scan

XACTstep Series 8000 Software

The XC8100 family was developed in parallel with new software tools that could exploit the advantages of the device architecture. The resulting Series 8000 development system software provides XC8100 customers with an ASIC-like design flow. Designs can be entered and simulated with third-party CAE tools and then placed and routed by Xilinx Series 8000 tools.

Unique features embedded within the new Series 8000 software include PowerMaze™, PowerGuide™ and TrueMap™. PowerMaze is a new high-speed router that can route thousands of gates per second. The tool includes rip-up-and-retry capability. PowerGuide, meanwhile, provides users with an incremental design capability in a synthesis environment. But unlike typical incremental design software, Xilinx uses a novel approach with the XC8100 family. By matching circuitry based on topology and not names, designers can maintain original timing and design information, which might otherwise be changed by successive synthesis runs. Xilinx TrueMap logic mapping provides a key feature to synthesis-based design flows. With TrueMap, all input nets, instance names and hierarchy in an EDIF netlist are maintained through the Series 8000 back-end tools, thus preserving the information for back annotation, simulation and debugging.

According to Xilinx customers, early evaluations of the XC8100 devices are underscoring the value of the new FPGA family. “Technology-independent design using VHDL is a priority at Northern Telecom,” said William Smith, principal engineer at Northern Telecom, Ireland. “The fine-grained XC8100 devices and Series 8000 software let our engineers harness the power of high-level design while maintaining technology independence.” Alan Jamieson, a senior design engineer also with Northern Telecom elaborates, “Series 8000 software has a very short learning curve and fits the Synopsys design flow extremely well. By using ‘fast’ design approaches and extensive hierarchical floorplanning, I was able to get my telecom application to run at 52 MHz in an XC8106 device.”

Additional Series 8000 development system features include Xilinx unified design-entry libraries, high-level floorplanning support and patented algorithms that perform both programming and testing of XC8100 antifuses. In fact, the Series 8000 software implements unique post-programming net verification, providing 100 percent

post-programming yield. These capabilities, along with complete on-chip JTAG support, ensure that XC8100 devices are completely testable.

The initial XC8100 product line includes four devices:

	XC8101	XC8103	XC8106	XC8109
Usable gates	1248	3328	5616	8700
I/O	80	128	168	208
Production	Now	Now	Now	4Q95

Pricing for the XC8106 device is \$85.10 each in 100-piece quantities. Volume pricing, by the second half of 1996, will be less than \$30 each. Depending on options, the Series 8000 software sells for about \$2000 for the PC versions. Existing Xilinx users with maintenance pay about \$1000. Other platforms supported include the Sun Sparc and HP 700 Series platforms. Initial CAE interfaces include most synthesis tools, with schematics to follow in the fourth quarter.

Founded in 1984, Xilinx is the world's largest supplier in the CMOS programmable logic industry. The company pioneered the market for field programmable gate array (FPGA) semiconductor devices that provide high integration and quick time-to-volume for electronic equipment manufacturers in the computer peripherals, telecommunications, industrial control, instrumentation, and military markets. Headquartered in San Jose, Calif., the company produces innovative device architectures and enabling electronic design automation software.

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