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**Xilinx FastFLASH™ Innovation Delivers Industry's Most Complete Solution  
for In-System Programmable CPLDs**

*XC9500 Family Uses Industry's First 5 volt Flash Technology for CPLDs*

SAN JOSE, Calif., October 23, 1995—Xilinx, Inc., (NASDAQ:XLNX), the leader in the programmable logic industry, announced today the XC9500 family of complex programmable logic devices (CPLDs) in five volt flash technology. The new family, based on an innovative FastFLASH™ technology, affords the user superior in-system programmable (ISP) capabilities by offering more than 10,000 program/erase cycles—as much as 100 times higher endurance than other comparable CPLDs. This enables the XC9500 devices to be used in applications requiring more frequent field upgrades, such as telecom and industrial control. In addition, this new product delivers unequaled pin-locking capability for design and reconfiguration, and enhanced in-system test, programming, and manufacturing capabilities using the industry-standard IEEE 1149.1 (JTAG) interface. These capabilities make the XC9500 CPLD family the industry's best solution for addressing the user's needs throughout the entire product life cycle: design, system integration, volume manufacturing, and field upgrades.

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The XC9500 family sustains Xilinx's reputation for high performance by offering pin-to-pin delays as fast as five nanoseconds. The initial nine member family ranges in density from 800 to 12,800 gates.

### **FastFLASH: The Enabling Technology**

Xilinx's FastFLASH process technology is the first 5V flash technology optimized for high-performance in-system programmable CPLDs. Jointly developed by Xilinx and technology partner Seiko-Epson (Fujimi, Japan), the 0.6 micron double-poly, double-metal flash process provides an industry-leading 10,000 reprogramming cycles. The capability for three to four times as many programmable routing switches in the same die area as EEPROM technology is available, resulting in superior routing for improved pin-locking support.

FastFLASH technology is compatible with the industry-leading flash memory processes and is optimized for high-performance logic. The FastFLASH programmable cell was specially developed to provide high-speed switching performance as well as built-in erase control to simplify on-chip programming and erase.

"The result is a high yielding, high-performance CPLD technology with enhanced endurance compared with existing EEPROM technologies," said Nick Kucharewski, vice president and general manager of the CPLD division. "This technology will drive the market acceptance level of in-system programmability to significantly higher levels than originally projected with the first generation products. In addition, a cell size which is one-third the area of comparable

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EEPROM-based CPLD cells affords increased performance and density,” Kucharewski added.

### **Flexible Full-Featured Architecture**

Key to this CPLD family is its industry-leading pin-locking capability. The XC9500 device incorporates the three critical elements necessary for optimal pin-locking:

- 1) 100 percent interconnect of all pins and function block outputs to function block inputs with the FastCONNECT™ switch matrix;
- 2) wide function block fan-in with 36 total inputs;
- 3) a flexible product term allocation architecture whereby any macrocell may increase its logic capacity without affecting adjacent macrocells;

All three features work together to ensure design changes will not cause the chip pinouts to change. Further, the newly developed FastCONNECT switch matrix combines the interconnect capabilities required for pin-locking with leading-edge speeds; pin-to-pin speeds are as fast as five nanoseconds.

With FastFLASH technology pin-locking, the designer saves significant costs during prototyping and system integration by eliminating additional board re-layout and rebuild. For field upgrades where design changes are unknown prior to the product shipping, the pin-locking capability will enable a system in the field to be upgraded easily without having to replace boards.

### **Enhanced JTAG**

By offering the most complete in-system test, programming, and manufacturing capabilities in the industry, the XC9500 family sets a new standard in development and manufacturing support. The XC9500 family is the only CPLD

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family to incorporate support for both USERCODE and INTEST functions within the IEEE 1149.1 standard. USERCODE allows user-specified in-system serialization of programming codes for pattern tracking and version control during manufacturing and field upgrades. The INTEST operation is useful during prototyping and systems integration, where newly programmed devices may be fully tested before connecting to the system. Integrated with the FastFLASH development software, this capability is essential in supporting rapid prototyping as well as field diagnostics and upgrades.

Other key IEEE 1149.1 instructions supported include IDCODE and HIZ, which allow device inventory control and simplified board testing. Together, the enhanced JTAG capabilities provide the best support for the development and manufacturing of the most sophisticated systems.

### **ISP Reduces Production Costs**

“With ISP capability, users can reduce overall system costs in several areas: manufacturing, field upgrades, and inventory,” said Rhondalee Rohleder, president of PACE Technologies (Scottsdale, AZ). “To date, however, users have had to choose between an EEPROM-based ISP CPLD, which may limit programming iterations, or a flash-based CPLD that is not ISP, due to high-voltage programming requirements.”

Additional savings are in shortened development and debug times, providing the best time to market opportunities, and eliminating the need for external hardware programmers.

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## Software Support

The FastFLASH CPLD family is supported by Xilinx's basic development system now called XACT<sub>step</sub><sup>™</sup>. This Windows<sup>™</sup>-based software package interfaces to popular VHDL/HDL and schematic design entry and simulation tools, providing a complete, user-friendly design environment for all Xilinx CPLDs and FPGAs. Once the design has been captured, the XACT<sub>step</sub> development and software automatically selects the proper CPLD and optimizes, partitions, and maps the design into a single device using timing constraints entered with XACT Performance.

A new module for the XACT<sub>step</sub> system that allows users to target the XC9500 family will be available at no charge to customers under maintenance contacts. Initial shipments are scheduled to begin this quarter.

## Pricing and Availability

<u>Device</u>	<u>Macrocells</u>	<u>Usable</u>	<u>Tpd</u>	<u>Registers</u>	<u>Availability</u>
		<u>Gates</u>			
XC9536	36	800	5	36	1Q96
XC9572	72	1,600	7.5	72	2Q96
XC95108	108	2,400	7.5	108	Now
XC95144	144	3,200	7.5	144	3Q96
XC95180	180	4,000	10	180	3Q96
XC95216	216	4,800	10	216	1Q96
XC95288	288	6,400	10	288	2Q96
XC95432	432	9,600	12	432	4Q96
XC95576	576	12,800	15	576	4Q96

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The XC95108 device is currently available in sample quantities, with production quantities available in 1Q96. Pricing for the XC95108-15 PQ100C device will be \$49.50 in 100+ quantities. Other members of the family will become available throughout 1996.

For more information, there are application notes and a data sheet for the XC9500 family on the Xilinx World Wide Web site. The address is listed in the Note to Editors at the end of the release.

Founded in 1984, Xilinx is the world's largest supplier in the CMOS programmable logic industry. The company pioneered the market for field programmable gate array (FPGA) semiconductor devices that provide high integration and quick time-to-volume for electronic equipment manufacturers in the computer peripherals, telecommunications, industrial control, instrumentation, and military markets. Headquartered in San Jose, Calif., the company produces innovative device architectures and enabling electronic design automation software.

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