

XACT^{step} version 6 Xilinx Development System

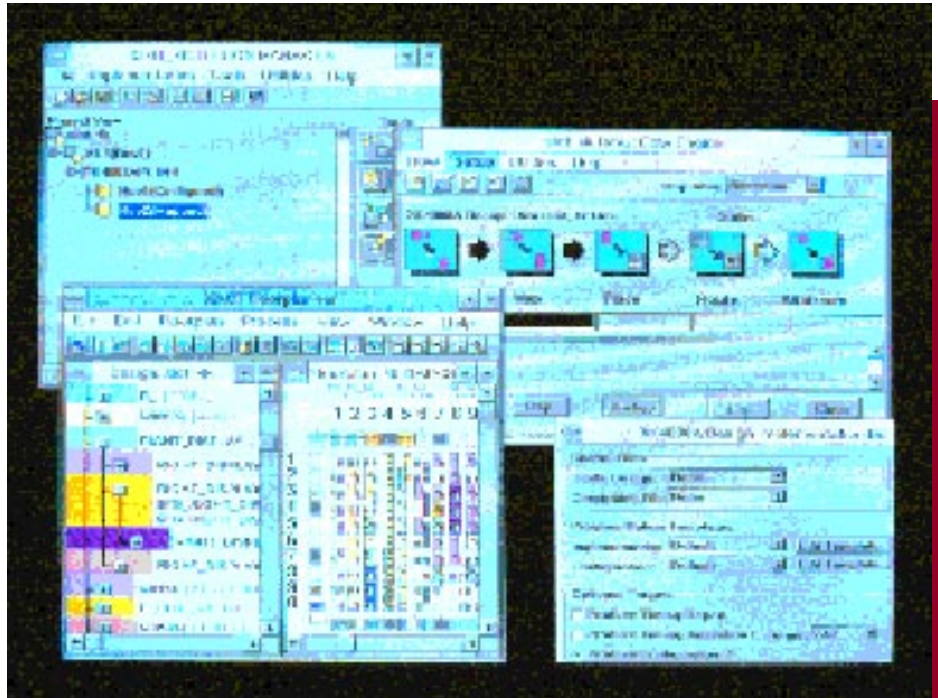


Powerful, easy-to-use tools for designing Xilinx CPLDs and FPGAs

XACT^{step}™ version 6 features a revolutionary combination of powerful tools and ease-of-use to provide accelerated learning curves, short implementation cycles and fast design debug. This high-productivity environment contains six new tools that are easily accessible through graphical tool bars, icons and pop-up menus. They support the complete spectrum of PLD designs from fully automatic to hand-crafted.

XACT^{step} v6 allows designers to use a single, integrated tool set for the industry's broadest array of PLD solutions including the XC2000, XC3000, XC3100, XC4000, XC5000 and XC7000 families. It provides technology independence and gives designers the flexibility to select target devices late in the design cycle. It also facilitates design reuse between projects.

For design entry and simulation, Xilinx supports an "open tools" approach that allows designers to use their favorite EDA tools. The entire spectrum of design methodologies are supported including schematic capture, text-based HDL and the emerging field of graphical HLDA. Xilinx's Alliance and Syndicate EDA programs insure high quality tools and accurate results.



XACT^{step} version 6 Contains Six Exciting New Tools

Flexible Design Manager

Provides version control, device retargeting and design reuse.

Configurable Flow Engine

Allows designers to easily control the implementation process.

Graphically-based Hierarchical Floorplanner

Makes it easy to achieve hand-crafted levels of performance and density. Industry first!

Interactive Timing Analyzer

Generates custom timing reports and allows 'what-if' speed grade analysis.

PROM Formatter

Simplifies device configuration and graphically creates daisy chain load sequences.

Powerful Hardware Debugger

Allows verification of configuration data and viewing of internal signals while the FPGA device is running in-circuit.



XACT^{step}

XACTstep Version 6 Key Features

All the tools in XACTstep v6 utilize a new graphical user interface (GUI) that accelerates the learning curve and boosts productivity. With this new GUI, programs are launched from tool bars and icons. Tool tips provide instant descriptions and on-line help is available for more in-depth information. Report browsers present message files with easy to understand titles and allow simultaneous viewing of multiple documents. On the PC, the GUI is fully Microsoft Windows compliant.

Design Manager

The easy-to-use *Design Manager* provides a hierarchical project management environment for a wide range of families. It manages all the underlying design files and features version control to simplify design iterations.

Using this tool, a design can be retargeted to a different device size or speed grade with the click of a button. This allows the designer to easily find the most cost effective implementation.

Flow Engine

The configurable *Flow Engine* eliminates the steep learning curve associated with FPGAs by allowing designers to control the implementation process using graphically based tools. They can choose a fully automatic flow or set break points that allow analysis and optimization of results before proceeding to the next step.

The *Flow Engine* translates a design into a bitstream that can be downloaded into an FPGA or a programming file for an EPLD. It also generates a set of files for third-party functional and timing simulators.

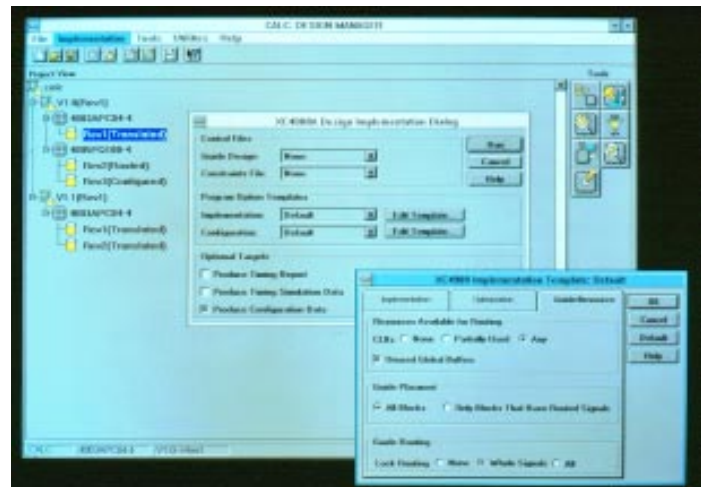
Floorplanner

The PLD industry's first graphically based hierarchical *Floorplanner* makes it easy to maximize the design's performance and density. In many cases, this tool enables the designer to use a slower speed grade or lower gate count device resulting in immediate cost savings.

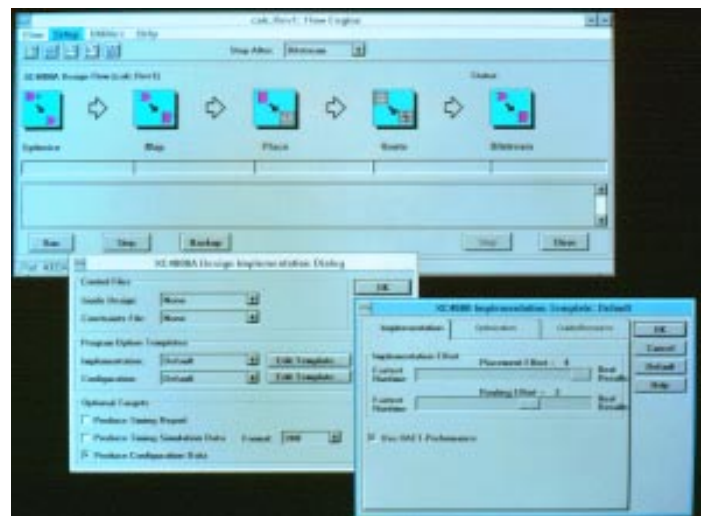
With this easy-to-use and powerful tool, designers can pass their knowledge about the design to the automatic placement and routing tools. They can interactively place structured design elements and graphically plan their data flow. The placement is done at a high level using their own design hierarchy and a floor plan of the device.

Floorplanning can be valuable for designs that have a high degree of structure or a large number of gates. It also allows optimization of structures like Xilinx's unique high-speed distributed RAM and tri-state internal bus features.

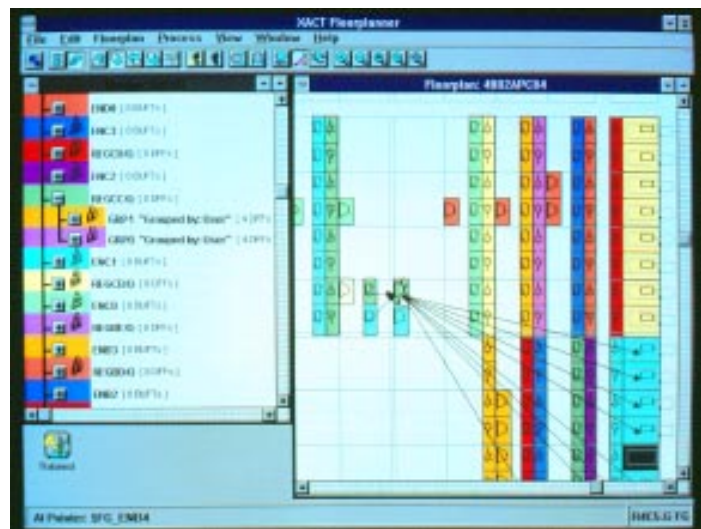
The Floorplanner supports the XC3000A, XC3100A, XC4000 and XC5000 families.



Design Manager

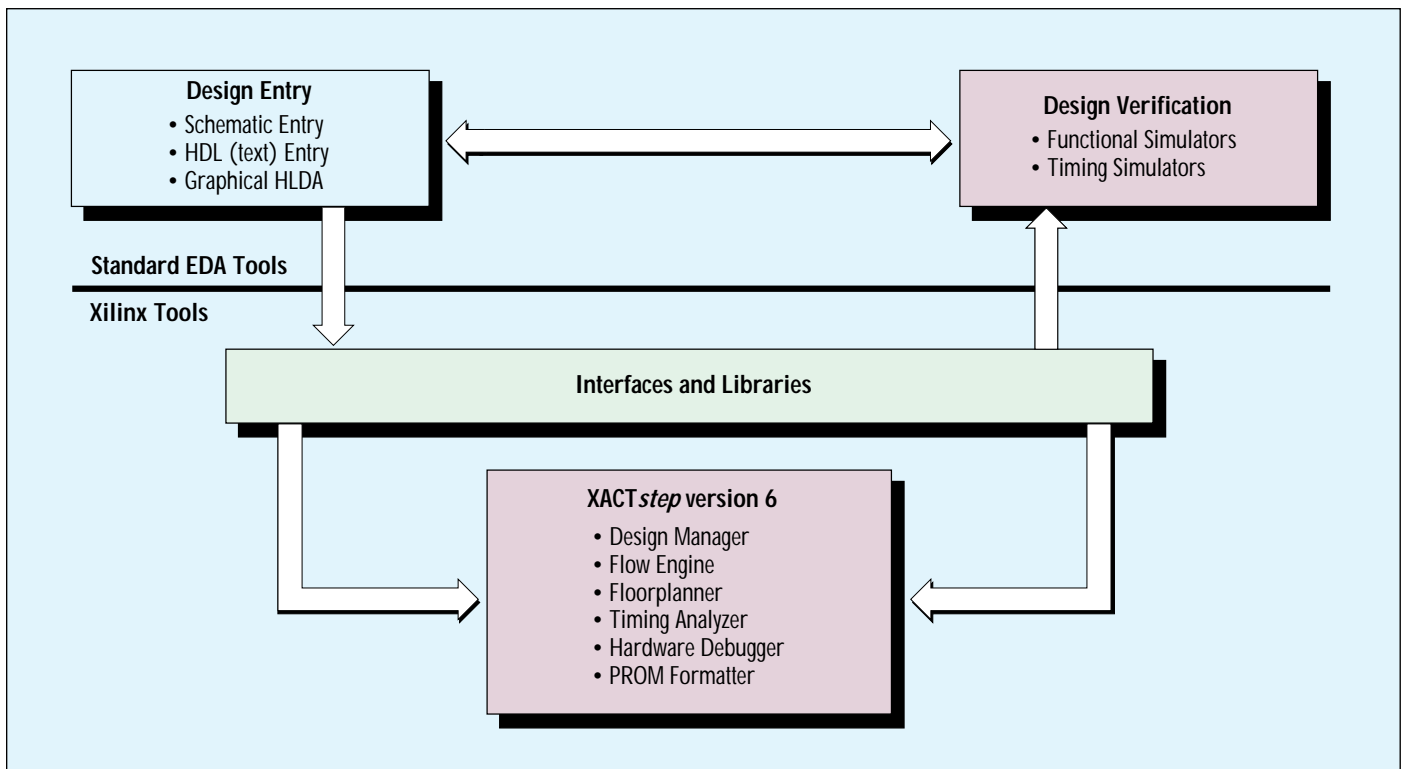


Flow Engine



Floorplanner

Xilinx Design Methodology



The Xilinx “open tools” approach uses third-party EDA tools for design entry and simulation.

Design Entry is accomplished using schematics, text-based HDL, and graphical HLDA to capture design function and timing requirements. These entry methods can easily be combined allowing the designer to choose the best tool for each portion of the design.

Libraries and interfaces for Viewlogic, Orcad, Mentor Graphics and Synopsys are available directly from Xilinx. Many others are available from the Xilinx Alliance partners including Cadence and Data I/O.

To simplify schematic entry, Xilinx provides a module generator and optimization tool called X-BLOX. This provides a tremendous boost in productivity by allowing the designer to capture their design using large functional elements. Optimization software chooses the best architectural implementation for speed or density taking full advantage of Xilinx's extensive device features. Synthesis vendors also support X-BLOX libraries to produce efficient design results.

During design entry, XACT performance lets the designer specify detailed timing requirements right in the schematic or HDL description. This information is used by the timing-driven place and route tools to make optimal use of the available resources.

Results from the design entry process are controlled by the Xilinx Design Manager which is part of XACT^{step} v6. It manages design revisions and allows re-targeting to different devices sizes and speed grades. The Design Manager is also used to launch implementation and verification tools by clicking on tool bars and icons.

Design Implementation

Design implementation is controlled by a powerful Flow Engine provided in XACT *step 6*.

For FPGA designs, the Flow Engine processes a schematic or HDL design into a BIT or PROM file that can be downloaded into a Xilinx device. Tools for logic reduction, design rule checking, mapping, automatic placement and routing and bitstream generation are included. Designers can choose a fully automatic flow or set break points that allow analysis and optimization of results before proceeding to the next step.

Powerful optimization tools such as the Floorplanner and XACT Design Editor (XDE) are included in XACT_{step} v6 to allow hand-crafting of high density or high performance designs.

For design iterations, guided design implementation allows unchanged portions of the design to maintain existing placement and routing.

At the completion of design implementation, designers of SRAM-based FPGAs can load the bitstream right into the target device or use the PROM Formatter to create a daisy chain or PROM programming file.

For CPLD designs, XACT^{step} v6 provides all the tools needed to process an XNF, CUPL, ABEL or PALASM file into a programming file. Included are tools for PLD compiler support and automatic optimization and mapping. This product can be used stand-alone or in combination with a wide variety of schematic entry, simulation and PLD compiler tools.

Design Verification and Debug

Verification of the performance and function of the design is accomplished with a combination of Xilinx tools and standard EDA tools.

Standard EDA tools are used for functional and timing simulation. Interfaces to simulators from Viewlogic, Orcad, Mentor Graphics and Synopsys are available directly from Xilinx. Many others are available from the Xilinx Alliance partners including Cadence's Verilog.

Verification tools provided by Xilinx in XACT^{step} v6 include an interactive Timing Analyzer and a powerful Hardware Debugger. These tools allow static timing analysis and in-circuit verification and debug.

Interfaces and Libraries available from Xilinx

Xilinx-generated third-party interfaces and libraries contain schematic symbols or HDL libraries, simulation models and Xilinx Netlist Format (XNF) translators.

Design Entry Tools available from Xilinx

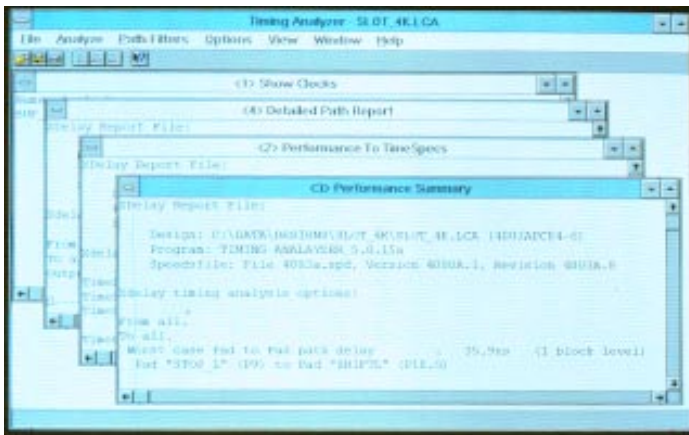
Stand alone packages are available that include Microsoft Windows based Viewlogic tools for the PC. In addition to the interfaces and libraries, these include the Viewlogic PROcapture Schematic Entry and Viewlogic PROsim Simulation tools. Extended packages are available that include Viewlogic PROsynthesis VHDL.

Xilinx ABEL supports text-based design entry and netlist translation using ABEL description language. ABEL language supports different design styles including Boolean equations, truth tables and encoded or symbolic state machines. It can be used for FPGA and EPLD designs.

Available Directly From Xilinx

Design Entry Viewlogic PROcapture Viewlogic PROsynthesis (VHDL) Xilinx ABEL
Interfaces and Libraries Viewlogic OrCAD Mentor Graphics Synopsys Cadence
Simulation Viewlogic PROsim
Design Management, Implementation and Verification XACT ^{step} version 6

Please reference the Xilinx Yellow Pages directory for an extensive list of tools available from our Alliance Partners



Timing Analyzer

Timing Analyzer

The new interactive Timing Analyzer simplifies the complex task of analyzing a design's performance. Powerful timing filters, accessed through pop-up menus, let the designer choose the exact paths they want to analyze.

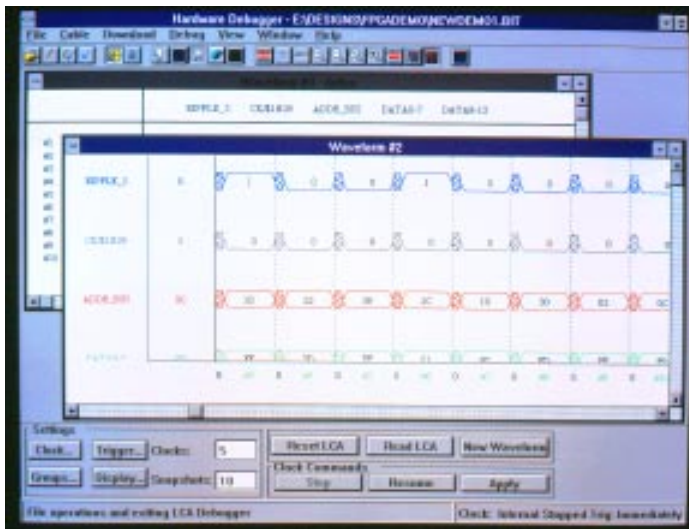
In addition, the Timing Analyzer shows the design's maximum clock frequencies, automatically compares actual delays to XACT-Performance specifications and finds the critical timing paths.

Hardware Debugger

The Hardware Debugger frees designers from the time consuming task of writing exhausting simulation vectors by allowing them to view internal signals while the FPGA device is running in circuit.

This innovative tool takes advantage of the reprogrammability of SRAM-based devices by configuring the FPGA in-circuit using a cable connected to a host PC or workstation.

While the device is running, an unlimited number of internal nodes can be displayed in a waveform window. By giving the Hardware Debugger control over the system clock, designers can step through their state machines and easily debug their logic and printed circuit boards.

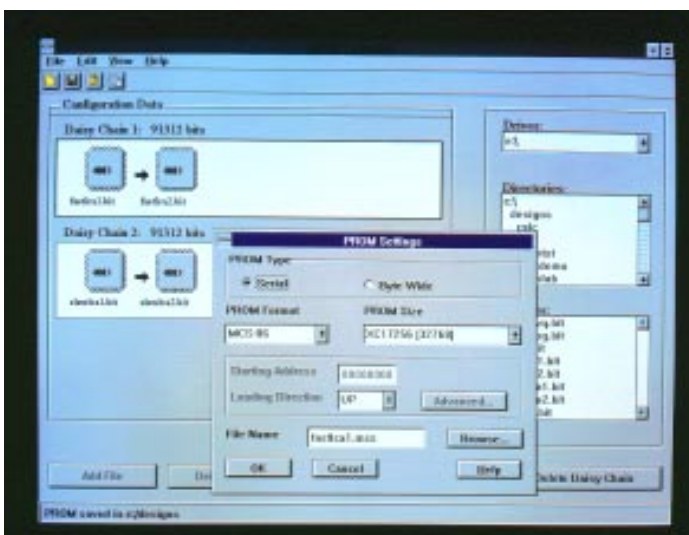


Hardware Debugger

PROM Formatter

The new PROM Formatter makes it easy for the designers to create PROM programming files for SRAM-based devices. This tool chooses the best PROM size and automatically splits the data into multiple files if smaller PROMs are required. It supports serial and byte wide PROMs in four different formats.

If the target system uses the daisy chain capability of the Xilinx FPGA, the PROM Formatter graphically creates the load order and verifies the load sequence.



PROM Formatter

Product Descriptions

Viewlogic interface and libraries offer support for all Viewlogic software products including PRO series, WorkView PLUS, PowerView and WorkView. The libraries support all Xilinx FPGAs and EPLDs. The interface is part of a well-integrated environment that allows the designer to easily access schematic capture tools, VHDL synthesis and simulation.

Synopsys - The Xilinx Synopsys Interface (XSI) consists of libraries for use with the Synopsys Design Compiler or FPGA Compiler synthesis tools and the VHDL System Simulator. With XSI, a designer can use either VHDL or Verilog HDL to design XC3000, XC4000 and XC5000 family FPGAs and all Xilinx EPLDs. Support is also included for X-BLOX optimized macrofunctions.

Mentor Graphics contains Falcon-integrated, Motif-based interface and libraries for Design Architect and QuickSim II. Intelligent scripts allow users to automatically get into functional and timing simulation from the push-button interface for both FPGAs and EPLDs.

OrCAD contains libraries for SDT386+ and timing models for VST386+. Translators allow users to easily move from schematics to functional simulations to post-route timing simulations for both FPGAs and EPLDs.

Alliance Program (Third party generated interfaces)

The Xilinx "open tools" approach welcomes third party support for Xilinx devices. Most EDA/CAE companies build and distribute design kits for Xilinx. These kits typically include symbol libraries, timing models, and translators for schematic entry and simulation. HDL interfaces contain libraries for synthesis tools.

Xilinx Software Packages

The Xilinx development system software is available in complete packages or as individual software products. Packages contain interfaces and libraries along with XACTstep v6 implementation and verification tools.

Base packages provide schematic capture and simulation interfaces, XACTstep v6 implementation and verification tools and download hardware for low complexity Xilinx devices. Devices supported include all EPLD families, the XC2000 FPGA family, XC3000, XC3000A, XC3100, XC3100A FPGA families (up to the XC3042/XC3142) and XC4000 FPGAs (up to the XC4003A).

Standard packages provide schematic capture and simulation interfaces, XACTstep v6 implementation and verification tools, X-BLOX module generator and optimizer and download hardware. These packages support all Xilinx devices.

Stand-alone packages are complete turnkey systems that include Microsoft Windows based Viewlogic tools on the PC.

The Stand-alone Base package includes the PROcapture schematic editor and PROsim simulator limited to 5,000 gates. It also includes all the components of the Base package.

The Stand-alone Standard package includes the PROcapture schematic editor and PROsim simulator with unlimited gates. It also includes all the components of the Standard package.

The Stand-alone Extended package includes VHDL entry, synthesis and VHDL simulation (PROsynthesis) plus all the features of the Standard Stand-alone Package.

Xilinx Support

- Software and documentation updates*
- Toll-free applications hotline
- Xilinx technical bulletin board access
- XCELL technical newsletter
- Access to Apps FAX
- Technical notes on common software issues

Platform Support

XACTstep v6 runs on IBM PC and compatible platforms with Microsoft Windows installed.

Workstation based tools with similar capabilities are supported by XACTstep v5.2.

Ordering Information

Please refer to Xilinx Reference and Pricing Guide or contact a Xilinx sales representative or distributor.

** Not included in all configurations.*



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