

CORE Generator™ tool for PCI

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Product Description

Features

- Supports LogiCORE PCI Master and Slave Interfaces
 - ◊ Fully 2.1 PCI compliant 32 bit, 33MHz PCI Interface cores for Xilinx XC4000-series FPGAs and HardWire
 - ◊ Pre-defined implementation for predictable timing
 - ◊ Enables 100% programmable single-chip solution with customizable back-end design
- Generates design files with functionality to customer specifications
- Generates simulation model for instant functional simulation
- Supports VHDL, Verilog and schematic design flows
- Easy-to-use Graphical User Interface (GUI)¹
 - ◊ Look and feel identical to PCI SIG Specification
 - ◊ Menu-driven parameter entry eliminates invalid data input
 - ◊ EDA tool independent
- Runs over the Internet¹
 - ◊ Instant access to new updates
 - ◊ Platform independent - runs in Java-enabled Web browser
- Extensive on-line help

For more information on LogiCORE PCI Master and Slave Interfaces, see separate product descriptions.

For more information on the VHDL and Verilog design methodology, see separate application *Using pre-implemented LogiCORE PCI Interfaces with VHDL and Verilog*.

Introduction

Xilinx's innovative CORE Generator tool for PCI is designed to solve performance and time-to-market issues associated with generic synthesizable cores used for high-performance FPGA applications.

An FPGA design compliant to the stringent PCI specification requires an implementation highly optimized for the targeted FPGA architecture and feature set. Typically, a generic synthesizable PCI core described in VHDL or Verilog for ASICs will not meet timing requirements in an FPGA without serious consideration to partitioning, placement, and routing of the design. Furthermore, the end-result is affected by coding style, synthesis tools, and

the customer back-end design. The engineering effort to tune a synthesizable PCI core for timing and to fully verify the design can add up to months even for an experienced FPGA designer. To address these issues, Xilinx has developed the CORE Generator and a design methodology for VHDL, Verilog and schematic design specially optimized for high-performance FPGA design.

The result: design time can be cut by months and you will be able to bring your product faster to market. After all, that is what FPGAs are all about.

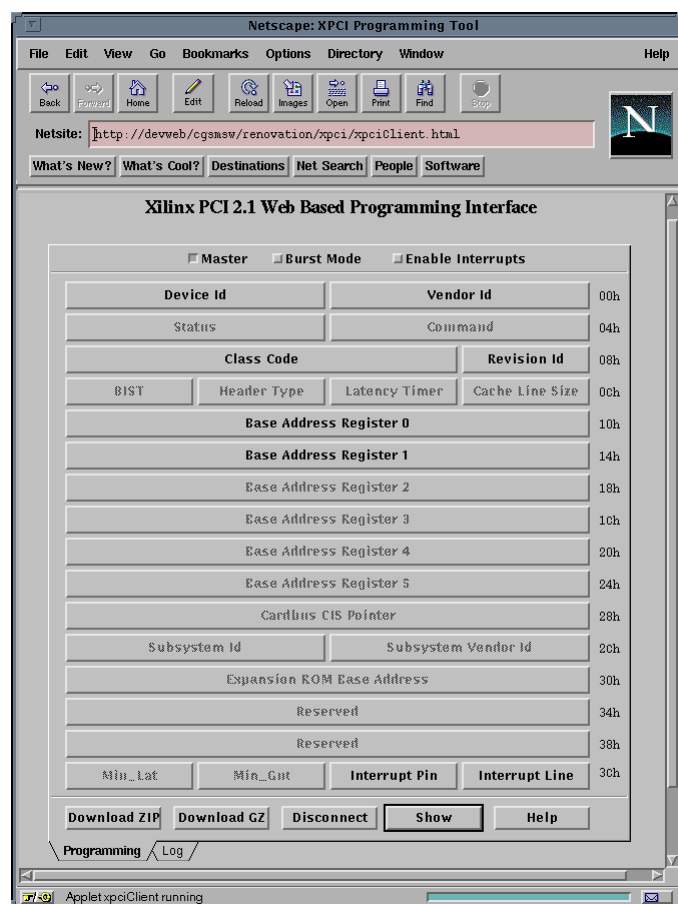


Figure 1: CORE Generator for PCI

General Description

Based on the user's specifications the CORE Generator tool generates a highly optimized PCI core with all critical paths pre-laid out and fully verified. This ensures that the core always meet the timing of the PCI spec. The user customizes the PCI core by entering parameters in an intuitive GUI. Parameter entry is completely menu driven, which prevents input of invalid data. As a result, the learning curve for PCI is greatly reduced. The generated

¹ Patent pending

PCI core is then instantiated in a VHDL, Verilog or schematic entry environment. The user benefits from both the flexibility of behavior-level design methodologies and predictability of the core.

In addition, the CORE Generator produces a VHDL and Verilog simulation model for functional verification.

The CORE Generator tool, developed in Java, is executable on WebLINX, Xilinx home page, to allow immediate access to core enhancements and added features. Simply logon to the CORE Solutions Section of WebLINX (www.xilinx.com/products/logicore/logicore.htm) and run the CORE Generator in any Java-enabled Web browser on any PC, Macintosh or workstation.

LogiCORE PCI

The CORE Generator tool for PCI enables customization of the features of Xilinx LogiCORE PCI Master and Slave Interfaces. The LogiCORE PCI products are highly optimized, pre-implemented and fully tested cores for Xilinx XC4000-series FPGAs. Depending on the size of the FPGA, between 5K and 15K gates remain for integrating a unique back-end interface and other system functions into a fully programmable one-chip solution. Xilinx DesignOnce™ service allows an automatic conversion to a low cost HardWire™ device for high-volume production.

The pin-out and the relative placement of the internal Configurable Logic Blocks (CLBs) are pre-defined. Critical paths are controlled by TimeSpec's to ensure that timing is always met. This significantly reduces engineering time required to implement the PCI portion of your design. Resources can instead be focused on the unique back-end logic in the FPGA and the system level design. As a result, the LogiCORE PCI products can cut your development time by several months.

Core Configuration

Customization of a LogiCORE PCI Interface is performed through an easy-to-use, menu-driven Graphical User Interface (GUI). The main window of the GUI, showed in Figure 1 is made to look identical to "Figure 6-1: Type 00h Configuration Space Header" in the PCI Local Bus Specification, Revision 2.1. This makes it extremely easy for a designer to navigate between the various options. Parameter entry is menu-driven so that no schematics or netlists must be edited. The following parameters of the core can be customized:

- Initiator/target functionality (PCI Master only)
- Enable burst transactions
- Enable interrupts
- Configuration Space Header
 - ◊ Device ID
 - ◊ Vendor ID
 - ◊ Class Code
 - ◊ Revision ID
- Base Address Register configuration (1 or 2 registers, size and mode)

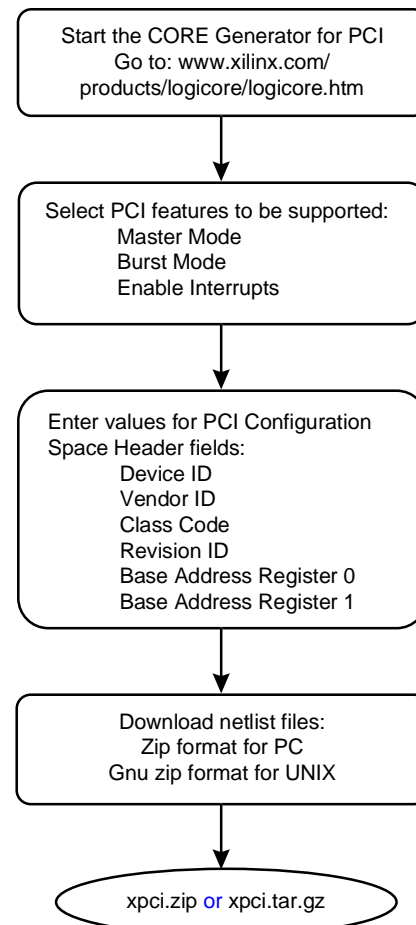


Figure 2: CORE Generation design flow

Initiator/Target Functionality

The "Master" button enables the device to act as a PCI Bus Master (initiator). De-selecting the "Master" button disables Bus Mastering (target functions only).

Enable Burst Transactions

The "Burst Mode" button enables the device to generate and receive burst mode transactions. The "Burst Mode" button de-selected disables the Source Enable logic and the Latency Timer.

Enable Interrupts

The "Enable Interrupts" button enables the interrupt logic.

Device ID

The Device ID field is used to identify a particular PCI device. The individual vendor determines the value.

Vendor ID

The Vendor ID is used to identify the device manufacturer. A unique Vendor ID is assigned by the PCI-SIG.

Class Code

The Class Code is used to determine the device's general function. The Xilinx PCI Configuration Manager displays the classes for this register, and allows the user to select from the list.

Base Class	Meaning
00h	Device was built before final Class Code definitions.
01h	Mass storage controller.
02h	Network controller.
03h	Display controller.
04h	Multimedia device.
05h	Memory controller.
06h	Bridge device.
07h	Simple communication controllers.
08h	Base system peripherals.
09h	Input devices.
0Ah	Docking stations.
0Bh	Processors.
0Ch	Serial bus controllers.
0D - FEh	Reserved.
FFh	Devices does not fit in any defined category.

Figure 3: Class Code selection window

Revision ID

The Revision ID is used to identify a particular version of a PCI device. The individual vendor determines the value.

Base Address Register (BAR) 0 - 1

The Base Address Register is used to determine how to allocate memory or I/O space to the particular PCI device.

The Xilinx PCI Configuration Manager displays the various Memory or I/O space options, and allows the user to select from the list of options. Base Address Register 0 is the first Base Address Register, located at offset 10h. Base Address Register 1 is the second Base Address Register, located at offset 14h.

Download Customized PCI Core

Once the CORE configuration is completed, the customized, yet optimized and verified, design files can be downloaded. The files are compressed into a Zip format for PC or a GNU zip format for UNIX.

The downloaded file includes all design data necessary to implement the LogiCORE PCI Interface in the FPGA.

- User-selected configuration settings used to generate the LogiCORE PCI
- Constraint files for implementation on XC4013E PQ208
- Design files for instantiation in VHDL or Verilog
- VHDL or Verilog simulation model for functional verification
- Synopsys sample synthesis script
- Hierarchical XNF netlist for implementation of the PCI Interface

The PCI module generated by the PCI Core Generator is identical to the Viewlogic schematic-based LogiCORE PCI designs shipped on CD-ROM. Current users can substitute the Viewlogic schematic product with the generated XNF netlists, without changing the top-level design. Furthermore, schematic files for Viewlogic are available if source code is required.

Design Integration

The resulting core is instantiated in the user design, described in VHDL, Verilog or schematic. Functional verification can be completed with the accompanying simulation model. See the Application Note *Using pre-implemented LogiCORE PCI Interfaces with VHDL and Verilog* for further details on the design flow.

Recommended Design Experience

The LogiCORE PCI interface is pre-implemented, allowing engineering focus at the unique back-end functions of a PCI design. Regardless, PCI is a high-performance system that is challenging to implement in any technology, ASIC or FPGA. Therefore, we recommend previous experience with building high-performance, pipelined FPGA designs using Xilinx implementation software, Floorplaner, TIMESPECs, and guide files. The challenge to implement a complete PCI design including back-end functions varies depending on configuration and functionality of your application. Contact your local Xilinx representative for a closer review and estimation for your specific requirements.

Ordering Information

The CORE Generator for PCI is available on WebLINX at www.xilinx.com/products/logicore/logicore.htm

For pricing and availability of LogiCORE products please contact your local Xilinx sales office.

Table 1: Part Numbers

Product	Part number	Supplier
LogiCORE™ PCI Master Interface	LC-DI-PCIM-C	Xilinx, Inc.
LogiCORE™ PCI Slave Interface	LC-DI-PCIS-C	Xilinx, Inc.

Related Information

Xilinx Documents

More PCI related information is available on WebLINX:

www.xilinx.com/products/logicore/logicore.htm

Documents include:

- LogiCORE PCI Master, LogiCORE PCI Slave - product description
- *LogiCORE PCI Master and Slave Interface User's Guide*
- *Using pre-implemented LogiCORE PCI Interfaces with VHDL and Verilog* - Application Note

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