



HardWire™ Array Initial Design Submittal Form

Date _____

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone () _____ Fax () _____

Customer Internal Part Number _____

FPGA File Name and Revision Date _____

Xilinx HardWire Array Device # _____

Temp. Grade (Check One) ☐ C ☐ I

(see cross reference table in HardWire Data Book for correct part number)

☐ 5 V ☐ 3.3 V (Check One)

Package _____

End Application For Device _____

Actual Function Performed In System _____

(information will be used for import/export purposes only)

Design Information Submitted to Xilinx:

PLD Design File Name _____

.XRP "DRC Informational" File Name _____

Design Schematic _____

Timing Diagram of System I/Os _____

Design Block Diagram _____

Development Methodology Used:

Design entry method used (Check all that apply):

☐ Schematic (type) _____ ☐ X-BLOX ☐ XABEL ☐ Synthesis type

Simulation: ☐ Not done ☐ Done with _____

FPGA Device _____ Speed Grade _____ Package _____ Temperature Grade _____

Configuration Mode Used in Programmable FPGA:

☐ Peripheral Synchronous ☐ Master Serial ☐ Slave Serial
☐ Peripheral Asynchronous ☐ Master Parallel Up ☐ Master Parallel Down
☐ Peripheral Parallel ☐ Express™ Mode

Is Configuration Emulation Needed? ☐ Yes ☐ No

Boundary Scan Emulation Needed? ☐ Always ☐ Only prior to configuration ☐ Never

RAM Description (Name, Size, Cycle, Time, etc.) _____

For Xilinx Use Only

Date Received _____

Marketing _____

Application Engineer _____

HD Code _____