



XC2318/L HardWire™ Array Design Verification Form

Company Name _____ Customer Name _____

Address _____ City _____ State _____ Zip _____

Telephone () _____ Fax () _____

Customer Internal Part Number _____

FPGA File Name and Revision Date _____

Xilinx HardWire Array Device # _____

(see cross reference table in HardWire Data Book for correct part number)

☐ 5 V ☐ 3.3 V (Check One)

Temp. Grade (Check One) ☐ C ☐ I

Package _____

HardWire Array Options:

Input Voltage Levels TTL _____ CMOS _____ (for low power)

Configuration Time Interval (D/P High) 64 μ s _____ 64 ms _____

Internal Pull-up Resistors:

D/P Yes _____ No _____

CCLK Yes _____ No _____

M0 Yes _____ No _____

PWRDWN Yes _____ No _____

HDC Operation Yes _____ No (I/O Only) _____

LDC Operation Yes _____ No (I/O Only) _____

DOOUT During Configuration DOOUT = DIN _____ High Impedance _____

Oscillator Inactive _____ Active _____

Package Marking Options:

☐ Custom Marking Form Attached ☐ Standard Xilinx Marking

Customer Part Marking for Device Package (Optional - 11 Characters max.)

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HardWire Terms and Conditions:

Please put a check mark against the following items as applicable. All items need to be checked for a signoff.

☐ The application circuit board must have a provision for configuration program storage (i.e., XC17128, EPROM, etc.). The socket can be left unpopulated when conversion to the HardWire device is made. The HardWire device is designed to provide a cost reduction path for existing fully debugged programmable designs.

☐ I certify that the above listed Design File and revision date is the correct design.

☐ I have reviewed the attached Xilinx HardWire Review Report (including the list of potentially hazardous nets) and have determined that none of the issues raised will be a problem in the system.

☐ I authorize Xilinx to start the HardWire fabrication process.

Customer Name _____ Signature _____ Date _____

For Xilinx Use Only

Xilinx HardWire Design Center Manager: _____ Signature _____ Date _____

Xilinx Review Number (HD Code): _____

Xilinx Customer Service: _____ Signature _____ Date _____

NRE PO Number: _____

Xilinx Product Engineering Manager: _____ Signature _____ Date _____

Xilinx Part Number (HPC Code): _____

Mask Set _____ Hole Mask _____ Program Code _____