

# Application Notes

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# XC3000 Applications

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- **Application Notes**

- [Loadable Binary Counters](#)
- [Register-Based FIFO](#)
- [Boundary-Scan Emulator for XC3000](#)
- [Harmonic Frequency Synthesizer and FSK Modulator](#)
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- [Adders, Subtractors and Accumulators in XC3000](#)
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- [Frequency/Phase Comparator for Phase-Locked Loops](#)
- [Serial Code Conversion Between BCD and Binary](#)
- [Megabit FIFO in Two Chips: One LCA Device and One DRAM](#)
- [Fully Compliant PCI Interface in XC3164A-2 FPGA](#)
- [C-Cube CL550 and Xilinx XC3020A ISA-Based Motion-JPEG Codec](#)
- [Configuring Mixed FPGA Daisy Chains](#)
- [Configuring FPGAs Over a Processor Bus](#)
- [Pulse-Width Modulation in Xilinx](#)
- [Design Migration from XC2000/XC3000 to XC5200](#)

- **Data Book**

- [XC3000 Series Field Programmable Gate Arrays](#)
- [XC3000A Field Programmable Gate Arrays](#)
- [XC3000L Field Programmable Gate Arrays](#)
- [XC3100A Field Programmable Gate Arrays](#)
- [XC3100L Field Programmable Gate Arrays](#)
- [Additional XC3000 Data](#)
- [3.3V and Mixed Voltage Compatible Products](#)

- **[XCELL Articles](#)**

# XC3000 Applications - XCELL Articles

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- [Demultiplexing 200 MHz Data Streams](#)
- [Ten-Digit Fully Synchronous BCD Counter Runs at 87 MHz](#)
- [Additional Settings for XC3000 and XC5200 in Synopsys](#)
- [Manchester Decoder in 3 CLBs](#)
- [Retargeting Designs in Mentor Design Architect](#)
- [Turning off the Internal Oscillator](#)
- [FPGAs Control ATM Connections to French Telecom Network](#)

## 3.3 Volt Devices

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- **Data Book**

- [3.3 V and Mixed Voltage Compatible Products](#)
- [XC9500 In-System Programmable CPLD Family](#)
- [XC7300 CMOS PLD Family](#)
- [XC4000 Series Field Programmable Gate Arrays \(XC4000XL\)](#)
- [XC4000XL Switching Characteristics](#)
- [XC4000L Switching Characteristics](#)
- [XC5200L Field Programmable Gate Arrays](#)
- [XC3000L Field Programmable Gate Arrays](#)
- [XC3100L Field Programmable Gate Arrays](#)

- **XCELL Articles**

- [XC4062XL Debuts](#)
- [Low-Voltage Product Line Expands With XC3100L and XC4000L FPGA Families](#)
- [XC4000 Drives 3.3V Devices Safely](#)
- [Power, Package, and Performance: Trading Off Among the Three P's](#)
- [Minimizing Power Consumption in FPGA Designs](#)
- [Mixing 3.3 Volt and 5 Volt Devices](#)

# XC4000 Series Applications

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- **Application Notes**
  - [XC4000 Series Edge-Triggered & Dual-Port RAM](#)
  - [Using Select-RAM Memory in XC4000 Series FPGAs](#)
  - [System Design with New XC4000EX I/O Features](#)
  - [Implementing FIFOs in XC4000 Series RAM](#)
  - [Synchronous and Asynchronous FIFO Designs](#)
  - [Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators](#)
  - [Using the Dedicated Carry Logic in XC4000E](#)
  - [Accelerating Loadable Counters in XC4000](#)
  - [Estimating Performance of XC4000E Adders & Counters](#)
  - [Ultra-Fast Synchronous Counters](#)
  - [Implementing State Machines in LCA Devices](#)
  - [Bus-Structured Serial Input/Output Device](#)
  - [Harmonic Frequency Synthesizer and FSK Modulator](#)
  - [Complex Digital Waveform Generator](#)
  - [16-Tap, 8-Bit FIR Filter](#)
  - [Using Programmable Logic to Accelerate DSP Functions](#)
  - [Using FPGAs for Application-Specific DSP Performance](#)
  - [Constant Coefficient Multipliers for the XC4000E](#)
  - [Block Adaptive Filter](#)
  - [Building High Performance FIR Filters Using KCMs](#)
  - [The Fastest FFT in the West](#)
  - [The Fastest Filter in the West](#)
  - [Plug and Play ISA in Xilinx FPGAs](#)
  - [Dynamic Microcontroller in XC4000](#)
  - [Pulse-Width Modulation in Xilinx](#)
  - [Design Migration from XC4000 to XC4000E](#)
  - [Design Migration from XC4000 to XC5200](#)
  - [CPLD-Based 1mbit Virtual SPROM Downloader for XC4000-Series FPGAs](#)
  - [Configuring Mixed FPGA Daisy Chains](#)
  - [Configuring FPGAs Over a Processor Bus](#)
  - [Using the XC4000 Readback Capability](#)
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# XC4000 Applications

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- **Application Notes (continued)**
  - [XC4000/XC5200 PC84 Footprint Compatibility](#)
  - [Boundary Scan in XC4000 and XC5000 Series Devices](#)
  - [LCA Speed Estimation: Asking the Right Question](#)
  - [Improving XC4000 Design Performance](#)
- **Application Briefs**
  - [XC4000E Select-RAM: Flexibility with Speed](#)
  - [XC4000E Low Power Consumption: At High Speeds](#)
  - [XC4000E Select-RAM: Maximum Configurability](#)
  - [XC4000EX Routing: A Comparison with XC4000E and ORCA](#)
  - [XC4000-Series FPGAs: The Best Choice for Delivering Logic Cores](#)
- **Data Book**
  - [XC4000 Series Field Programmable Gate Arrays](#)
  - [XC4000E Switching Characteristics](#)
  - [XC4000EX Switching Characteristics](#)
  - [XC4000XL Switching Characteristics](#)
  - [XC4000L Switching Characteristics](#)
  - [XC4000 High Reliability Family](#)
  - [XC4000 Series Technical Information](#)
  - [3.3V and Mixed Voltage Compatible Products](#)
- [XCELL Articles](#)

# XC4000 Applications

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- **XCELL Articles**

- [XC4062XL Debuts](#)
- [Faster XC4000E-1 FPGAs Support High-Performance Applications](#)
- [New XACTstep M1 Software for High-Density Designs](#)
- [Implementing Median Filters in XC4000E FPGAs](#)
- [XC4000 Series Select-RAM Memory: Advantages and Uses](#)
- [FIFO Buffer Designs in the XC4000E/EX FPGA Families](#)
- [Synchronous RAM Improves System Speed](#)
- [Synchronous RAM Timing in the XC4000E FPGA](#)
- [Advanced Carry-Logic Techniques](#)
- [Distributed Arithmetic Laplacian Filter](#)
- [XC4000 Drives 3.3V Devices Safely](#)
- [Introducing the XC4000EX Family](#)
- [PCI-Based Reconfigurable Computers](#)
- [Examining XC4000E RAM Capabilities](#)
- [Manchester Decoder in 3 CLBs](#)

# XC5200 Applications

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- **Application Notes**
  - [Macro Library Supplement](#)
  - [Implementing State Machines in LCA Devices](#)
  - [Design Migration from XC2000/XC3000 to XC5200](#)
  - [Design Migration from XC4000 to XC5200](#)
  - [Gate Count Capacity Metrics for FPGAs](#)
  - [Configuring Mixed FPGA Daisy Chains](#)
  - [XC4000/XC5200 PC84 Footprint Compatibility](#)
  - [Boundary Scan in XC4000 and XC5000 Series Devices](#)
- **Data Book**
  - [XC5200 Field Programmable Gate Arrays](#)
  - [XC5200L Field Programmable Gate Arrays](#)
  - [XC5202 Pinouts in VQ64 Package](#)
- **XCELL Articles**
  - [Designing with XC5200 Carry Logic](#)
  - [Additional Settings for XC3000 and XC5200 in Synopsys](#)
  - [FPGAs Go "Down Under" in an ISDN Terminal Adapter](#)
  - [Manchester Decoder in 3 CLBs](#)
  - [Retargeting Designs in Mentor Design Architect](#)
  - [Turning off the Internal Oscillator](#)
  - [Videoconferencing with XC5000 FPGAs](#)



# XC6200 Applications

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- **Application Notes**
  - [Interfacing the XC6200 to a Microprocessor - Motorola MC68020 Example](#)
  - [Interfacing the XC6200 to a Microprocessor - TMS320C50 Example](#)
- **Data Sheet**
  - [XC6200 Field Programmable Gate Arrays](#)
- **XCELL Articles**
  - [Virtual Computer Debuts XC6200 Development Kit](#)
  - [Reconfigurable Computing: Coming of Age](#)
  - [The New XC6200 FPGA Architecture](#)

# Arithmetic Function Applications

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- **Application Notes**
  - [16-Tap, 8-Bit FIR Filter](#)
  - [Constant Coefficient Multipliers for the XC4000E](#)
  - [Building High Performance FIR Filters Using KCMs](#)
  - [The Role of Distributed Arithmetic in FPGA-Based Signal Processing](#)
  - [Harmonic Frequency Synthesizer and FSK Modulator](#)
  - [Adders, Subtractors and Accumulators in XC3000](#)
  - [Using the Dedicated Carry Logic in XC4000E](#)
- **XCELL Articles**
  - [Implementing Median Filters in XC4000E FPGAs](#)
  - [Distributed Arithmetic Laplacian Filter](#)
  - [Advanced Carry-Logic Techniques](#)
  - [Designing with XC5200 Carry Logic](#)

# Bus Applications

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- **Application Notes**
  - [Fully Compliant PCI Interface in XC3164A-2 FPGA](#)
  - [Plug and Play ISA in Xilinx FPGAs](#)
  - [Bus-Structured Serial Input/Output Device](#)
  - [C-Cube CL550 and Xilinx XC3020A ISA-Based Motion-JPEG Codec](#)
  - [Dynamic Microcontroller in XC4000](#)
  - [Configuring FPGAs Over a Processor Bus](#)
  - [Interfacing XC6200 to Microprocessors \(TMS320C50 Example\)](#)
  - [Interfacing XC6200 to Microprocessors \(MC68020 Example\)](#)
- **XCELL Articles**
  - [New LogiCORE PCI Target Eases System Integration](#)
  - [PCI-Based Reconfigurable Computers](#)
  - [First LogiCORE Module: PCI Interface](#)

# Configuration Applications

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- **Application Notes**
  - [CPLD-Based 1MBit Virtual SPROM Downloader for XC4000-Series FPGAs](#)
  - [FPGA Configuration Guidelines](#)
  - [Configuring Mixed FPGA Daisy Chains](#)
  - [Configuration Issues: Power-up, Volatility, Security, Battery Back-up](#)
  - [Dynamic Reconfiguration](#)
  - [Using the XC4000 Readback Capability](#)
  - [Boundary Scan in XC4000 and XC5000 Series Devices](#)
  - [XC2000 Power Monitoring](#)
  - [Configuring FPGAs Over a Processor Bus](#)
  - [Interfacing XC6200 to Microprocessors \(TMS320C50 Example\)](#)
  - [Interfacing XC6200 to Microprocessors \(MC68020 Example\)](#)
  - [XC3000 Series Technical Information \(CCLK, Powerdown, Startup\)](#)
  - [Using In-System Programmability in Boundary-Scan Systems](#)
  - [Using Automatic Test Equipment to Program XC9500 Devices In-System](#)
  - [In-System Programming Times](#)
  - [XC9500 In-System Programming Using an 8051 Microcontroller](#)
  - [Programming Xilinx XC9500 CPLDs on HP 3070 Testers](#)
- **Application Briefs**
  - [FastFlash: A New Electrically Erasable CPLD Technology](#)
- **Data Book**
  - [XC1700D Family of Serial Configuration PROMs](#)
- **[XCELL Articles](#)**

# Configuration Applications

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- **XCELL Articles**

- [Programmer Support](#)
- [XC9500 ISP on the HP3070 Tester](#)
- [Downloading CPLDs with an Embedded Processor](#)
- [New CPLD Software Updates, HW-130 Device Programmer Update](#)
- [PCI-Based Reconfigurable Computers](#)
- [Metalithic System Exploits Real-Time Reconfigurability for Audio Processing](#)
- [Sensitivity to Power Glitches](#)
- [Readback in FPGAs](#)
- [Reconfigurable Computing Developer's Platform](#)
- [Xilinx Takes the Lead in ISP Standardization Effort](#)
- [In-System Programming and Flash Technology for CPLDs](#)

# Counter Applications

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- **Application Notes**
  - [Accelerating Loadable Counters in XC4000](#)
  - [Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators](#)
  - [Estimating the Performance of XC4000E Adders and Counters](#)
  - [Ultra-Fast Synchronous Counters](#)
  - [Loadable Binary Counters](#)
  - [Implementing State Machines in LCA Devices](#)
  - [Using the Dedicated Carry Logic in XC4000E](#)
  - [Pulse-Width Modulation in Xilinx](#)
- **XCELL Articles**
  - [Ten-Digit Fully Synchronous BCD Counter Runs at 87 MHz](#)
  - [Advanced Carry-Logic Techniques](#)
  - [Designing with XC5200 Carry Logic](#)

# CPLD Applications

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- **Application Notes**
  - [CPLD-Based 1MBit Virtual SPROM Downloader for XC4000-Series FPGAs](#)
  - [XC9536 ISP Demo Board](#)
  - [Metastability Considerations](#)
  - [Embedded Instrumentation Using XC9500 CPLDs](#)
  - [Using ABEL with Xilinx CPLDs](#)
  - [Pin Preassigning with XC9500 CPLDs](#)
  - [Designing with XC9500 CPLDs](#)
  - [XC9500 Design Optimization](#)
  - [Using the XC9500 Timing Model](#)
  - [Using In-System Programmability in Boundary-Scan Systems](#)
  - [Using the XC9500 JTAG Boundary-Scan Interface](#)
  - [In-System Programming Times](#)
  - [Using Automatic Test Equipment to Program XC9500 Devices In-System](#)
  - [Design Migration with XC9500 CPLDs](#)
  - [XC9500 In-System Programming Using an 8051 Microcontroller](#)
  - [Programming Xilinx XC9500 CPLDs on HP 3070 Testers](#)
  - [Programming XC9500 CPLDs on GENRAD Testers, EZTag Version](#)
  - [Designing with XC7318/XC7336 CPLDs](#)
- **Application Briefs**
  - [FastFLASH : A New Electrically Erasable CPLD Technology](#)
  - [XC9500 Pin-Locking Capability and Benchmarks](#)
- **[XCELL Articles](#)**

# CPLD Applications

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- **XCELL Articles**

- [New XC9500 ISP Products in Volume Production](#)
- [New CPLD Software Updates](#)
- [HW-130 Device Programmer Update](#)
- [VITAL Model Support for XC9500 CPLDs](#)
- [XC9500 ISP on the HP3070 Tester](#)
- [Downloading CPLDs with an Embedded Processor](#)



# Other FPGA Application Notes

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See also: [XAPP Application Notes](#) and [Application Briefs](#)

- [Fully Compliant PCI Interface in an XC3164A-2 FPGA](#)
- [16-Tap, 8-Bit FIR Filter Application Note](#)
- [Using Programmable Logic to Accelerate DSP Functions](#)
- [A Guide to Using Field Programmable Gate Arrays \(FPGAs\) for Application-Specific DSP Performance](#)
- [Building High Performance FIR Filters Using KCMs](#)
- [FPGAs and DSP](#)
- [The Fastest FFT in the West](#)
- [The Fastest Filter in the West](#)
- [The Role of Distributed Arithmetic in FPGA-based Signal Processing](#)
- [Plug and Play ISA in Xilinx FPGAs](#)
- [Dynamic Microcontroller in XC4000](#)
- [Pulse-Width Modulation in Xilinx](#)
- [C-Cube CL550 and Xilinx XC3020A ISA-based Motion-JPEG Codec](#)
- [HDL Synthesis for FPGAs Design Guide](#)
- [XC5000 Macro Library Supplement](#)
- [Configuring FPGAs Over a Processor Bus](#)

# HDL Synthesis Applications

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- **Application Notes**

- [HDL Synthesis for FPGAs Design Guide](#)
- [Fully Compliant PCI Interface in an XC3164A-2 FPGA](#)

- **XCELL Articles**

- [Update Your Foundation Software with v6.0.2 Service Pack](#)
- [Xilinx Alliance EDA Companies, Products, and Contacts](#)
- [HDL Synthesis and Built-In Clock Enables](#)
- [Logic Synthesis for FPGAs - An Update](#)
- [Technical Questions and Answers: Synopsys BSCAN Instantiation](#)
- [Technical Questions and Answers: Mentor, Synopsys](#)
- [Technical Questions and Answers: Mentor, Synopsys](#)
- [Technical Questions and Answers: Synopsys](#)
- [Technical Questions and Answers: ABEL, Synopsys, Mentor](#)
- [Foundation Series Software Solutions: VHDL Made Easy](#)
- [Synopsys Introduces FPGA Express](#)

# Hi-Rel Product Applications

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- **Data Book**
  - [High-Reliability and Military Products](#)
  - [XC4000 Series High-Reliability Family](#)
- **XCELL Articles**
  - [Xilinx Receives QML Certification](#)
  - [FPGA Highs and Lows: Up in Space and Below the Surface](#)
  - [XC4000 Hi-Rel Product Family](#)

# JTAG Boundary Scan Applications

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- **Application Notes**
  - [Boundary Scan in XC4000 and XC5000 Series Devices](#)
  - [Boundary Scan Emulator for XC3000](#)
  - [Using the XC9500 Boundary-Scan Interface](#)
  - [Using In-System Programmability in Boundary-Scan Systems](#)
  - [Using Automatic Test Equipment to Program XC9500 Devices In-System](#)
  - [In-System Programming Times](#)
  - [XC9500 In-System Programming Using an 8051 Microcontroller](#)
- **XCELL Articles**
  - [Downloading CPLDs with an Embedded Processor](#)
  - [JTAG Support in the XC9500 CPLD Family](#)

# Memory Applications

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- **Application Notes**

- [XC4000 Series Edge-Triggered and Dual-Port RAM Capability](#)
- [Using Select-RAM Memory in XC4000 Series FPGAs](#)
- [Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators](#)
- [Implementing FIFOs in XC4000 Series RAM](#)
- [Synchronous and Asynchronous FIFO Designs](#)
- [High-Performance RAM-Based FIFO](#)

- **Application Briefs**

- [XC4000E Select-RAM: Flexibility with Speed](#)
- [XC4000E Select-RAM: Maximum Configurability](#)

- **XCELL Articles**

- [XC4000 Series Select-RAM Memory: Advantages and Uses](#)
- [Synchronous RAM Improves System Speed](#)
- [Synchronous RAM Timing in the XC4000E FPGA](#)
- [FIFO Buffer Designs in the XC4000E/EX FPGA Families](#)
- [Examining XC4000E RAM Capabilities](#)

# Packaging Applications

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- **Application Notes**
  - [Xilinx Thermally Enhanced Packaging](#)
  - [Footprint Compatibility Guide](#)
  - [Common XC4000/XC5200 PC84 Footprint](#)
  - [Ball-Grid Array Package Information](#)
  - [Pin Preassigning with XC9500 CPLDs](#)
- **Application Briefs**
  - [PLDs, Pins, and PCBs: The Importance of Pin-Locking and Footprint Compatibility](#)
  - [XC4000E Low Power Consumption: At High Speeds](#)
  - [XC9500 Pin Locking Capability and Benchmarks](#)
- **Data Book**
  - [Packages and Thermal Characteristics](#)
  - [XC5202 Pinouts including VQ64 Package](#)
- **XCELL Articles**
  - [Benchmarks Again Demonstrate XC9500 Pinlocking Capabilities](#)
  - [Benchmarks Confirm XC9500 CPLD Pin-Locking Capabilities](#)
  - [Power, Package, and Performance: Trading Off Among the Three P's](#)

# Schematic Entry Applications

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- **Application Notes**
  - [XC5000 Macro Library Supplement](#)
  - [Improving XC4000 Design Performance](#)
  - [Using Select-RAM Memory in XC4000 Series FPGAs](#)
  - [Design Migration from XC4000 to XC4000E](#)
  - [Design Migration from XC4000 to XC5200](#)
- **XCELL Articles**
  - [Xilinx Alliance EDA Companies, Products, and Contacts](#)
  - [Update Your Foundation Software with the v6.0.2 Service Pack](#)
  - [ProSeries Users Upgraded with Workview Office](#)
  - [OrCAD to Provide Support for OrCAD-Xilinx Interface](#)
  - [Using OrCAD Capture and Simulate with XACTstep version 6](#)
  - [Running Xilinx Foundation Series Software on a Network](#)
  - [Using Viewlogic's Workview Office with XACTstep version 6](#)
  - [Retargeting Designs in Mentor Graphics Design Architect](#)
  - [Technical Questions and Answers: Foundation, Mentor](#)
  - [Technical Questions and Answers: CPLDs, Mentor, Synopsys](#)
  - [Technical Questions and Answers \(Mentor\)](#)
  - [Technical Questions and Answers \(FXC library, Viewlogic\)](#)

# Timing Applications

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- **Application Notes**
  - [Set-up and Hold Times](#)
  - [Using the XC9500 Timing Model](#)
  - [Metastable Recovery \(FPGAs\)](#)
  - [Metastability Considerations \(CPLDs\)](#)
  - [Overshoot and Undershoot](#)
  - [LCA Speed Estimation: Asking the Right Question](#)
  - [Estimating the Performance of XC4000E Adders and Counters](#)
  - [Improving XC4000 Design Performance](#)
  - [XC4000 Series Technical Information \(Capacitive Loading, Ground Bounce\)](#)
  - [XC3000 Series Technical Information \(I/O Characteristics, Oscillator\)](#)
- **Application Briefs**
  - [PLL Design Techniques and Usage in FPGA Design](#)
- **XCELL Articles**
  - [Trouble-Free Switching Between Clocks](#)
  - [A Look at "Minimum" Delays](#)
  - [Power, Package, and Performance: Trading Off Among the Three P's](#)
  - [Metastability Recovery in Xilinx FPGAs](#)
  - [Using Decoupling Capacitors](#)
  - [Minimizing Power Consumption in FPGA Designs](#)
  - [Synchronous RAM Timing in the XC4000E FPGA](#)
  - [User-Defined Schmitt Triggers](#)
  - [Overshoot and Undershoot](#)
  - [Low-Pass Filtering of Noisy Inputs](#)
  - [Hold is a Four-Letter Word](#)



# XACTstep Software Applications

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- **Application Notes**
  - [Improving XC4000 Design Performance](#)
- **XCELL Articles**
  - [Released Software Status](#)
  - [Xilinx Alliance EDA Companies, Products, and Contacts](#)
  - [New XACTstep M1 Software for High-Density Designs](#)
  - [Technical Training Update - XACTstep M1 Course Available](#)
  - [Running XACTstep 5.2.1 in a Windows NT Environment](#)
  - [XACTstep and Alternate Operating Systems](#)
  - [Executing from the XACTstep CD-ROM](#)
  - [New XACTstep Release Adds XC4000E and XC9500 Family Support](#)
  - [Technical Q & A: Install, Design Manager/Flow Engine](#)

# XAPP Application Notes

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XAPP	Title	Design Files
XAPP004	<a href="#">Loadable Binary Counters</a>	Viewlogic OrCAD
XAPP005	<a href="#">Register-Based FIFO</a>	Viewlogic OrCAD
XAPP007	<a href="#">Boundary-Scan Emulator for XC3000</a>	Viewlogic OrCAD
XAPP009	<a href="#">Harmonic Frequency Synthesizer and FSK Modulator</a>	Viewlogic OrCAD
XAPP010	<a href="#">Bus-Structured Serial Input/Output Device</a>	
XAPP011	<a href="#">LCA Speed Estimation: Asking the Right Question</a>	
XAPP012	<a href="#">Quadrature Phase Detector</a>	
XAPP013	<a href="#">Using the Dedicated Carry Logic in XC4000E</a>	
XAPP014	<a href="#">Ultra-Fast Synchronous Counters</a>	Viewlogic OrCAD
XAPP015	<a href="#">Using the XC4000 Readback Capability</a>	
XAPP017	<a href="#">Boundary Scan in XC4000/XC5000 Devices</a>	
XAPP018	<a href="#">Estimating the Performance of XC4000E Adders and Counters</a>	
XAPP022	<a href="#">Adders, Subtractors and Accumulators in XC3000</a>	Viewlogic OrCAD
XAPP023	<a href="#">Accelerating Loadable Counters in XC4000</a>	Viewlogic OrCAD
XAPP026	<a href="#">Multiplexers and Barrel Shifters in XC3000/XC3100</a>	Viewlogic OrCAD
XAPP027	<a href="#">Implementing State Machines in LCA Devices</a>	
XAPP028	<a href="#">Frequency/Phase Comparator for Phase-Locked Loops</a>	Viewlogic OrCAD
	<a href="#">Continued...</a>	

# XAPP Application Notes

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XAPP	Title	Design Files
XAPP029	<a href="#">Serial Code Conversion between BCD and Binary</a>	Viewlogic OrCAD
XAPP030	<a href="#">Megabit FIFO in Two Chips: One LCA Device and One DRAM</a>	
XAPP043	<a href="#">Improving XC4000 Design Performance</a>	
XAPP051	<a href="#">Synchronous and Asynchronous FIFO Designs</a>	
XAPP052	<a href="#">Efficient Shift Registers, LFSR Counters, and Long Pseudo-Random Sequence Generators</a>	Viewlogic
XAPP053	<a href="#">Implementing FIFOs in XC4000 Series RAM</a>	
XAPP054	<a href="#">Constant Coefficient Multipliers for the XC4000E</a>	
XAPP055	<a href="#">Block Adaptive Filter</a>	
XAPP056	<a href="#">System Design with New XC4000EX I/O Features</a>	PC, SunOS, Solaris, HP
XAPP057	<a href="#">Using Select-RAM Memory in XC4000 Series FPGAs</a>	
XAPP058	<a href="#">XC9500 In-System Programming Using an 8051 Microcontroller</a>	
XAPP059	<a href="#">Gate Count Capacity Metrics for FPGAs</a>	
XAPP060	<a href="#">Design Migration from XC4000 to XC5200</a>	
XAPP061	<a href="#">Design Migration from XC2000/XC3000 to XC5200</a>	
XAPP062	<a href="#">Design Migration from XC4000 to XC4000E</a>	
XAPP063	<a href="#">Interfacing the XC6200 to a uP - Motorola MC68020 Example</a>	
XAPP064	<a href="#">Interfacing the XC6200 to uP - TMS320C50 Example</a>	
	<a href="#">Continued...</a>	

# XAPP Application Notes

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XAPP	Title	Design Files
XAPP065	<a href="#">XC4000 Series Edge-Triggered and Dual-Port RAM Capability</a>	
XAPP066	<a href="#">Design Migration with XC9500 CPLDs</a>	
XAPP067	<a href="#">Using Automatic Test Equipment to Program XC9500 Devices In-System</a>	
XAPP068	<a href="#">In-System Programming Times</a>	
XAPP069	<a href="#">Using the XC9500 JTAG Boundary-Scan Interface</a>	
XAPP070	<a href="#">Using In-System Programmability in Boundary-Scan Systems</a>	
XAPP071	<a href="#">Using the XC9500 Timing Model</a>	
XAPP072	<a href="#">XC9500 Design Optimization</a>	
XAPP073	<a href="#">Designing with XC9500 CPLDs</a>	
XAPP074	<a href="#">Pin Preassigning with XC9500 CPLDs</a>	
XAPP075	<a href="#">Using ABEL with Xilinx CPLDs</a>	
XAPP076	<a href="#">Embedded Instrumentation Using XC9500 CPLDs</a>	
XAPP077	<a href="#">Metastability Considerations</a>	
XAPP078	<a href="#">XC9536 Demo Board</a>	ABEL, VHDL
XAPP079	<a href="#">CPLD-Based 1Mbit Virtual SPROM Downloader for XC4000-Series FPGAs</a>	ABEL

# Xilinx Application Briefs

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Application Brief	Title
XBRF001	<a href="#"><u>XC4000E Select-RAM: Flexibility with Speed</u></a>
XBRF002	<a href="#"><u>XC4000E Low Power Consumption: At High Speeds</u></a>
XBRF003	<a href="#"><u>XC4000E Select-RAM: Maximum Configurability</u></a>
XBRF004	<a href="#"><u>PLDs, Pins, and PCBs: The Importance of Pin-Locking and Footprint Compatibility</u></a>
XBRF005	<a href="#"><u>XC4000EX Routing: A Comparison with XC4000E and ORCA</u></a>
XBRF006	<a href="#"><u>PLL Design Techniques and Usage in FPGA Design</u></a>
XBRF007	<a href="#"><u>XC4000-Series FPGAs: The Best Choice for Delivering Logic Cores</u></a>
XBRF009	<a href="#"><u>XC9500 Pin Locking Capability and Benchmarks</u></a>
XBRF010	<a href="#"><u>FastFLASH: A New Electrically Erasable CPLD Technology</u></a>
XBRF011	<a href="#"><u>An Alternative Capacity Metric for LUT-Based FPGAs</u></a>

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  - [Development Systems Products Overview](#)
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- CPLD Products
  - [XC9500 In-System Programmable CPLD Family](#)
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    - [XC7336/XC7336Q 36-Macrocell CMOS CPLD](#)
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    - [Addendum: XC4000E Switching Characteristics](#)
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  - XC5200 Series
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    - [Addendum: XC5202 Pinouts including VQ64 Package](#)
  - XC3000 Series
    - [XC3000 Series Field Programmable Gate Arrays](#)
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# Xilinx Data Book - Product Technical Information

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- [XC4000 Series Technical Information](#)
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- [FPGA Configuration Guidelines](#)
- [Configuring Mixed FPGA Daisy Chains](#)
- [Configuration Issues: Power-up, Volatility, Security, Battery Back-up](#)
- [Dynamic Reconfiguration](#)
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- [Set-up and Hold Times](#)
- [Overshoot and Undershoot](#)
- [Boundary Scan in XC4000 and XC5000 Series Devices](#)



# XCELL Journal

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- [XCELL 24](#): First Quarter, 1997
- [XCELL 23](#): Fourth Quarter, 1996
- [XCELL 22](#): Third Quarter, 1996
- [XCELL 21](#): Second Quarter, 1996
- [XCELL 20](#): First Quarter, 1996
- [XCELL 19](#): Fourth Quarter, 1995
- [XCELL 18](#): Third Quarter, 1995
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