

Features

- 10 ns pin-to-pin logic delays on all pins
- f_{CNT} to 111 MHz
- 216 macrocells with 4800 usable gates
- Up to 166 user I/O pins
- 5 V in-system programmable
 - Endurance of 10,000 program/erase cycles
 - Program/erase over full voltage and temperature range
- Enhanced pin-locking architecture
- Flexible 36V18 Function Block
 - 90 product terms drive any or all of 18 macrocells within Function Block
 - Global and product term clocks, output enables, set and reset signals
- Extensive IEEE Std 1149.1 boundary-scan (JTAG) support
- Programmable power reduction mode in each macrocell
- Slow rate control on individual outputs
- User programmable ground pin capability
- Extended pattern security features for design protection
- High-drive 24 mA outputs with 3.3 V or 5 V I/O capability
- PCI compliant (-10 speed grade)
- Advanced 0.6 μ m CMOS 5V FastFLASH technology
- Supports parallel programming of more than one XC9500 concurrently
- Available in 160-pin PQFP and 208-pin HQFP packages

Description

The XC95216 is a high-performance CPLD providing advanced in-system programming and test capabilities for general purpose logic integration. It is comprised of twelve 36V18 Function Blocks, providing 4,800 usable gates with propagation delays of 10 ns. See Figure 2 for the architecture overview.

Power Management

Power dissipation can be reduced in the XC95216 by configuring macrocells to standard or low-power modes of operation. Unused macrocells are turned off to minimize power dissipation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} (1.7) + MC_{LP} (0.9) + MC (0.006 \text{ mA/MHz}) f$$

Where:

MC_{HP} = Macrocells in high-performance mode

MC_{LP} = Macrocells in low-power mode

MC = Total number of macrocells used

f = Clock frequency (MHz)

Figure 1 shows a typical calculation for the XC95216 device.

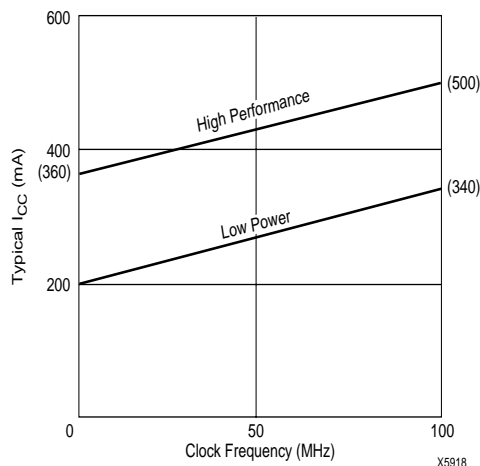


Figure 1: Typical I_{CC} vs. Frequency For XC95216

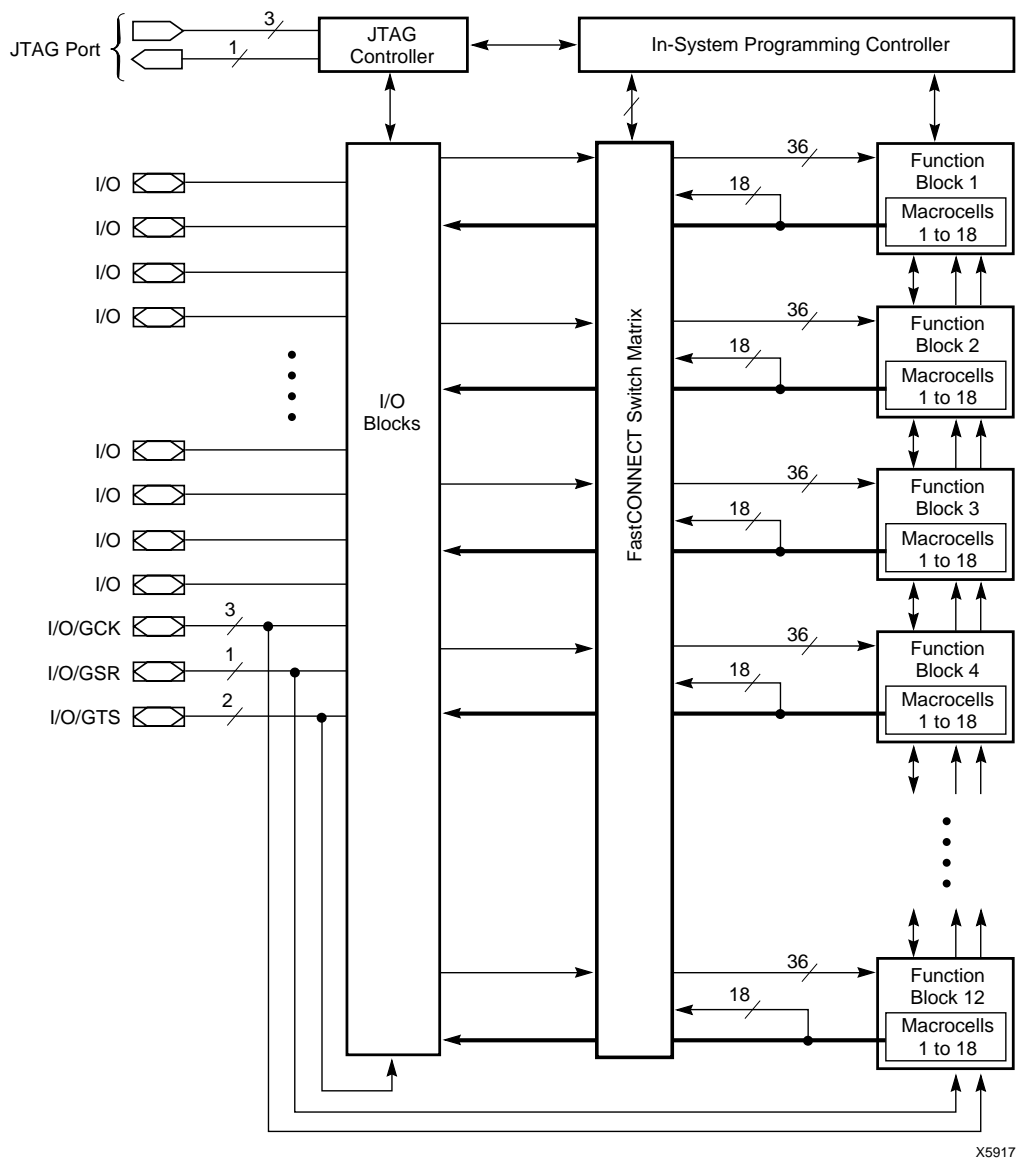


Figure 2: XC95216 Architecture

Function Block outputs (indicated by the bold line) drive the I/O Blocks directly

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage relative to GND	-0.5 to 7.0	V
V_{IN}	DC input voltage relative to GND	-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Max soldering temperature (10 ns @ 1/16 in = 1.5 mm)	+260	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Rating conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions¹

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage for internal logic and input buffer	4.75 (4.5)	5.25 (5.5)	V
V_{CCIO}	Supply voltage for output drivers for 5 V operation	4.75 (4.5)	5.25 (5.5)	V
	Supply voltage for output drivers for 3.3 V operation	3.0	3.6	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	$V_{CCINT} + 0.5$	V
V_O	Output voltage	0	$V_{CCINT} + 0.5$	V

Note: 1. Numbers in parenthesis are for industrial-temperature range versions.

Endurance Characteristics

Symbol	Parameter	Min	Max	Units
t_{DR}	Data Retention	20	-	Years
N_{PE}	Program/Erase Cycles	10,000	-	Cycles

DC Characteristics Over Recommended Operating Conditions

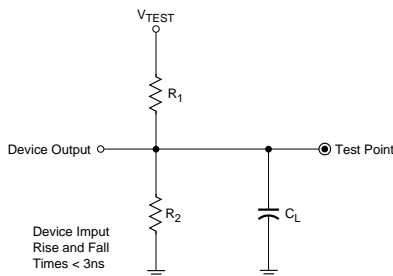
Symbol	Parameter	Test Conditions	Min	Max	Units
V_{OH}	Output high voltage for 5 V operation	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	Output high voltage for 3.3 V operation	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
V_{OL}	Output low voltage for 5 V operation	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	Output low voltage for 3.3 V operation	$I_{OL} = 10 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
I_{IL}	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		± 10.0	μA
I_{IH}	I/O high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CC}$		± 10.0	μA
C_{IN}	I/O capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
I_{CC}	Operating Supply Current (low power mode, active)	$V_I = \text{GND, No load}$ $f = 1.0 \text{ MHz}$	200 (typ)		ma

AC Characteristics

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	I/O to output valid		10.0		15.0		20.0	ns
t_{SU}	I/O setup time before GCK	6.5		8.0		10.0		ns
t_H	I/O hold time after GCK	0.0		0.0		0.0		ns
t_{CO}	GCK to output valid		6.5		8.0		10.0	ns
f_{CNT}^1	16-bit counter frequency	111		95		83		MHz
f_{SYSTEM}^2	Multiple FB internal operating frequency	67		56		50		MHz
t_{PSU}	I/O setup time before p-term clock input	2.5		4.0		4.0		ns
t_{PH}	I/O hold time after p-term clock input	4.0		4.0		6.0		ns
t_{PCO}	P-term clock to output valid		10.5		12.0		16.0	ns
t_{OE}	GTS to output valid		10.0		15.0		20.0	ns
t_{OD}	GTS to output disable		10.0		15.0		20.0	ns
t_{POE}	Product term OE to output enabled		15.5		18.0		22.0	ns
t_{POD}	Product term OE to output disabled		15.5		18.0		22.0	ns
t_{WLH}	GCK pulse width (High or Low)		4.5		5.5		5.5	ns

Preliminary

- Note:**
- f_{CNT} is the fastest 16-bit counter frequency available, using the local feedback when applicable.
 f_{CNT} is also the Export Control Maximum flip-flop toggle rate, f_{TOG} .
 - f_{SYSTEM} is the internal operating frequency for general purpose system designs spanning multiple FBs.



V_{CCIO} Level	V_{TEST}	R_1	R_1	C_L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 3: AC Load Circuit

Internal Timing Parameters

Symbol	Parameter	XC95216-10		XC95216-15		XC95216-20		Units
		Min	Max	Min	Max	Min	Max	
Buffer Delays								
t _{IN}	Input buffer delay		3.5		4.5		6.5	ns
t _{GCK}	GCK buffer delay		3.0		3.0		3.0	ns
t _{GSR}	GSR buffer delay		6.0		7.5		9.5	ns
t _{GTS}	GTS buffer delay		10.0		15.0		20.0	ns
t _{OUT}	Output buffer delay		3.0		4.5		6.5	ns
t _{EN}	Output buffer enable/disable delay		0.0		0.0		0.0	ns
Product Term Control Delays								
t _{PTCK}	Product term clock delay		3.5		2.5		2.5	ns
t _{PTSR}	Product term set/reset delay		2.5		3.0		3.0	ns
t _{PTTS}	Product term 3-state delay		12.0		13.5		15.5	ns
Internal Register and Combinatorial delays								
t _{PDI}	Combinatorial logic propagation delay		1.0		3.0		4.0	ns
t _{SUI}	Register setup time	3.5		3.5		3.5		ns
t _{HI}	Register hold time	3.0		4.5		6.5		ns
t _{COI}	Register clock to output valid time		0.5		0.5		0.5	ns
t _{AOI}	Register async. S/R to output delay		7.0		8.0		9.0	ns
t _{RAI}	Register async. S/R recovery before clock	10.0		15.0		20.0		ns
t _{LOGI}	Internal logic delay		2.5		3.0		3.0	ns
t _{LOGILP}	Internal low power logic delay		11.0		11.5		11.5	ns
Feedback Delays								
t _F	FastCONNECT matrix feedback delay		8.5		11.0		13.0	ns
t _{LF}	Function Block local feedback delay		2.5		3.5		5.0	ns
Time Adders								
t _{PTA} ³	Incremental Product Term Allocator delay		1.0		1.5		1.5	ns
t _{SLEW}	Slew-rate limited delay		4.5		5.0		5.5	ns

Preliminary

Note: 3. t_{PTA} is multiplied by the span of the function as defined in the family data sheet.

XC95216 I/O Pins

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
1	1	—	—	645	
1	2	18	22	642	
1	3	19	23	639	
1	4	—	28	636	
1	5	21	25	633	
1	6	22	30	630	
1	7	—	—	627	
1	8	23	31	624	
1	9	24	32	621	
1	10	—	12	618	
1	11	25	33	615	
1	12	26	34	612	
1	13	—	—	609	
1	14	27	35	606	
1	15	28	36	603	
1	16	29	37	600	
1	17	30	38	597	
1	18	—	—	594	
2	1	—	—	591	
2	2	6	7	588	[1]
2	3	7	8	585	
2	4	—	29	582	
2	5	8	9	579	[1]
2	6	9	10	576	
2	7	—	—	573	
2	8	11	15	570	
2	9	12	16	567	
2	10	—	-	564	
2	11	13	17	561	
2	12	14	18	558	
2	13	—	—	555	
2	14	15	19	552	
2	15	16	20	549	
2	16	—	14	546	
2	17	17	21	543	
2	18	—	—	540	
3	1	—	—	537	
3	2	32	43	534	
3	3	33	44	531	[1]
3	4	—	39	528	
3	5	34	45	525	
3	6	35	46	522	[1]
3	7	—	—	519	
3	8	36	47	516	
3	9	37	49	513	
3	10	—	67	510	
3	11	38	50	507	
3	12	39	51	504	
3	13	—	—	501	
3	14	42	55	498	[1]
3	15	43	56	495	
3	16	—	80	492	
3	17	44	57	489	
3	18	—	—	486	
4	1	—	—	483	
4	2	152	198	480	
4	3	153	199	477	
4	4	—	196	474	
4	5	154	200	471	
4	6	155	201	468	
4	7	—	—	465	
4	8	156	202	462	
4	9	158	205	459	
4	10	—	-	456	
4	11	159	206	453	[1]
4	12	2	3	450	[1]
4	13	—	—	447	
4	14	3	4	444	
4	15	4	5	441	[1]
4	16	—	203	438	
4	17	5	6	435	
4	18	—	—	432	

XC95216 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes	Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
5	1	—	—	429		7	1	—	—	321	
5	2	45	58	426		7	2	58	76	318	
5	3	47	60	423		7	3	59	77	315	
5	4	—	41	420		7	4	—	54	312	
5	5	48	61	417		7	5	60	78	309	
5	6	49	63	414		7	6	62	82	306	
5	7	—	—	411		7	7	—	—	303	
5	8	50	64	408		7	8	63	83	300	
5	9	52	70	405		7	9	64	84	297	
5	10	—	109	402		7	10	—	91	294	
5	11	53	71	399		7	11	65	85	291	
5	12	54	72	396		7	12	66	86	288	
5	13	—	—	393		7	13	—	—	285	
5	14	55	73	390		7	14	67	87	282	
5	15	56	74	387		7	15	68	88	279	
5	16	—	40	384		7	16	—	48	276	
5	17	57	75	381		7	17	69	89	273	
5	18	—	—	378		7	18	—	—	270	
6	1	—	—	375		8	1	—	—	267	
6	2	140	180	372		8	2	126	162	264	
6	3	142	182	369		8	3	128	164	261	
6	4	—	208	366		8	4	—	143	258	
6	5	143	185	363		8	5	129	166	255	
6	6	144	186	360		8	6	130	167	252	
6	7	—	—	357		8	7	—	—	249	
6	8	145	187	354		8	8	131	170	246	
6	9	146	188	351		8	9	132	171	243	
6	10	—	183	348		8	10	—	195	240	
6	11	147	191	345		8	11	133	173	237	
6	12	148	192	342		8	12	134	174	234	
6	13	—	—	339		8	13	—	—	231	
6	14	149	193	336		8	14	135	175	228	
6	15	150	194	333		8	15	138	178	225	
6	16	—	169	330		8	16	—	189	222	
6	17	151	197	327		8	17	139	179	219	
6	18	—	—	324		8	18	—	—	216	

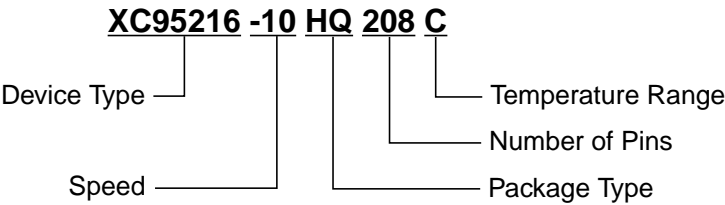
XC95216 I/O Pins (continued)

Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes	Function Block	Macrocell	PQ160	HQ208	BScan Order	Notes
9	1	—	—	213		11	1	—	—	105	
9	2	72	95	210		11	2	87	115	102	
9	3	74	97	207		11	3	88	116	99	
9	4	—	101	204		11	4	—	119	96	
9	5	76	99	201		11	5	89	117	93	
9	6	77	100	198		11	6	90	118	90	
9	7	—	—	195		11	7	—	—	87	
9	8	78	102	192		11	8	91	121	84	
9	9	79	103	189		11	9	92	122	81	
9	10	—	90	186		11	10	—	107	78	
9	11	82	110	183		11	11	93	123	75	
9	12	83	111	180		11	12	95	125	72	
9	13	—	—	177		11	13	—	—	69	
9	14	84	112	174		11	14	96	126	66	
9	15	85	113	171		11	15	97	127	63	
9	16	—	62	168		11	16	—	120	60	
9	17	86	114	165		11	17	98	128	57	
9	18	—	—	162		11	18	—	—	54	
10	1	—	—	159		12	1	—	—	51	
10	2	113	147	156		12	2	101	131	48	
10	3	114	148	153		12	3	102	133	45	
10	4	—	144	150		12	4	—	106	42	
10	5	115	149	147		12	5	103	134	39	
10	6	116	150	144		12	6	104	135	36	
10	7	—	—	141		12	7	—	—	33	
10	8	117	152	138		12	8	105	136	30	
10	9	118	154	135		12	9	106	137	27	
10	10	—	168	132		12	10	—	151	24	
10	11	119	155	129		12	11	107	138	21	
10	12	122	158	126		12	12	108	139	18	
10	13	—	—	123		12	13	—	—	15	
10	14	123	159	120		12	14	109	140	12	
10	15	124	160	117		12	15	111	145	9	
10	16	—	165	114		12	16	—	142	6	
10	17	125	161	111		12	17	112	146	3	
10	18	—	—	108		12	18	—	—	0	

XC95216 Global, JTAG and Power Pins

Pin Type	PQ160	HQ208
I/O/GCK1	33	44
I/O/GCK2	35	46
I/O/GCK3	42	55
I/O/GTS1	6	7
I/O/GTS2	8	9
I/O/GTS3	2	3
I/O/GTS4	4	5
I/O/GSR	159	206
TCK	75	98
TDI	71	94
TDO	136	176
TMS	73	96
V _{CCINT} 5 V	10,46,94,157	11, 59, 124, 153, 204
V _{CCIO} 3.3 V/5 V	1,41,61,81,121,141	1, 26, 53, 65, 79, 92, 105, 132, 157, 172, 181, 184
GND	20, 31, 40, 51, 70, 80, 99, 100, 110, 120, 127, 137, 160	2, 13, 24, 27, 42, 52, 66, 68, 69, 81, 93, 104, 108, 129, 130, 141, 156, 163, 177, 190, 207
No Connects	—	—

Ordering Information



Speed Options

- 20 20 ns pin-to-pin delay
- 15 15 ns pin-to-pin delay
- 10 10 ns pin-to-pin delay

Packaging Options

- PQ160 160-Pin Plastic Quad Flat Pack (PQFP)
- HQ208 208-Pin Heat Sink Quad Flat Pack (HQFP)

Temperature Options

- C Commercial 0°C to 70°C
- I Industrial -40°C to 85°C

Component Availability

Pins		160	160
Type		Plastic PQFP	Power QFP
Code		PQ160	HQ208
XC95216	-20	C(I)	C(I)
	-15	C	C
	-10	C	C

C = Commercial = 0° to +70°C I = Industrial = -40° to 85°C