

## Features

- High-performance Complex Programmable Logic Devices (CPLDs)
  - 7.5 ns pin-to-pin speeds on all fast inputs
  - Up to 125 MHz maximum clock frequency
- 100% PCI compliant
- 18 outputs with 24 mA drive
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V  $\pm 0.3$  V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- High-speed arithmetic carry network
  - 1 ns ripple-carry delay per bit
  - 61 MHz 18-bit accumulators
- Multiple independent clocks
- Up to 84 inputs programmable as direct, latched, or registered
- Power management options
- Multiple security bits for design protection
- 72 macrocells with programmable I/O architecture
- Advanced Dual-Block architecture
  - 2 Fast Function Blocks
  - 6 High-Density Function Blocks
- 0.8  $\mu$  CMOS EPROM technology
- Available in 68-pin and 84-pin PLCC/CLCC and 100-pin PQFP packages

## General Description

The XC7372 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks and six High Density Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™). See Figure 2 for the architecture overview.

## Power Management

The XC7372 features a power-management scheme that permits non-speed-critical paths of a design to be operated at reduced power. Overall power dissipation is often reduced significantly, since, in most systems only a few paths are speed critical.

Macrocells can individually be specified for high performance or low power operation by adding attributes to the logic schematic, or declaration statements to the behavioral description. To minimize power dissipation, unused Func-

tion Blocks are turned off and unused macrocells in used Function Blocks are configured for low power operation.

Operating current for each design can be approximated for specific operating conditions using the following equation:

$$I_{CC} \text{ (mA)} = MC_{HP} (3.1) + MC_{LP} (2.6) + MC (0.012 \text{ mA/MHz}) f$$

Where:

$MC_{HP}$  = Macrocells in high-performance mode  
 $MC_{LP}$  = Macrocells in low-power mode  
 $MC$  = Total number of macrocells used  
 $f$  = Clock frequency (MHz)

Figure 1 shows a typical power calculation for the XC7372 device, programmed as four 16-bit counters and operating at the indicated clock frequency.

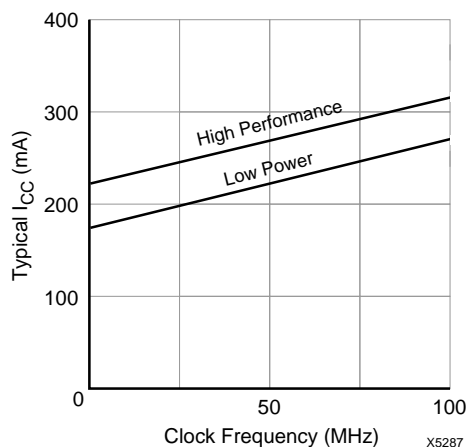


Figure 1: Typical  $I_{CC}$  vs. Frequency for XC7372

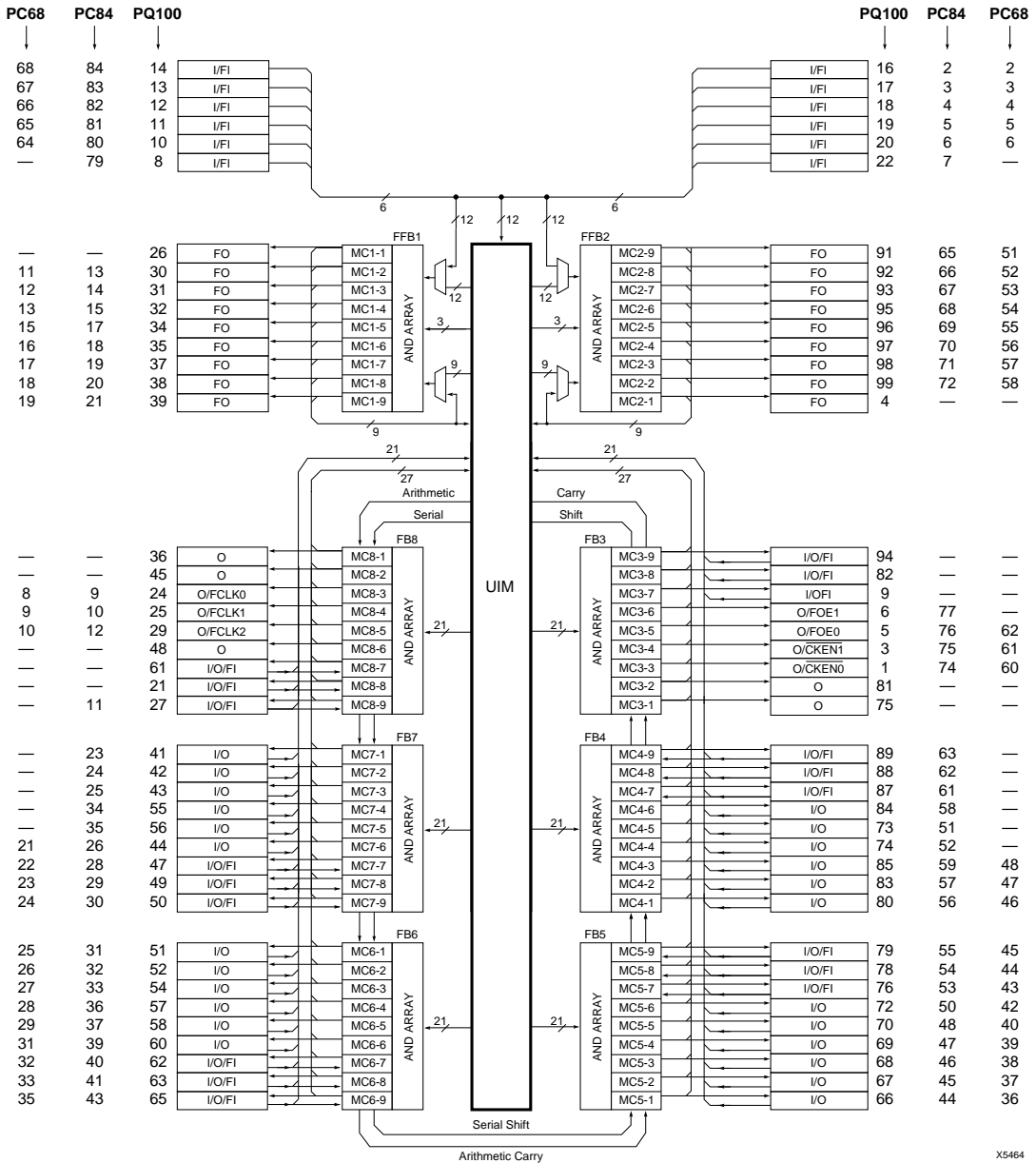


Figure 2: XC7372 Architecture

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage with respect to GND	-0.5 to 7.0	V
$V_{IN}$	DC Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

**Warning:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{CCINT}/V_{CCIO}$	Supply voltage relative to GND Commercial $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	4.75	5.25	V
	Supply voltage relative to GND Industrial $T_A = -40^{\circ}\text{C}$ to $85^{\circ}\text{C}$	4.5	5.5	V
	Supply voltage relative to GND Military $T_A = -55^{\circ}\text{C}$ to $T_C + 125^{\circ}\text{C}$	4.5	5.5	V
$V_{CCIO}$	I/O supply voltage relative to GND	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.8	V
$V_{IH}$	High-level input voltage	2.0	$V_{CC} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V
$T_{IN}$	Input signal transition time		50	ns

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	5 V TTL High-level output voltage	$I_{OH} = -4.0\text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	3.3 V High-level output voltage	$I_{OH} = -3.2\text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	5 V TTL Low-level output voltage	$I_{OL} = 24\text{ mA (FO)}$ $I_{OL} = 12\text{ mA (I/O)}$ $V_{CC} = \text{Min}$		0.5	V
	3.3 V Low-level output voltage	$I_{OL} = 10\text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CCIO}$		$\pm 10.0$	$\mu\text{A}$
$I_{OZ}$	Output high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CCIO}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	Input capacitance for Input and I/O pins	$V_{IN} = \text{GND}$ $f = 1.0\text{ MHz}$		8.0	pF
$C_{IN}$	Input capacitance for global control pins (FCLK0, FCLK1, FCLK2, FOE0, FOE1)	$V_{IN} = \text{GND}$ $f = 1.0\text{ MHz}$		12.0	pF
$C_{OUT}^1$	Output capacitance	$V_{IN} = \text{GND}$ $f = 1.0\text{ MHz}$		10.0	pF
$I_{CC}^2$	Supply current (low power mode)	$V_{IN} = V_{CC}$ or GND $V_{CCINT} = V_{CCIO} = 5\text{ V}$ $f = 1.0\text{ MHz @ } 25^{\circ}\text{C}$	187 Typ		mA

**Notes:** 1. Sample tested.  
2. Measured with device programmed as four 16-bit counters.

## Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
$t_{WMR}$	Master Reset input Low pulse width	100			ns
$t_{RESET}$	Configuration completion time		80	160	$\mu$ s

## Fast Function Block (FFB) External AC Characteristics<sup>3</sup>

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$f_{CF}$	Max count frequency <sup>1, 2, 4</sup>	125.0		100.0		80.0		66.7		MHz
$t_{SUF}$	Fast input setup time before FCLK $\uparrow$ <sup>1</sup>	4.0		5.0		6.0		7.0		ns
$t_{HF}$	Fast input hold time after FCLK $\uparrow$	0		0		0		0		ns
$t_{COF}$	FCLK $\uparrow$ to output valid		5.5		8.0		9.0		12.0	ns
$t_{PFO}$	Fast input to output valid <sup>1, 2</sup>		7.5		10.0		12.0		15.0	ns
$t_{PDFU}$	I/O to output valid <sup>1, 2</sup>		14.0		17.0		20.0		24.0	ns
$t_{CWF}$	Fast clock pulse width (High or Low)	4.0		5.0		5.5		6.0		ns

- Notes:**
1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of  $t_{FLOGILP} - t_{FLOGI}$  or  $t_{LOGILP} - t_{LOGI}$ .
  2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.
  3. All appropriate specifications tested using Figure 3 as the test load circuit.
  4. Export Control Max. flip-flop toggle rate.

## High-Density Function Block (FB) External AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
$f_C$	Max count frequency <sup>1, 2</sup>	95.2		71.4		62.5		52.6		MHz
$t_{SU}$	I/O setup time before FCLK $\uparrow$ <sup>1, 2</sup>	12.5		14.0		16.0		19.0		ns
$t_H$	I/O hold time after FCLK $\uparrow$	0		0		0		0		ns
$t_{CO}$	FCLK $\uparrow$ to output valid		7.0		10.0		12.0		15.0	ns
$t_{PSU}$	I/O setup time before p-term clock $\uparrow$ <sup>2</sup>	6.0		6.0		7.0		9.0		ns
$t_{PH}$	I/O hold time after p-term clock $\uparrow$	0		0		0		0		ns
$t_{PCO}$	P-term clock $\uparrow$ to output valid		13.5		18.0		21.0		25.0	ns
$t_{PD}$	I/O to output valid <sup>1, 2</sup>		18.5		23.0		28.0		33.0	ns
$t_{CW}$	Fast clock pulse width	4.0		5.0		5.5		6.0		ns
$t_{PCW}$	P-term clock pulse width	5.0		6.0		7.5		8.5		ns

- Notes:**
1. This parameter is given for the high-performance mode. In low-power mode, this parameter is increased due to additional logic delay of  $t_{FLOGILP} - t_{FLOGI}$  or  $t_{LOGILP} - t_{LOGI}$ .
  2. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

## Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>FLOGI</sub>	FFB logic array delay <sup>1</sup>		1.5		1.5		2.0		2.0	ns
t <sub>FLOGILP</sub>	Low-power FFB logic array delay <sup>1</sup>		3.5		5.5		7.0		8.0	ns
t <sub>FSUI</sub>	FFB register setup time	1.5		2.5		3.0		4.0		ns
t <sub>FHI</sub>	FFB register hold time	2.5		2.5		3.0		3.0		ns
t <sub>FCOI</sub>	FFB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t <sub>FPDI</sub>	FFB register pass through delay		0.5		0.5		1.0		1.0	ns
t <sub>FAOI</sub>	FFB register async. set delay		2.0		2.5		3.0		4.0	ns
t <sub>PTXI</sub>	FFB p-term assignment delay		0.8		1.0		1.2		1.5	ns
t <sub>FFD</sub>	FFB feedback delay		4.0		5.0		6.5		8.0	ns

**Note:** 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

## High-Density Function Block (FB) Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>LOGI</sub>	FB logic array delay <sup>1</sup>		3.5		3.5		4.0		5.0	ns
t <sub>LOGILP</sub>	Low power FB logic delay <sup>1</sup>		7.0		7.5		9.0		11.0	ns
t <sub>SUI</sub>	FB register setup time	1.5		2.5		3.0		4.0		ns
t <sub>HI</sub>	FB register hold time	3.5		3.5		4.0		5.0		ns
t <sub>COI</sub>	FB register clock-to-output delay		1.0		1.0		1.0		1.0	ns
t <sub>PDI</sub>	FB register pass through delay		1.5		2.5		4.0		4.0	ns
t <sub>AOI</sub>	FB register async. set/reset delay		2.5		3.0		4.0		5.0	ns
t <sub>RA</sub>	Set/reset recovery time before FCLK <sup>↑</sup>	13.5		17.0		19.0		22.0		ns
t <sub>HA</sub>	Set/reset hold time after FCLK <sup>↑</sup>	0		0		0		0		ns
t <sub>PRA</sub>	Set/reset recovery time before p-term clock <sup>↑</sup>	7.5		10.0		12.0		15.0		ns
t <sub>PHA</sub>	Set/reset hold time after p-term clock <sup>↑</sup>	5.0		6.0		8.0		9.0		ns
t <sub>PCI</sub>	FB p-term clock delay		1.0		0		0		0	ns
t <sub>OEI</sub>	FB p-term output enable delay		3.0		4.0		5.0		7.0	ns
t <sub>CARY8</sub>	ALU carry delay within 1 FB <sup>2</sup>		5.0		6.0		8.0		12.0	ns
t <sub>CARYFB</sub>	Carry lookahead delay per additional Functional Block <sup>2</sup>		1.0		1.5		2.0		3.0	ns

**Notes:** 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.  
2. Arithmetic carry delays are measured as the increase in required set-up time to adjacent macrocell(s) for adder with registered outputs.

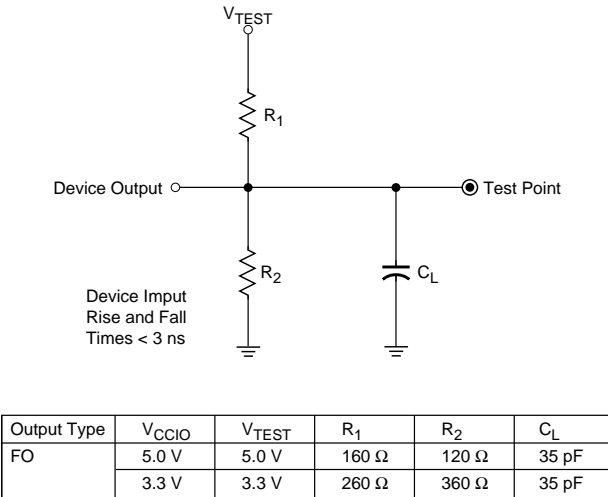
I/O Block External AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
f <sub>IN</sub>	Max pipeline frequency (input register to FFB or FB register) <sup>1</sup>	95.2		71.4		62.5		52.6		MHz
t <sub>SUIN</sub>	Input register/latch setup time before FCLK ↑	4.0		5.0		6.0		7.0		ns
t <sub>HIN</sub>	Input register/latch hold time after FCLK ↑	0		0		0		0		ns
t <sub>COIN</sub>	FCLK ↑ to input register/latch output		2.5		3.5		4.0		5.0	ns
t <sub>CESUIN</sub>	Clock enable setup time before FCLK ↑	5.0		7.0		8.0		10.0		ns
t <sub>CEHIN</sub>	Clock enable hold time after FCLK ↑	0		0		0		0		ns
t <sub>CWHIN</sub>	FCLK pulse width high time	4.0		5.0		5.5		6.0		ns
t <sub>CWLIN</sub>	FCLK pulse width low time	4.0		5.0		5.5		6.0		ns

**Note:** 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC7372-7 (Com only)		XC7372-10 (Com/Ind only)		XC7372-12		XC7372-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>IN</sub>	Input pad and buffer delay		2.5		3.5		4.0		5.0	ns
t <sub>FOUT</sub>	FFB output buffer and pad delay		3.0		4.5		5.0		7.0	ns
t <sub>OUT</sub>	FB output buffer and pad delay		4.5		6.5		8.0		10.0	ns
t <sub>UIM</sub>	Universal Interconnect Matrix delay		6.5		7.0		8.0		9.0	ns
t <sub>FOE</sub>	FOE input to output valid		7.5		10.0		12.0		15.0	ns
t <sub>FOD</sub>	FOE input to output disable		7.5		10.0		12.0		15.0	ns
t <sub>FCLKI</sub>	Fast clock buffer delay		1.5		2.5		3.0		4.0	ns



X3491

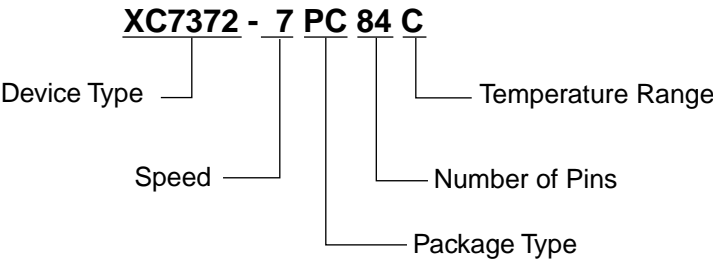
Figure 3: AC Load Circuit

## XC7372 Pinouts

PQ100	PC84	PC68	Input	XC7372	Output
15	1	1		MR	
16	2	2	I/FI		
17	3	3	I/FI		
18	4	4	I/FI		
19	5	5	I/FI		
20	6	6	I/FI		
21	–	–	I/O/FI		MC8-8
22	7	–	I/FI		
23	8	7		GND	
24	9	8	O/FCLK0		MC8-3
25	10	9	O/FCLK1		MC8-4
26	–	–	FO		MC1-1
27	11	–	I/O/FI		MC8-9
28	–	–		V <sub>CCIO</sub>	
29	12	10	O/FCLK2		MC8-5
30	13	11	FO		MC1-2
31	14	12	FO		MC1-3
32	15	13	FO		MC1-4
33	16	14		GND	
34	17	15	FO		MC1-5
35	18	16	FO		MC1-6
36	–	–	O		MC8-1
37	19	17	FO		MC1-7
38	20	18	FO		MC1-8
39	21	19	FO		MC1-9
40	22	20		V <sub>CCIO</sub>	
41	23	–	I/O		MC7-1
42	24	–	I/O		MC7-2
43	25	–	I/O		MC7-3
44	26	21	I/O		MC7-6
45	–	–	O		MC8-2
46	27	–		GND	
47	28	22	I/O/FI		MC7-7
48	–	–	O		MC8-6
49	29	23	I/O/FI		MC7-8
50	30	24	I/O/FI		MC7-9
51	31	25	I/O		MC6-1
52	32	26	I/O		MC6-2
53	–	–		V <sub>CCIO</sub>	
54	33	27	I/O		MC6-3
55	34	–	I/O		MC7-4
56	35	–	I/O		MC7-5
57	36	28	I/O		MC6-4
58	37	29	I/O		MC6-5
59	38	30		V <sub>CCINT</sub>	
60	39	31	I/O		MC6-6
61	–	–	I/O/FI		MC8-7
62	40	32	I/O/FI		MC6-7
63	41	33	I/O/FI		MC6-8
64	42	34		GND	

PQ100	PC84	PC68	Input	XC7372	Output
65	43	35	I/O/FI		MC6-9
66	44	36	I/O		MC5-1
67	45	37	I/O		MC5-2
68	46	38	I/O		MC5-3
69	47	39	I/O		MC5-4
70	48	40	I/O		MC5-5
71	49	41		GND	
72	50	42	I/O		MC5-6
73	51	–	I/O		MC4-5
74	52	–	I/O		MC4-4
75	–	–	O		MC3-1
76	53	43	I/O/FI		MC5-7
77	–	–		GND	
78	54	44	I/O/FI		MC5-8
79	55	45	I/O/FI		MC5-9
80	56	46	I/O		MC4-1
81	–	–	O		MC3-2
82	–	–	I/O/FI		MC3-8
83	57	47	I/O		MC4-2
84	58	–	I/O		MC4-6
85	59	48	I/O		MC4-3
86	60	49		GND	
87	61	–	I/O/FI		MC4-7
88	62	–	I/O/FI		MC4-8
89	63	–	I/O/FI		MC4-9
90	64	50		V <sub>CCIO</sub>	
91	65	51	FO		MC2-9
92	66	52	FO		MC2-8
93	67	53	FO		MC2-7
94	–	–	I/O/FI		MC3-9
95	68	54	FO		MC2-6
96	69	55	FO		MC2-5
97	70	56	FO		MC2-4
98	71	57	FO		MC2-3
99	72	58	FO		MC2-2
100	73	59		V <sub>CCINT</sub>	
1	74	60	O/CKEN <sub>0</sub>		MC3-3
2	–	–		GND	
3	75	61	O/CKEN <sub>1</sub>		MC3-4
4	–	–	FO		MC2-1
5	76	62	O/FOE <sub>0</sub>		MC3-5
6	77	–	O/FOE <sub>1</sub>		MC3-6
7	78	63		V <sub>CCINT</sub> / V <sub>PP</sub>	
8	79	–	I/FI		
9	–	–	I/O/FI		MC3-7
10	80	64	I/FI		
11	81	65	I/FI		
12	82	66	I/FI		
13	83	67	I/FI		
14	84	68	I/FI		

Ordering Information



Speed Options

- 15      15 ns pin-to-pin delay
- 12      12 ns pin-to-pin delay
- 10      10 ns pin-to-pin delay (commercial and industrial only)
- 7        7.5 ns pin-to-pin delay (commercial only)

Packaging Options

- PC68     68-Pin Plastic Leaded Chip Carrier
- WC68     68-Pin Windowed Ceramic Leaded Chip Carrier
- PC84     84-Pin Plastic Leaded Chip Carrier
- WC84     84-Pin Windowed Ceramic Leaded Chip Carrier
- PQ100    100-Pin Plastic Quad Flat Pack

Temperature Options

- C        Commercial 0°C to 70°C
- I        Industrial -40°C to 85°C
- M        Military -55°C (Ambient) to 125°C (Case)

Component Availability

Pins		68		84		100
Type		Plastic PLCC	Ceramic CLCC	Plastic PLCC	Ceramic CLCC	Plastic PQFP
Code		PC68	WC68	PC84	WC84	PQ100
XC7372	-15	CI	CIM	CI	CIM	CI
	-12	CI	CIM	CI	CI	CI
	-10	CI	CI	CI	CI	CI
	-7	C	C	C	C	C

C = Commercial = 0° to +70°C      I = Industrial = -40° to 85°C      M = Military = -55°C(A) to 125°C (C)