

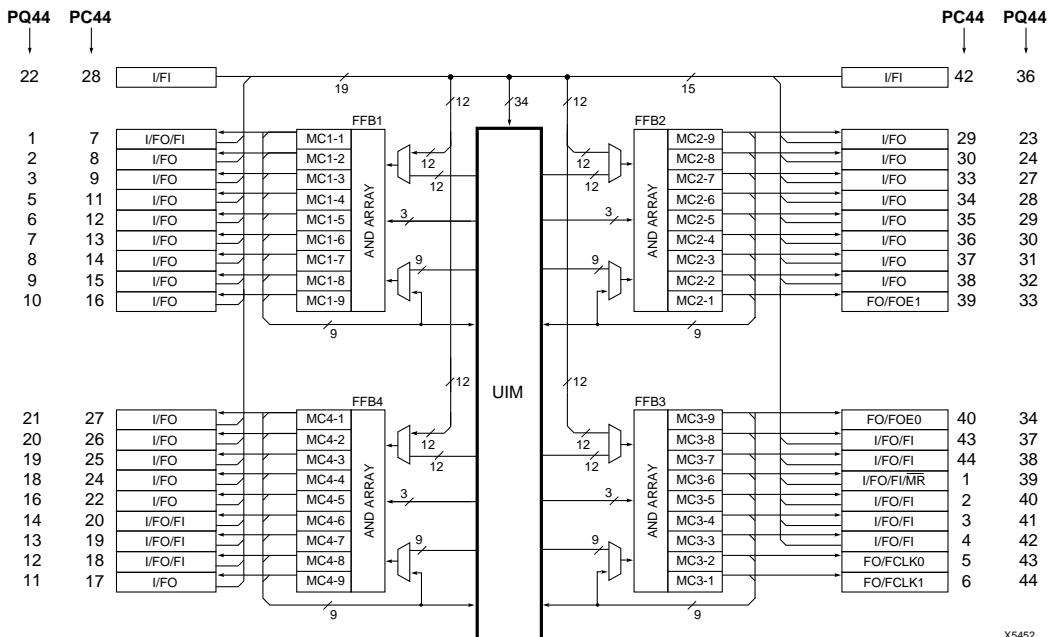
Features

- Ultra high-performance Complex Programmable Logic Devices (CPLDs)
 - 5 ns pin-to-pin speeds on all fast inputs
 - Up to 167 MHz maximum clock frequency
- New low power XC7336Q
- 100% PCI compliant
- High-drive 24 mA output
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V ± 0.3 V
- 100% interconnect matrix
 - Maximizes resource utilization
 - Wire-AND capability via SMARTswitch
- Multiple security bits for design protection
- Incorporates four PAL-like 24V9 Fast Function Blocks
- 0.8 μ CMOS EPROM technology
- Available in 44-pin VQFP, PQFP and PLCC/CLCC packages

General Description

The XC7336 is a high performance CPLD providing general purpose logic integration. It consists of four PAL-like 24V9 Fast Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™). See [Figure 1](#) for the architecture overview.

The XC7336 is designed in 0.8 μ CMOS EPROM technology, in speed grades ranging from 5 to 15 ns. The XC7336Q is also available now, providing lower power consumption in -10, -12 and -15 ns speed grades.



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Figure 1: XC7336 Architecture

Power Estimation

Figure 2 shows a typical power estimation for the XC7336 and the XC7336Q device, programmed as two 16-bit counters and operating at the indicated clock frequency.

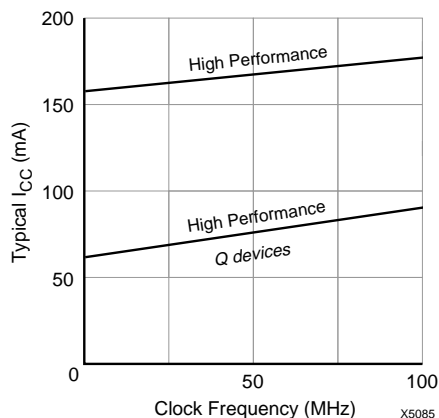


Figure 2: Typical I_{CC} vs. Frequency for XC7336

Absolute Maximum Ratings

Symbol	Parameter	Value	Units
V_{CC}	Supply voltage with respect to GND	-0.5 to 7.0	V
V_{IN}	DC Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+250	°C

Warning: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CCINT}	Supply voltage relative to GND Commercial $T_A = 0^{\circ}\text{C}$ to 70°C	4.75	5.25	V
V_{CCIO}	Supply voltage relative to GND Industrial $T_A = -40^{\circ}\text{C}$ to 85°C	4.50	5.50	V
V_{CCIO}	I/O supply voltage relative to GND	3.0	3.60	V
V_{IL}	Low-level input voltage	0	0.80	V
V_{IH}	High-level input voltage	2.0	$V_{CC} + 0.5$	V
V_O	Output voltage	0	V_{CCIO}	V
T_{IN}	Input signal transition time		50	ns

DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter		Test Conditions	Min	Max	Units
V _{OH}	5 V TTL High-level output voltage		I _{OH} = -4.0 mA V _{CC} = Min	2.4		V
	3.3 V High-level output voltage		I _{OH} = -3.2 mA V _{CC} = Min	2.4		V
V _{OL}	5 V TTL Low-level output voltage		I _{OL} = 24 mA V _{CC} = Min		0.5	V
	3.3 V Low-level output voltage		I _{OL} = 24 mA V _{CC} = Min		0.4	V
I _{IL}	Input leakage current		V _{CC} = Max V _{IN} = GND or V _{CCIO}		±10.0	μA
I _{OZ}	Output high-Z leakage current		V _{CC} = Max V _{IN} = GND or V _{CCIO}		±10.0	μA
C _{IN}	Input capacitance for Input and I/O pins		V _{IN} = GND f = 1.0 MHz		6.0	pF
C _{IN}	Input capacitance for global control pins (FCLK0, FCLK1, FOE0, FOE1)		V _{IN} = GND f = 1.0 MHz		8.0	pF
C _{IN}	Input capacitance for Fast Inputs		V _{IN} = GND f = 1.0 MHz		12.0	pF
C _{OUT} ¹	Output capacitance		V _{IN} = GND f = 1.0 MHz		10.0	pF
I _{CC} ²	Supply current	(Non Q)	V _{IN} = V _{CC} or GND V _{CCINT} = V _{CCIO} = 5V	126 Typ		mA
		(Q)	f = 1.0 MHz @ 25°C	55 Typ		

Notes: 1. Sample tested.
2. Measured with device programmed as two 16-bit counters.

Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
t_{WMR}	Master Reset input Low pulse width	100			ns
t_{RESET}	Configuration completion time		80	160	μs

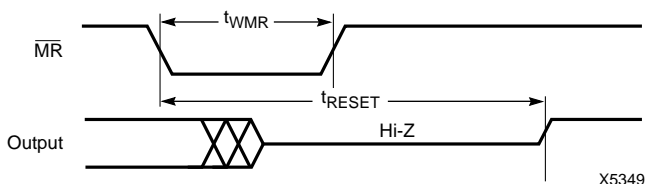


Figure 3: Global Reset Waveform

Fast Function Block (FFB) External AC Characteristics ¹

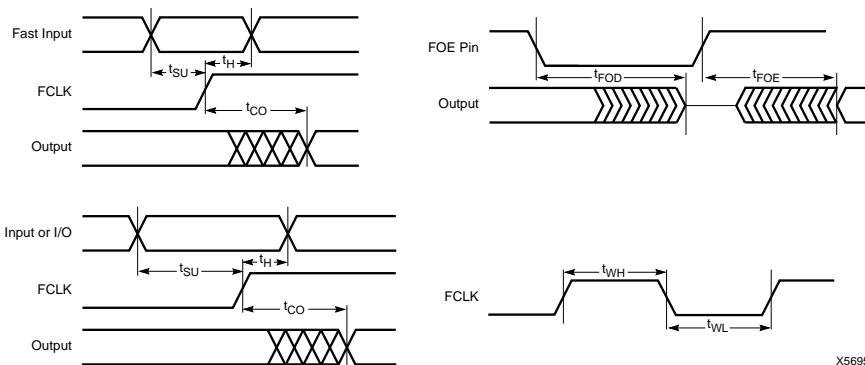
Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t_{PD}	Fast input to output valid ²		5.0		7.5		10.0		12.0		15.0	ns
	I/O or input to output valid ²		8.5		12.0		15.0		19.0		23.0	ns
t_{SU}	Fast input setup time before FCLK	4.5		5.0		5.0		6.0		7.0		ns
	I/O or input setup time before FCLK	7.0		8.5		10.0		13.0		15.0		ns
t_H	Fast, I/O or input hold time after FCLK	0		0		0		0		0		ns
t_{CO}	FCLK input to output valid		4.5		4.5		8.0		9.0		12.0	ns
t_{FOE}	FOE input to output valid		7.0		7.5		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		7.0		7.5		10.0		12.0		15.0	ns
f_{MAX}	Max count frequency ^{2,3}	167.0		125.0		100.0		80.0		66.7		MHz
t_{WLH}	Fast Clock pulse width (High or Low)	3.0		4.0		5.0		5.5		6.0		ns

Symbol	Parameter	XC7336Q-10		XC7336Q-12		XC7336Q-15		Units
		Min	Max	Min	Max	Min	Max	
t_{PD}	Fast input to output valid ²		10.0		12.0		15.0	ns
	I/O or input to output valid ²		15.0		19.0		23.0	ns
t_{SU}	Fast input setup time before FCLK	6.5		6.5		7.0		ns
	I/O or input setup time before FCLK	11.5		13.5		15.0		ns
t_H	Fast, I/O or input hold time after FCLK	0		0		0		ns
t_{CO}	FCLK input to output valid		6.5		8.5		12.0	ns
t_{FOE}	FOE input to output valid		10.0		12.0		15.0	ns
t_{FOD}	FOE input to output disable		10.0		12.0		15.0	ns
f_{MAX}	Max count frequency ^{2,3}	100.0		80.0		66.7		MHz
t_{WLH}	Fast Clock pulse width (High or Low)	5.0		5.5		6.0		ns

Notes: 1. All appropriate ac specifications tested using Figure 5 as test load circuit.

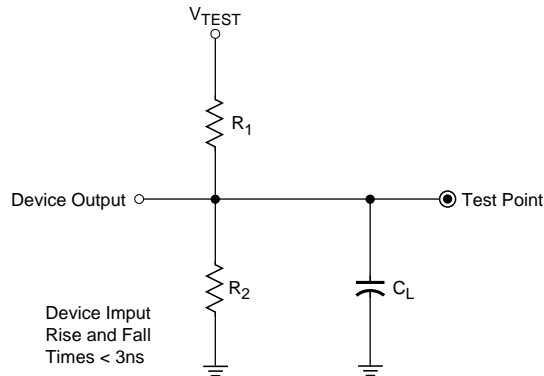
2. Assumes four product terms per output.

3. Export Control Max. flip-flop toggle rate.



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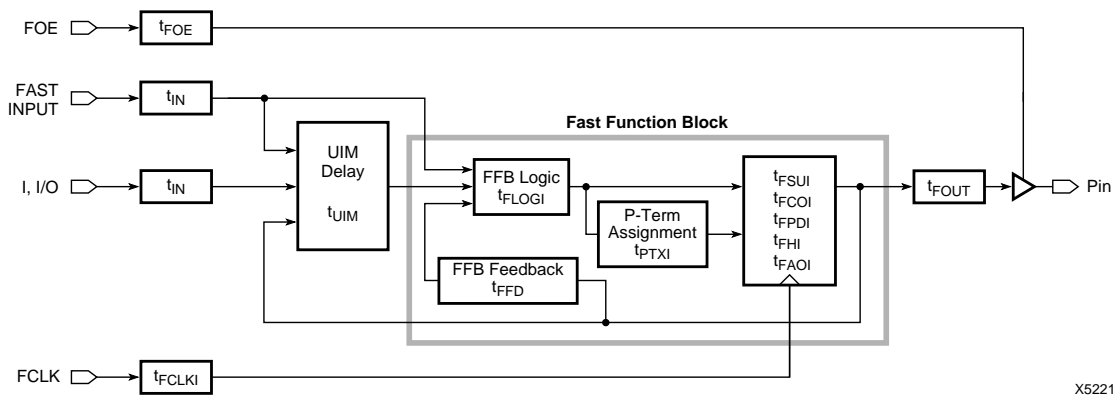
Figure 4: Switching Waveform



V_{CCIO} Level	V_{TEST}	R_1	R_1	C_L
5 V	5.0 V	160 Ω	120 Ω	35 pF
3.3 V	3.3 V	260 Ω	360 Ω	35 pF

X5222

Figure 5: AC Load Circuit



X5221

Figure 6: XC7336 Timing Model

Timing Model

Timing within the XC7336 is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in [Figure 6](#).

The timing model is based on the fixed internal delays of the XC7336 architecture that consists of three basic parts:

I/O Blocks, the UIM and Fast Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for the XC7336.

Fast Function Block (FFB) Internal AC Characteristics

Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{FLOGI}	FFB logic array delay ¹		1.0		1.5		1.5		2.0		2.0	ns
t _{FLOGILP}	Low-power FFB logic array delay ¹		2.0		3.5		5.5		7.0		8.0	ns
t _{FSUI}	FFB register setup time	2.5		1.5		2.5		3.0		4.0		ns
t _{FHI}	FFB register hold time	1.0		2.5		2.5		3.0		3.0		ns
t _{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0		1.0		1.0	ns
t _{FPDI}	FFB register pass through delay		0.5		0.5		0.5		1.0		1.0	ns
t _{FAOI}	FFB register async. set delay		2.0		2.0		2.5		3.0		4.0	ns
t _{PTXI}	FFB p-term assignment delay		0.6		0.8		1.0		1.2		1.5	ns
t _{FFD}	FFB feedback delay		0.5		4.0		5.0		6.5		8.0	ns

Symbol	Parameter	XC7336Q-10		XC7336Q-12		XC7336Q-15		Units
		Min	Max	Min	Max	Min	Max	
t _{FLOGI}	FFB logic array delay ¹		3.0		3.0		2.0	ns
t _{FLOGILP}	Low-power FFB logic array delay ¹		5.5		7.0		8.0	ns
t _{FSUI}	FFB register setup time	2.5		3.0		4.0		ns
t _{FHI}	FFB register hold time	2.5		3.0		3.0		ns
t _{FCOI}	FFB register clock-to-output delay		1.0		1.0		1.0	ns
t _{FPDI}	FFB register pass through delay		0.5		1.0		1.0	ns
t _{FAOI}	FFB register async. set delay		2.5		3.0		4.0	ns
t _{PTXI}	FFB p-term assignment delay		1.0		1.2		1.5	ns
t _{FFD}	FFB feedback delay		5.0		6.5		8.0	ns

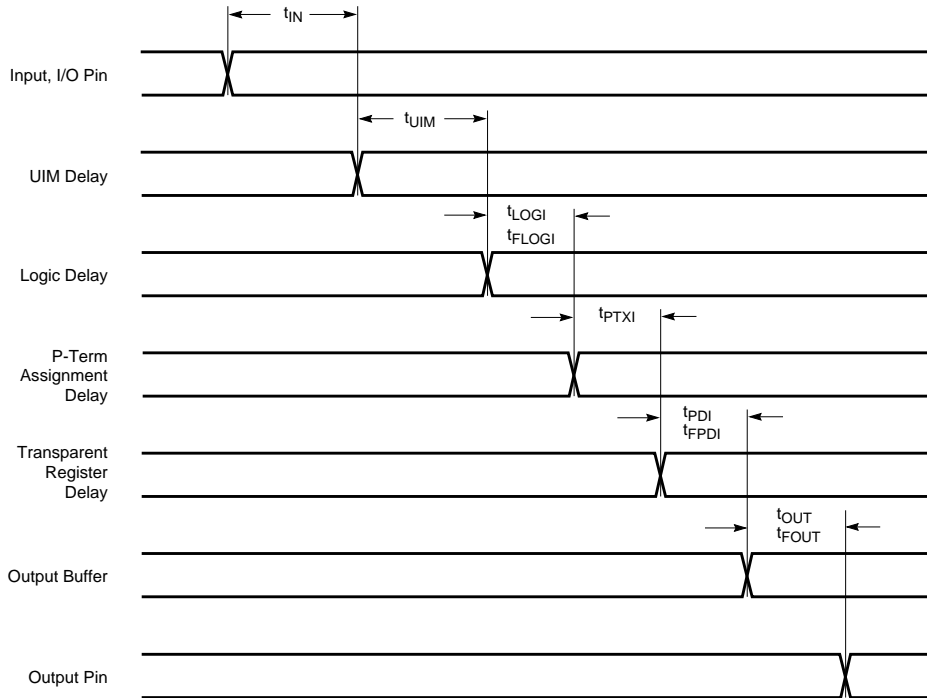
Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given macrocell.

Internal AC Characteristics

Symbol	Parameter	XC7336-5		XC7336-7		XC7336-10		XC7336-12		XC7336-15		Units
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay		1.5		2.5		3.5		4.0		5.0	ns
t _{FOUT}	FFB output buffer and pad delay		2.0		3.0		4.5		5.0		7.0	ns
t _{UIM}	Universal Interconnect Matrix delay		3.5		4.5		5.0		7.0		8.0	ns
t _{FCLKI}	Fast clock buffer delay		1.5		1.5		2.5		3.0		4.0	ns

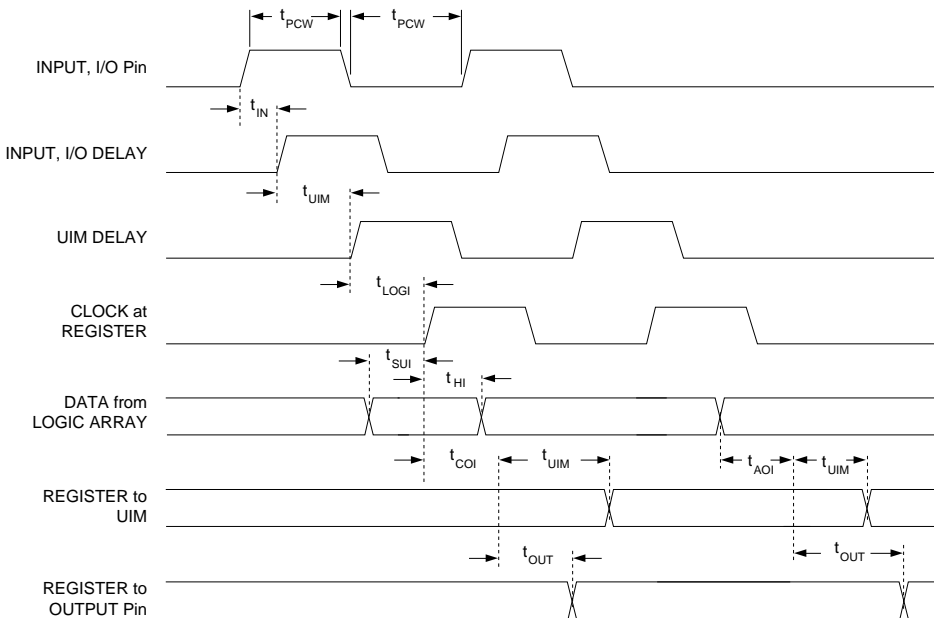
Symbol	Parameter	XC7336Q-10		XC7336Q-12		XC7336Q-15		Units
		Min	Max	Min	Max	Min	Max	
t _{IN}	Input pad and buffer delay		3.5		4.0		5.0	ns
t _{FOUT}	FFB output buffer and pad delay		3.0		4.5		7.0	ns
t _{UIM}	Universal Interconnect Matrix delay		5.0		7.0		8.0	ns
t _{FCLKI}	Fast clock buffer delay		2.5		3.0		4.0	ns

Combinational Switching Characteristics



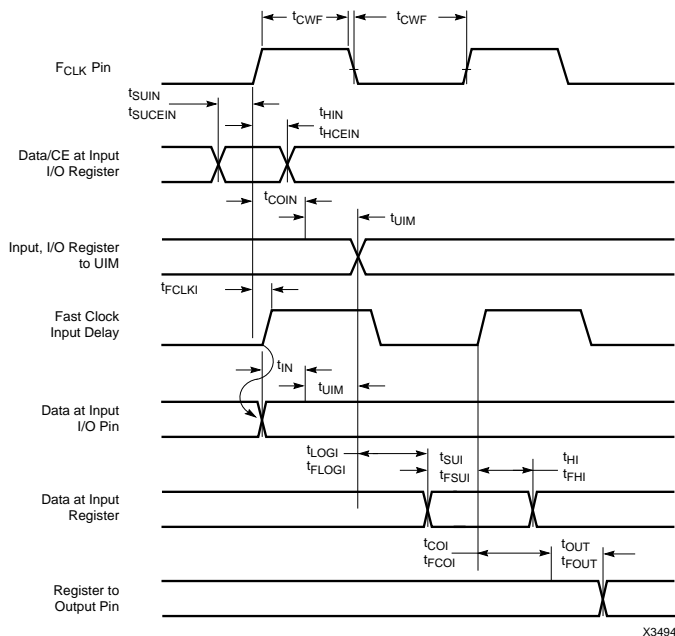
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Asynchronous Switching Characteristics



X3580

Synchronous Switching Characteristics

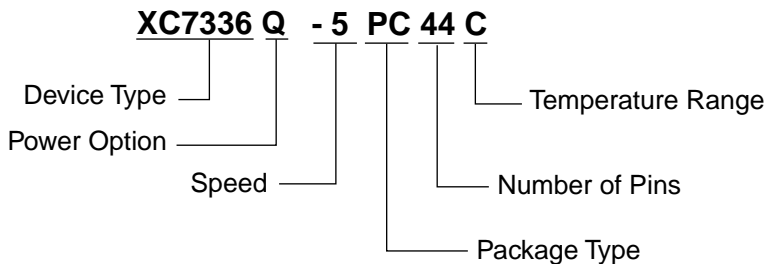


XC7336 Pinouts

VQ44/PQ44	PC44	Input	XC7336	Output
39	1	I/FO/FI	\overline{MR}	MC3-6
40	2	I/FO/FI		MC3-5
41	3	I/FO/FI		MC3-4
42	4	I/FO/FI		MC3-3
43	5	FO/FCLK0		MC3-2
44	6	FO/FCLK1		MC3-1
1	7	I/FO/FI		MC1-1
2	8	I/FO		MC1-2
3	9	I/FO		MC1-3
4	10		GND	
5	11	I/FO		MC1-4
6	12	I/FO		MC1-5
7	13	I/FO		MC1-6
8	14	I/FO		MC1-7
9	15	I/FO		MC1-8
10	16	I/FO		MC1-9
11	17	I/FO		MC4-9
12	18	I/FO/FI		MC4-8
13	19	I/FO/FI		MC4-7
14	20	I/FO/FI		MC4-6
15	21		V_{CCINT}	
16	22	I/FO		MC4-5

VQ44/PQ44	PC44	Input	XC7336	Output
17	23		GND	
18	24	I/FO		MC4-4
19	25	I/FO		MC4-3
20	26	I/FO		MC4-2
21	27	I/FO		MC4-1
22	28	I/FI		
23	29	I/FO		MC2-9
24	30	I/FO		MC2-8
25	31		GND	
26	32		V_{CCIO}	
27	33	I/FO		MC2-7
28	34	I/FO		MC2-6
29	35	I/FO		MC2-5
30	36	I/FO		MC2-4
31	37	I/FO		MC2-3
32	38	I/FO		MC2-2
33	39	FO/FOE1		MC2-1
34	40	FO/FOE0		MC3-9
35	41		V_{CCINT}/V_{PP}	
36	42	I/FI		
37	43	I/FO/FI		MC3-8
38	44	I/FO/FI		MC3-7

Ordering Information



Power Options

Q Low Power -10, -12, -15 speeds

Speed Options

-15 15 ns pin-to-pin delay
 -12 12 ns pin-to-pin delay
 -10 10 ns pin-to-pin delay
 -7 7.5 ns pin-to-pin delay (commercial only)
 -5 5 ns pin-to-pin delay (commercial only)

Packaging Options

PC44 44-Pin Plastic Leaded Chip Carrier
 WC44 44-Pin Windowed Ceramic Leaded
 Chip Carrier
 PQ44 44-Pin Plastic Quad Flat Pack
 VQ44 44-Pin Thin Quad Pack

Temperature Options

C Commercial 0°C to 70°C
 I Industrial -40°C to 85°C

Component Availability

Pins		44			
Type		Plastic PLCC	Ceramic CLCC	Plastic PQFP	Plastic VQFP
Code		PC44	WC44	PQ44	VQ44
XC7336	-15	CI	CI	CI	
	-12	CI	CI	C	
	-10	CI	CI	C	
	-7	C	C	C	
	-5	C	C	C	
XC7336Q	-15	CI	CI	C	C
	-12	CI	CI	C	C
	-10	C	C	C	C

C = Commercial = 0° to +70°C I = Industrial = -40° to 85°C

