

## Features

- Ultra high-performance Complex Programmable Logic Devices (CPLDs)
  - 5 ns pin-to-pin speeds on all fast inputs
  - Up to 167 MHz maximum clock frequency
- 100% PCI compliant
- High-drive 24 mA output
- I/O operation at 3.3 V or 5 V
- Meets JEDEC Standard (8-1A) for 3.3 V  $\pm 0.3$  V
- 100% interconnect matrix
  - Maximizes resource utilization
  - Wire-AND capability via SMARTswitch
- Multiple security bits for design protection
- Incorporates two PAL-like 24V9 Fast Function Blocks
- 0.8  $\mu$  CMOS EPROM technology
- Available in 44-pin PQFP and PLCC packages

## General Description

The XC7318 is a high performance CPLD providing general purpose logic integration. It consists of two PAL-like 24V9 Fast Function Blocks interconnected by the 100%-populated Universal Interconnect Matrix (UIM™). See [Figure 1](#) for the architecture overview.

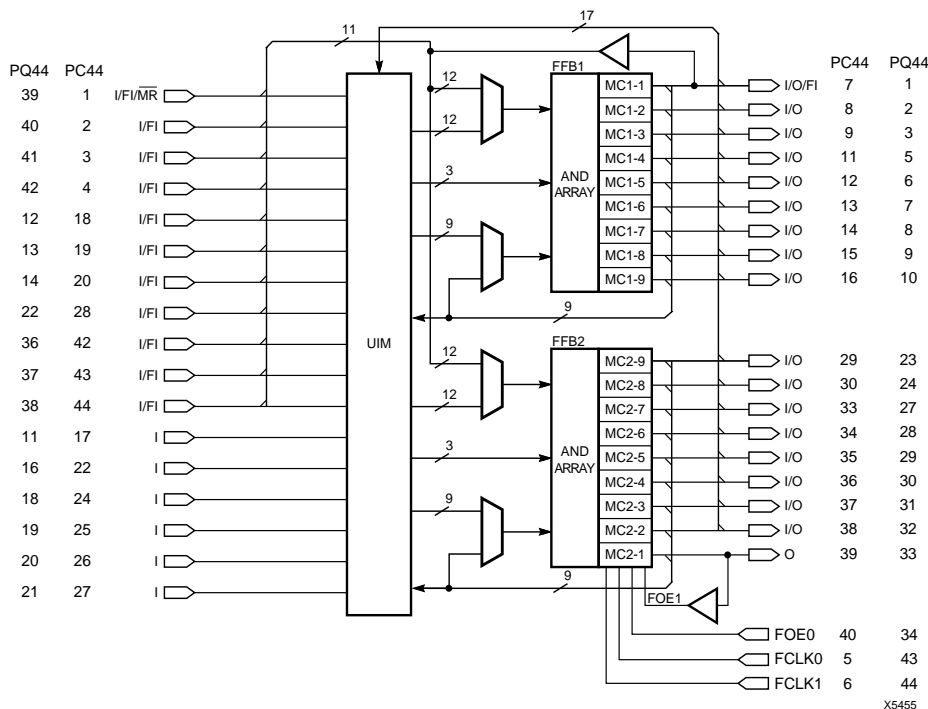


Figure 1: XC7318 Architecture

## Power Estimation

Figure 2 shows a typical power estimation for the XC7318 device, programmed as a 16-bit counter and operating at the indicated clock frequency.

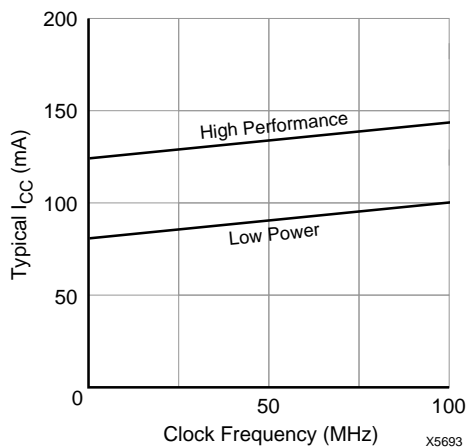


Figure 2: Typical  $I_{CC}$  vs. Frequency for XC7318

## Absolute Maximum Ratings

Symbol	Parameter	Value	Units
$V_{CC}$	Supply voltage with respect to GND	-0.5 to 7.0	V
$V_{IN}$	DC Input voltage with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$V_{TS}$	Voltage applied to 3-state output with respect to GND	-0.5 to $V_{CC} + 0.5$	V
$T_{STG}$	Storage temperature	-65 to +150	°C
$T_{SOL}$	Maximum soldering temperature (10s @ 1/16 in. = 1.5 mm)	+260	°C

**Warning:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
$V_{CCINT}$ $V_{CCIO}$	Supply voltage relative to GND    Commercial $T_A = 0^{\circ}\text{C}$ to $70^{\circ}\text{C}$	4.75	5.25	V
$V_{CCIO}$	I/O supply voltage relative to GND	3.0	3.6	V
$V_{IL}$	Low-level input voltage	0	0.8	V
$V_{IH}$	High-level input voltage	2.0	$V_{CC} + 0.5$	V
$V_O$	Output voltage	0	$V_{CCIO}$	V
$T_{IN}$	Input signal transition time		50.0	ns

## DC Characteristics Over Recommended Operating Conditions

Symbol	Parameter	Test Conditions	Min	Max	Units
$V_{OH}$	5 V TTL High-level output voltage	$I_{OH} = -4.0 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
	3.3 V High-level output voltage	$I_{OH} = -3.2 \text{ mA}$ $V_{CC} = \text{Min}$	2.4		V
$V_{OL}$	5 V TTL Low-level output voltage	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.5	V
	3.3 V Low-level output voltage	$I_{OL} = 24 \text{ mA}$ $V_{CC} = \text{Min}$		0.4	V
$I_{IL}$	Input leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CCIO}$		$\pm 10.0$	$\mu\text{A}$
$I_{OZ}$	Output high-Z leakage current	$V_{CC} = \text{Max}$ $V_{IN} = \text{GND or } V_{CCIO}$		$\pm 10.0$	$\mu\text{A}$
$C_{IN}$	Input capacitance for Input and I/O pins	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		6.0	pF
$C_{IN}$	Input capacitance for global control pins (FCLK0, FCLK1, FOE0, FOE1)	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		8.0	pF
$C_{OUT}^1$	Output capacitance	$V_{IN} = \text{GND}$ $f = 1.0 \text{ MHz}$		10.0	pF
$I_{CC}^2$	Supply current	$V_{IN} = V_{CC} \text{ or GND}$ $V_{CCINT} = V_{CCIO} = 5\text{V}$ $f = 1.0 \text{ MHz @ } 25^\circ\text{C}$	90 Typ		mA

Notes: 1. Sample tested.  
2. Measured with device programmed as a 16-bit counter.

## Power-up/Reset Timing Parameters

Symbol	Parameter	Min	Typ	Max	Units
$t_{WMR}$	Master Reset input Low pulse width	100			ns
$t_{RESET}$	Configuration completion time		80	160	$\mu\text{s}$

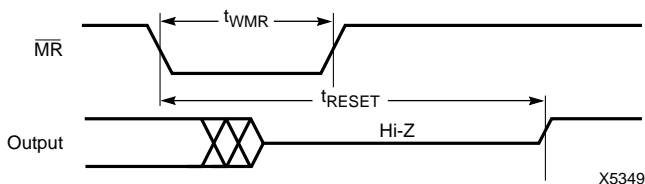


Figure 3: Global Reset Waveform

Fast Function Block (FFB) External AC Characteristics <sup>1</sup>

Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
$t_{PD}$	Fast input to output valid <sup>2</sup>		5.0		7.5	ns
	I/O or input to output valid <sup>2</sup>		8.5		12.0	ns
$t_{SU}$	Fast input setup time before FCLK	4.5		5.0		ns
	I/O or input setup time before FCLK	7.0		8.5		ns
$t_H$	Fast, I/O or input hold time after FCLK	0		0		ns
$t_{CO}$	FCLK input to output valid		4.5		4.5	ns
$t_{FOE}$	FOE input to output valid		7.0		7.5	ns
$t_{FOD}$	FOE input to output disable		7.0		7.5	ns
$f_{MAX}$	Max count frequency <sup>2,3</sup>	167.0		125.0		MHz
$t_{WLH}$	Fast Clock pulse width (High or Low)	3.0		4.0		ns

- Notes: 1. All appropriate ac specifications tested using Figure 5 as test load circuit.  
2. Assumes four product terms per output.  
3. Export Control Max. flip-flop toggle rate.

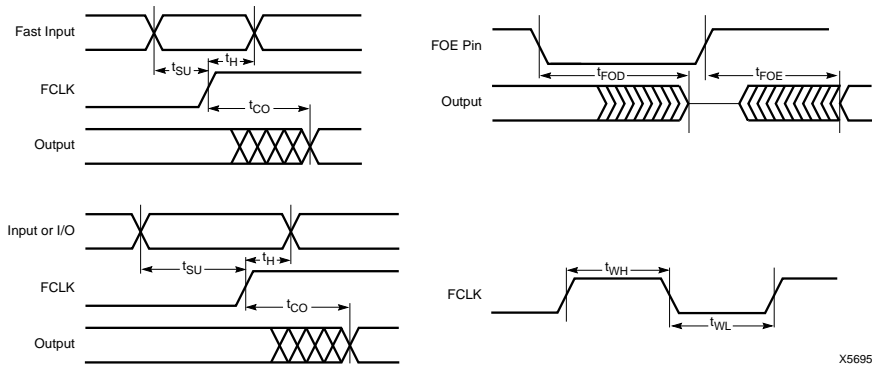


Figure 4: Switching Waveform

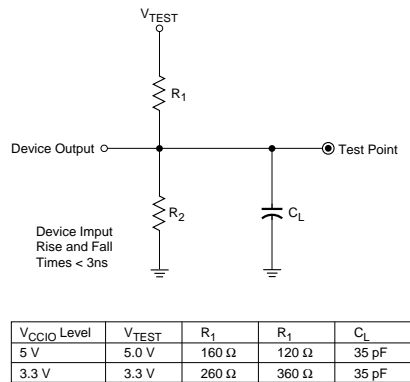
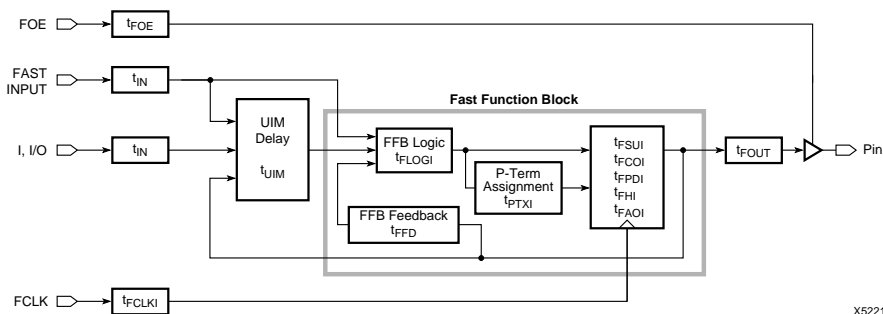


Figure 5: AC Load Circuit



**Figure 6: XC7318 Timing Model**

## Timing Model

Timing within the XC7318 is accurately determined using external timing parameters from the device data sheet, using a variety of CAE simulators, or with the timing model shown in [Figure 6](#).

The timing model is based on the fixed internal delays of the XC7318 architecture that consists of three basic parts:

I/O Blocks, the UIM and Fast Function Blocks. The timing model identifies the internal delay paths and their relationships to ac characteristics. Using this model and the ac characteristics, designers can easily calculate the timing information for the XC7318.

## Fast Function Block (FFB) Internal AC Characteristics

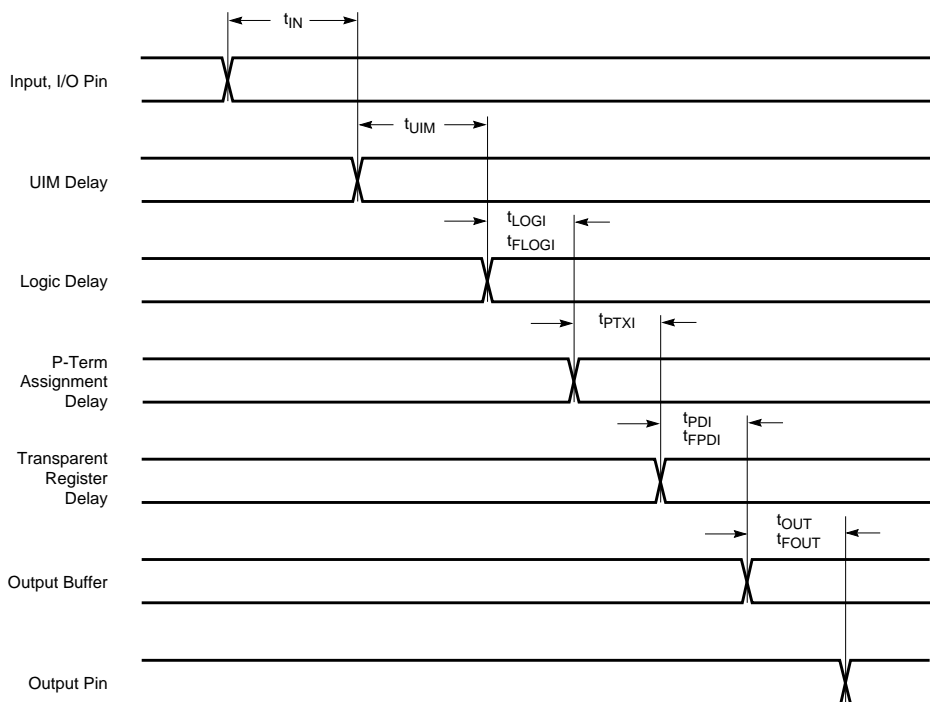
Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
$t_{FLOGI}$	FFB logic array delay <sup>1</sup>		1.0		1.5	ns
$t_{FLOGILP}$	Low-power FFB logic array delay <sup>1</sup>		2.0		3.5	ns
$t_{FSUI}$	FFB register setup time	2.5		1.5		ns
$t_{FHI}$	FFB register hold time	1.0		2.5		ns
$t_{FCOI}$	FFB register clock-to-output delay		1.0		1.0	ns
$t_{FPDI}$	FFB register pass through delay		0.5		0.5	ns
$t_{FAOI}$	FFB register async. set delay		2.0		2.0	ns
$t_{PTXI}$	FFB p-term assignment delay		0.6		0.8	ns
$t_{FFD}$	FFB feedback delay		0.5		4.0	ns

Note: 1. Specifications account for logic paths that use the maximum number of available product terms for a given Macrocell.

## Internal AC Characteristics

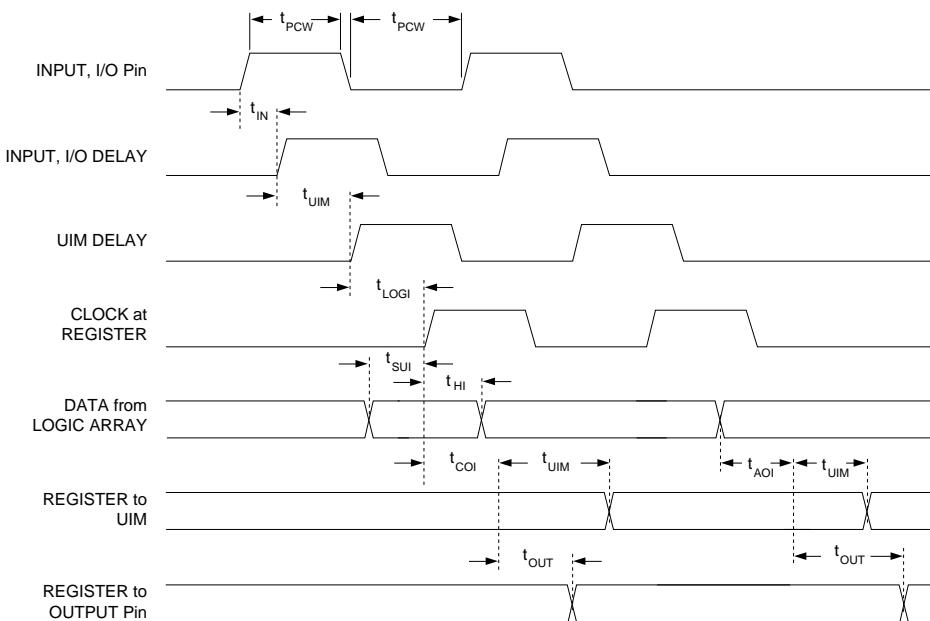
Symbol	Parameter	XC7318-5		XC7318-7		Units
		Min	Max	Min	Max	
$t_{IN}$	Input pad and buffer delay		1.5		2.5	ns
$t_{FOUT}$	FFB output buffer and pad delay		2.0		3.0	ns
$t_{UIM}$	Universal Interconnect Matrix delay		3.5		4.5	ns
$t_{FCLKI}$	Fast clock buffer delay		1.5		1.5	ns

## Combinational Switching Characteristics



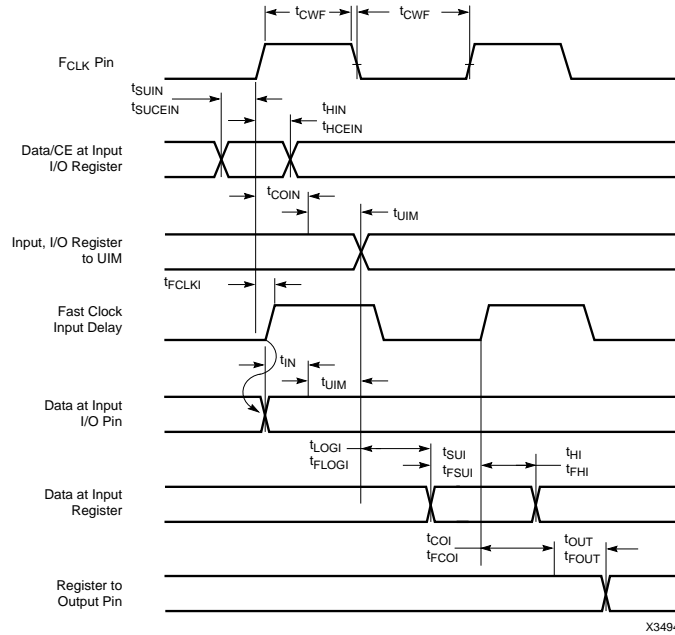
X3339

## Asynchronous Switching Characteristics



X3580

## Synchronous Switching Characteristics

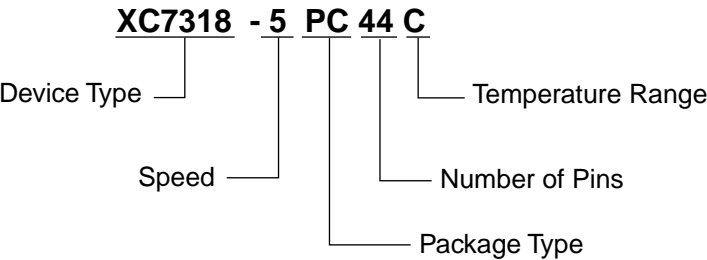


## XC7318 Pinouts

PQ44	PC44	Input	XC7318	Output
39	1	I/FI	MR	
40	2	I/FI		
41	3	I/FI		
42	4	I/FI		
43	5	FCLK0		
44	6	FCLK1		
1	7	I/FO/FI		MC1-1
2	8	I/FO		MC1-2
3	9	I/FO		MC1-3
4	10		GND	
5	11	I/FO		MC1-4
6	12	I/FO		MC1-5
7	13	I/FO		MC1-6
8	14	I/FO		MC1-7
9	15	I/FO		MC1-8
10	16	I/FO		MC1-9
11	17	I		
12	18	I/FI		
13	19	I/FI		
14	20	I/FI		
15	21		V <sub>CCINT</sub>	
16	22	I		

PQ44	PC44	Input	XC7318	Output
17	23		GND	
18	24	I		
19	25	I		
20	26	I		
21	27	I		
22	28	I/FI		
23	29	I/FO		MC2-9
24	30	I/FO		MC2-8
25	31		GND	
26	32		V <sub>CCIO</sub>	
27	33	I/FO		MC2-7
28	34	I/FO		MC2-6
29	35	I/FO		MC2-5
30	36	I/FO		MC2-4
31	37	I/FO		MC2-3
32	38	I/FO		MC2-2
33	39	FOE1/FO		MC2-1
34	40	FOE0		
35	41		V <sub>CCINT</sub> /V <sub>PP</sub>	
36	42	I/FI		
37	43	I/FI		
38	44	I/FI		

Ordering Information



Speed Options

- 7 7.5 ns pin-to-pin delay (commercial only)
- 5 5 ns pin-to-pin delay (commercial only)

Packaging Options

- PC44 44-Pin Plastic Leaded Chip Carrier
- PQ44 44-Pin Plastic Quad Flat Pack

Temperature Options

- C Commercial 0°C to 70°C

Component Availability

Pins		44	
Type		Plastic PLCC	Plastic PQFP
Code		PC44	PQ44
XC7318	-7	C	C
	-5	C	C

C = Commercial = 0° to +70°C