

Features

- 3.3 V V_{CC} with 5 V tolerant inputs
- Third Generation Field-Programmable Gate Arrays
 - Select-RAM™ memory: on-chip ultra-fast RAM with synchronous write and dual port options
 - Abundant flip-flops and flexible function generators
 - Dedicated high-speed carry logic
 - Wide edge decoders on each edge
 - Internal 3-state bus capability
- Almost twice the routing capacity of XC4000E devices
 - Buffered interconnect for maximum speed
 - New latch capability in CLBs
 - Flexible high-speed clock networks
 - 8 global low-skew clock or signal networks
 - Optional multiplexer device outputs
 - High-Speed Parallel Express™ configuration mode
- System Performance to 80 MHz
- Systems-Oriented Features
 - Fully 3.3-V PCI Compliant
 - IEEE 1149.1-compatible boundary scan logic
 - Individually programmable output slew rate
 - Programmable input pull-up or pull-down resistors
 - 12 mA sink current
 - Unlimited reprogrammability
- Readback Capability

Description

The XC4000XL devices extend the popular XC4000E family over the broadest gate capacity range, from 3,000 to 180,000 gates, with up to 7,168 flip-flops. XC4000XL devices are structurally and functionally a superset of the XC4000E family, offering additional and improved signal and clock routing resources, and a new, much faster, byte-wide express configuration mode. XC4000XL devices operate from a 3.3 V supply, but their inputs are 5 V tolerant.

All XC4000-Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a power hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave, peripheral and express modes).

All XC4000-Series FPGAs are supported by powerful and sophisticated software, covering every aspects of design from schematic or behavioral entry, floorplanning, simulation, automatic block placement and routing of interconnects, to the creation, downloading, and readback of the configuration bit stream.

XC4000XL Family of Field Programmable Gate Arrays

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total Logic Blocks	Number of Flip-Flops	Max.Decode Inputs per side	Max. User I/O
XC4005XL	5,000	6,272	3,000 - 9,000	14 x 14	196	616	42	112
XC4010XL	10,000	12,800	7,000 - 20,000	20 x 20	400	1,120	60	160
XC4013XL	13,000	18,432	10,000 - 30,000	24 x 24	576	1,336	72	192
XC4020XL	20,000	25,088	13,000 - 40,000	28 x 28	784	2,016	84	224
XC4028XL	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	96	256
XC4036XL	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	108	288
XC4044XL	44,000	51,200	27,000 - 80,000	40 x 40	1,600	3,840	120	320
XC4052XL	52,000	61,952	33,000 - 100,000	44 x 44	1,936	4,576	132	352
XC4062XL	62,000	73,728	40,000 - 130,000	48 x 48	2,304	5,376	144	384
XC4085XL	85,000	100,352	55,000 - 180,000	56 x 56	3,136	7,168	168	448

* Max values of Typical Gate Range include 20-30% of CLBs used as RAM

XC4000XL Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND		-0.5 to 4.0 V
V_{IN}	Input voltage relative to GND (Note 1)		-0.5 to 5.5 V
V_{TS}	Voltage applied to 3-state output (Note 1)		-0.5 to 5.5 V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 3V		50 ms
T_{STG}	Storage temperature (ambient)		-65 to +150 °C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)		+260 °C
T_J	Junction temperature	Ceramic packages	+150 °C
		Plastic packages	+125 °C

Notes: 1. Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to + 7.0 V, provided this over- or undershoot lasts less than 10 ns.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0\text{ °C to }+85\text{ °C}$	Commercial	3.0	3.6	V
	Supply voltage relative to GND, $T_J = -40\text{ °C to }+100\text{ °C}$	Industrial	3.0	3.6	V
V_{IH}	High-level input voltage		50% of V_{CC}	5.5	V
V_{IL}	Low-level input voltage		0	30 of % V_{CC}	V
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C. Input and output measurement threshold is ~50% of V_{CC} .

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ $I_{OH} = -4.0$ mA, V_{CC} min (LVTTL)		2.4		V
	High-level output voltage @ $I_{OH} = -500$ μ A, (LVCMOS)		90% V_{CC}		V
V_{OL}	Low-level output voltage @ $I_{OL} = 12.0$ mA, V_{CC} min (LVTTL) (Note 1)			0.4	V
	Low-level output voltage @ $I_{OL} = 1500$ μ A, (LVCMOS)			10% V_{CC}	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		2.5		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			5	mA
I_L	Input or output leakage current		-10	+10	μ A
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{in} = 0$ V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ $V_{in} = 3.6$ V (sample tested)		0.02	0.15	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND.

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). All XC4036XL values are preliminary.

Speed Grade			-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Max	Max	Max	Max	Max	
From pad through Global Low Skew buffer, to any clock K	T _{GLS}	XC4005XL	5.0					ns
		XC4010XL	5.9					ns
		XC4013XL	6.5					ns
		XC4020XL	7.0					ns
		XC4028XL	7.5					ns
		XC4036XL	7.9					ns
		XC4044XL	8.4					ns
		XC4052XL	8.8					ns
		XC4062XL	9.2					ns
XC4085XL	9.9	ns						
From pad through Global Early buffer, to any clock K in same quadrant	T _{GE}	XC4005XL	3.0					ns
		XC4010XL	3.5					ns
		XC4013XL	3.9					ns
		XC4020XL	4.2					ns
		XC4028XL	4.4					ns
		XC4036XL	4.7					ns
		XC4044XL	5.0					ns
		XC4052XL	5.2					ns
		XC4062XL	5.4					ns
XC4085XL	5.9	ns						
			ADVANCE					

CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and expressed in nanoseconds unless otherwise noted. All XC4036XL values are preliminary.

Speed Grade		-3		-2		-1		-09		-08	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Combinatorial Delays											
F/G inputs to X/Y outputs	T _{ILO}		1.8								
F/G inputs via H' to X/Y outputs	T _{IHO}		3.2								
F/G inputs via transparent latch to Q outputs	T _{ITO}		2.7								
C inputs via SR/H0 via H' to X/Y outputs	T _{HH0O}		3.0								
C inputs via H1 via H' to X/Y outputs	T _{HH1O}		2.5								
C inputs via DIN/H2 via H' to X/Y outputs	T _{HH2O}		3.0								
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T _{CBYP}		1.6								
CLB Fast Carry Logic											
Operand inputs (F1, F2, G1, G4) to COUT	T _{OPCY}		3.9								
Add/Subtract input (F3) to COUT	T _{ASCY}		3.7								
Initialization inputs (F1, F3) to COUT	T _{INCY}		2.6								
CIN through function generators to X/Y outputs	T _{SUM}		3.9								
CIN to COUT, bypass function generators	T _{BYP}		0.4								
Sequential Delays											
Clock K to Flip-Flop outputs Q	T _{CKO}		1.9								
Clock K to Latch outputs Q	T _{CKLO}		1.9								
Setup Time before Clock K											
F/G inputs	T _{IJK}	1.2									
F/G inputs via H'	T _{IHCK}	2.6									
C inputs via H0 through H'	T _{HH0CK}	2.5									
C inputs via H1 through H'	T _{HH1CK}	2.0									
C inputs via H2 through H'	T _{HH2CK}	2.5									
C inputs via DIN	T _{DICK}	1.1									
C inputs via EC	T _{ECCK}	1.2									
C inputs via S/R, going Low (inactive)	T _{RCK}	1.1									
CIN input via F'/G'	T _{CCK}	2.1									
CIN input via F'/G' and H'	T _{CHCK}	3.5									
Hold Time after Clock K											
F/G inputs	T _{CKI}	0									
F/G inputs via H'	T _{CKIH}	0									
C inputs via SR/H0 through H'	T _{CKHH0}	0									
C inputs via H1 through H'	T _{CKHH1}	0									
C inputs via DIN/H2 through H'	T _{CKHH2}	0									
C inputs via DIN/H2	T _{CKDI}	0									
C inputs via EC	T _{CKEC}	0									
C inputs via SR, going Low (inactive)	T _{CKR}	0									
Clock											
Clock High time	T _{CH}	3.0									
Clock Low time	T _{CL}	3.0									
Set/Reset Direct											
Width (High)	T _{RPW}	3.0									
Delay from C inputs via S/R, going High to Q	T _{RIO}		3.6								
Global Set/Reset											
Minimum GSR Pulse Width	T _{MRW}		11.5								
Delay from GSR input to any Q	T _{MRQ}	Note 1									
Toggle Frequency (MHz) (Note 2)	F _{TOG}		166								
ADVANCE											

Note 1: For values per device, see Globals Set/Reset entries on page 15.

Note 2: Maximum flip-flop toggle rate for export control purposes.

CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted. All XC4036XL values are preliminary.

Single Port RAM	Speed Grade		-3		-2		-1		-09		-08	
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Write Operation												
Address write cycle time (clock K period)	16x2	T_{WCS}	9.0									
	32x1	T_{WCTS}	9.0									
Clock K pulse width (active edge)	16x2	T_{WPS}	4.5	1 ms								
	32x1	T_{WPTS}	4.5	1 ms								
Address setup time before clock K	16x2	T_{ASS}	2.2									
	32x1	T_{ASTS}	2.2									
Address hold time after clock K	16x2	T_{AHS}	0									
	32x1	T_{AHTS}	0									
DIN setup time before clock K	16x2	T_{DSS}	2.0									
	32x1	T_{DSTS}	2.5									
DIN hold time after clock K	16x2	T_{DHS}	0									
	32x1	T_{DHTS}	0									
WE setup time before clock K	16x2	T_{WSS}	2.0									
	32x1	T_{WSTS}	1.8									
WE hold time after clock K	16x2	T_{WHS}	0									
	32x1	T_{WHTS}	0									
Data valid after clock K	16x2	T_{WOS}		6.8								
	32x1	T_{WOTS}		7.0								

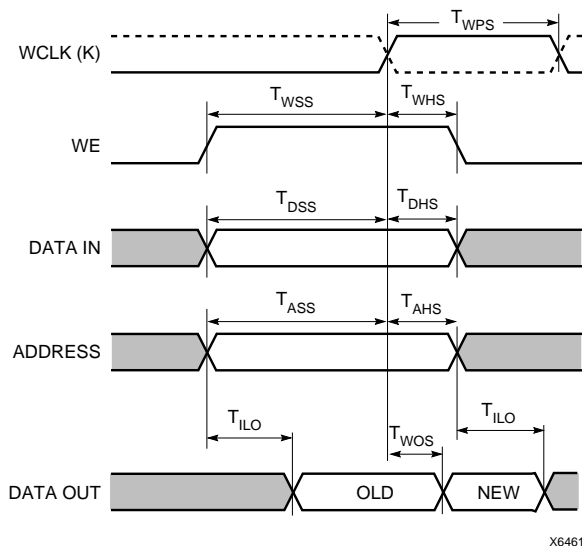
ADVANCE

Dual Port RAM	Speed Grade		-3		-2		-1		-09		-08	
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Write Operation												
Address write cycle time (clock K period)	16x1	T_{WCDS}	9.0	1 ms								
Clock K pulse width (active edge)	16x1	T_{WPDS}	4.5	1 ms								
Address setup time before clock K	16x1	T_{ASDS}	2.5									
Address hold time after clock K	16x1	T_{AHDS}	0									
DIN setup time before clock K	16x1	T_{DSDS}	2.5									
DIN hold time after clock K	16x1	T_{DHDS}	0									
WE setup time before clock K	16x1	T_{WSDS}	1.8									
WE hold time after clock K	16x1	T_{WHDS}	0									
Data valid after clock K	16x1	T_{WODS}		7.8								

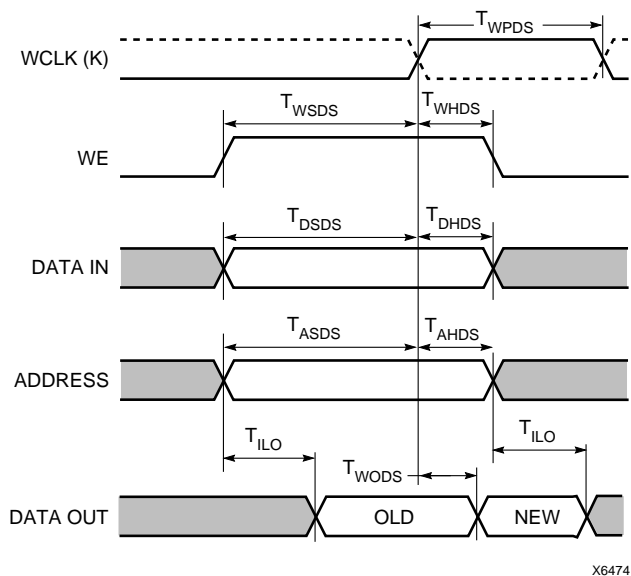
ADVANCE

Notes: Timing for the 16 x1 RAM option is identical to 16 x 2 RAM timing.
Applicable Read timing specifications are identical to Asynchronous (Level Sensitive) Read timing

CLB RAM Synchronous (Edge-Triggered) Write Timing



CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



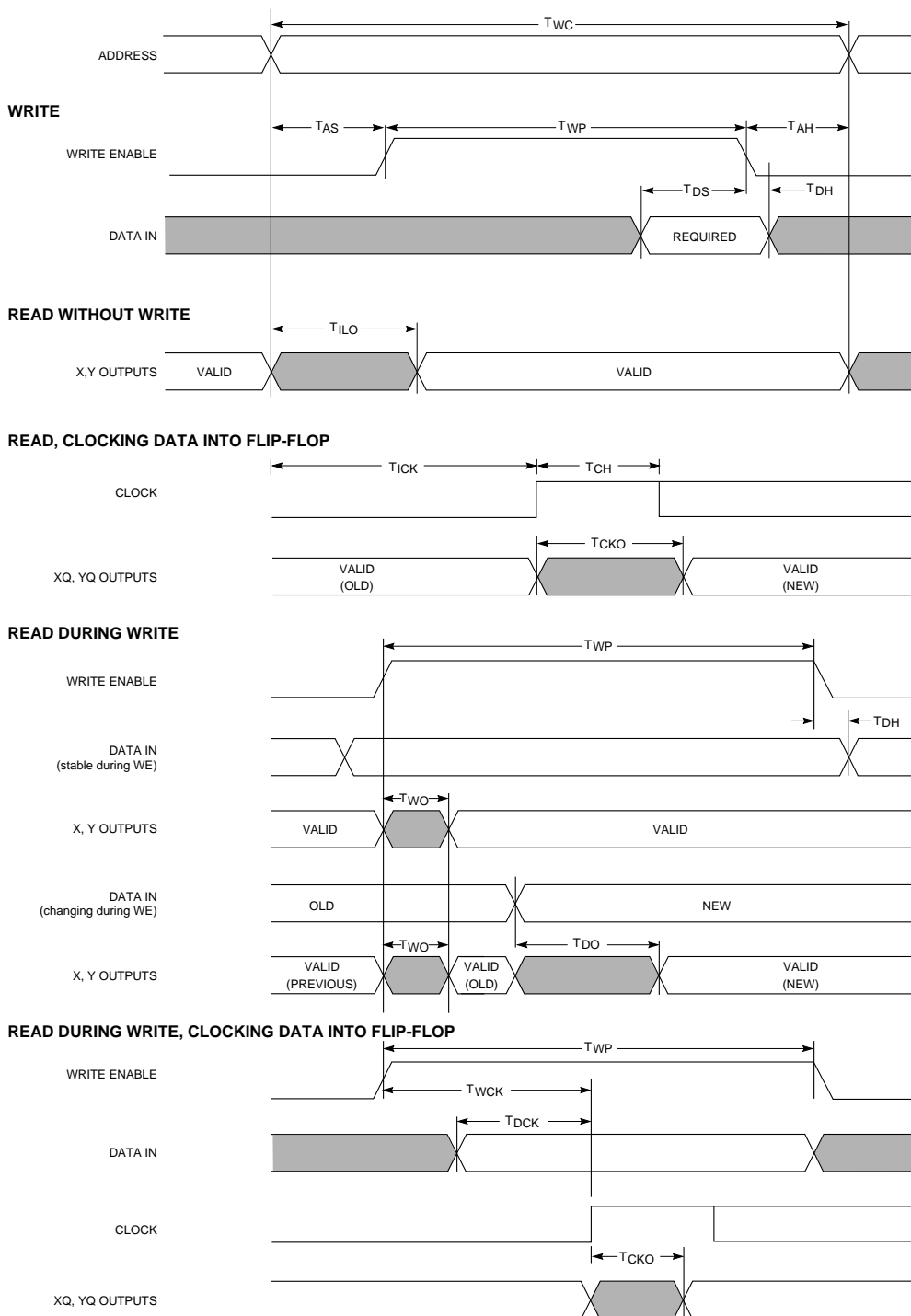
CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted. All XC4036XL values are preliminary

Speed Grade			-3		-2		-1		-09		-08	
Description	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Write Operation												
Address write cycle time	16x2	T _{WC}	8.0									
	32x1	T _{WCT}	8.0									
Write Enable pulse width (High)	16x2	T _{WP}	4.0									
	32x1	T _{WPT}	4.0									
Address setup time before WE	16x2	T _{AS}	2.0									
	32x1	T _{AST}	2.0									
Address hold time after end of WE	16x2	T _{AH}	2.0									
	32x1	T _{AHT}	2.0									
DIN setup time before end of WE	16x2	T _{DS}	2.2									
	32x1	T _{DST}	2.2									
DIN hold time after end of WE	16x2	T _{DH}	2.0									
	32x1	T _{DHT}	2.0									
Read Operation												
Address read cycle time	16x2	T _{RC}	3.1									
	32x1	T _{RCT}	5.5									
Data valid after address change (no Write Enable)	16x2	T _{ILO}		1.8								
	32x1	T _{IHO}		3.2								
Read Operation, Clocking Data into Flip-Flop												
Address setup time before clock K	16x2	T _{ICK}	1.2									
	32x1	T _{IHCK}	2.6									
Read During Write												
Data valid after WE goes active (DIN stable before WE)	16x2	T _{WO}		6.0								
	32x1	T _{WOT}		7.3								
Data valid after DIN (DIN changes during WE)	16x2	T _{DO}		6.6								
	32x1	T _{DOT}		7.6								
Read During Write, Clocking Data into Flip-Flop												
WE setup time before clock K	16x2	T _{WCK}	6.0									
	32x1	T _{WCKT}	6.8									
Data setup time before clock K	16x2	T _{DCK}	5.2									
	32x1	T _{DCKT}	6.2									
			ADVANCE									

Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing

CLB RAM Asynchronous (Level-Sensitive) Timing Characteristics



X2640

Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All XC4036XL values are preliminary.

Output Flip-Flop, Clock to Out

Speed Grade			-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Max	Max	Max	Max	Max	
Global Low Skew Clock to Output using OFF	T _{ICKOF}	XC4005XL	11.1					ns
		XC4010XL	12.1					ns
		XC4013XL	12.6					ns
		XC4020XL	13.2					ns
		XC4028XL	13.6					ns
		XC4036XL	14.1					ns
		XC4044XL	14.5					ns
		XC4052XL	14.9					ns
		XC4062XL	15.3					ns
		XC4085XL	16.0					ns
Global Early Clock to Output using OFF	T _{ICKEOF}	XC4005XL	9.1					ns
		XC4010XL	9.7					ns
		XC4013XL	10.0					ns
		XC4020XL	10.3					ns
		XC4028XL	10.6					ns
		XC4036XL	10.9					ns
		XC4044XL	11.1					ns
		XC4052XL	11.4					ns
		XC4062XL	11.6					ns
		XC4085XL	12.0					ns
For output SLOW option add	T _{SLOW}	All Devices	3.0					ns
OFF = Output Flip Flop			ADVANCE					

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

Output timing is measured at ~50% V_{CC} threshold with 35 pF external capacitive load.

Output MUX, Clock to Out

Speed Grade			-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Max	Max	Max	Max	Max	
Global Low Skew Clock to Output using OMUX	T _{PEFPF}	XC4005XL	10.5					ns
		XC4010XL	11.5					ns
		XC4013XL	12.0					ns
		XC4020XL	12.5					ns
		XC4028XL	13.0					ns
		XC4036XL	13.5					ns
		XC4044XL	13.9					ns
		XC4052XL	14.3					ns
		XC4062XL	14.7					ns
		XC4085XL	15.4					ns
Global Early Clock to Output using OMUX	T _{PEFPF}	XC4005XL	8.5					ns
		XC4010XL	9.1					ns
		XC4013XL	9.4					ns
		XC4020XL	9.7					ns
		XC4028XL	10.0					ns
		XC4036XL	10.2					ns
		XC4044XL	10.5					ns
		XC4052XL	10.7					ns
		XC4062XL	11.0					ns
		XC4085XL	11.4					ns
For output SLOW option add	T _{SLOW}	All Devices	3.0					ns
			ADVANCE					

OMUX = Output MUX

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net. Output timing is measured at ~50% V_{CC} threshold with 35 pF external capacitive load.

Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All XC4036XL values are preliminary.

Global Low Skew Clock, Set-Up and Hold

Speed Grade			-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Min	Min	Min	Min	
Input Setup Time, using Global Low Skew clock and IFF (full delay)	T _{PSD}	XC4005XL	6.8					ns
		XC4010XL	6.8					ns
		XC4013XL	6.8					ns
		XC4020XL	6.8					ns
		XC4028XL	6.8					ns
		XC4036XL	6.8					ns
		XC4044XL	6.8					ns
		XC4052XL	6.8					ns
		XC4062XL	6.8					ns
XC4085XL	6.8					ns		
Input Hold Time, using Global Low Skew clock and IFF (full delay)	T _{PHD}	XC4005XL	0					ns
		XC4010XL	0					ns
		XC4013XL	0					ns
		XC4020XL	0					ns
		XC4028XL	0					ns
		XC4036XL	0					ns
		XC4044XL	0					ns
		XC4052XL	0					ns
		XC4062XL	0					ns
XC4085XL	0					ns		
IFF = Input Flip-Flop or Latch			ADVANCE					

Note: Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Global Early Clock, Set-Up and Hold for IFF

Description	Symbol	Speed Grade Device	-3	-2	-1	-09	-08	Units
			Min	Min	Min	Min	Min	
Input Setup Time, using Global Early clock and IFF (partial delay)	T _{PSEP}	XC4005XL						ns
		XC4010XL						ns
		XC4013XL	5.4					ns
		XC4020XL						ns
		XC4028XL						ns
		XC4036XL	5.4					ns
		XC4044XL						ns
		XC4052XL						ns
		XC4062XL	5.4					ns
		XC4085XL						ns
Input Hold Time, using Global Early clock and IFF (partial delay)	T _{PHEP}	XC4005XL	0					ns
		XC4010XL	0					ns
		XC4013XL	1					ns
		XC4020XL	0					ns
		XC4028XL	0					ns
		XC4036XL	1					ns
		XC4044XL	0					ns
		XC4052XL	0					ns
		XC4062XL	1					ns
		XC4085XL	0					ns

IFF = Input Flip-Flop or Latch

ADVANCE

Note: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

Global Early Clock, Set-Up and Hold for FCL

Description	Symbol	Speed Grade Device	-3	-2	-1	-09	-08	Units
			Min	Min	Min	Min	Min	
Input Setup Time, using Global Early clock and FCL (partial delay)	T _{PFSEP}	XC4005XL						ns
		XC4010XL						ns
		XC4013XL	5.0					ns
		XC4020XL						ns
		XC4028XL						ns
		XC4036XL	5.0					ns
		XC4044XL						ns
		XC4052XL						ns
		XC4062XL	5.0					ns
		XC4085XL						ns
Input Hold Time, using Global Early clock and FCL (partial delay)	T _{PFHEP}	XC4005XL	0					ns
		XC4010XL	0					ns
		XC4013XL	1					ns
		XC4020XL	0					ns
		XC4028XL	0					ns
		XC4036XL	1					ns
		XC4044XL	0					ns
		XC4052XL	0					ns
		XC4062XL	1					ns
		XC4085XL	0					ns

FCL = Fast Capture Latch

ADVANCE

Note: Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Note: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6

IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). All XC4036XL values are preliminary.

Speed Grade			-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Min	Min	Min	Min	
Clocks								
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T _{OKIK}	All devices	2.6					ns
Propagation Delays			Max	Max	Max	Max	Max	
Pad to I1, I2	T _{PID}	All devices	1.9					ns
Pad to I1, I2 via transparent input latch, no delay	T _{PLI}	All devices	3.2					ns
Pad to I1, I2 via transparent input latch, partial delay	T _{PPLI}	XC4005XL	7.2					ns
		XC4010XL	8.5					ns
		XC4013XL	9.4					ns
		XC4020XL	10.2					ns
		XC4028XL	11.1					ns
		XC4036XL	12.1					ns
		XC4044XL	12.8					ns
		XC4052XL	13.7					ns
		XC4062XL	14.6					ns
XC4085XL	16.3	ns						
Pad to I1, I2 via transparent input latch, full delay	T _{PDLI}	XC4005XL	9.0					ns
		XC4010XL	11.0					ns
		XC4013XL	12.4					ns
		XC4020XL	13.8					ns
		XC4028XL	15.2					ns
		XC4036XL	16.2					ns
		XC4044XL	17.9					ns
		XC4052XL	19.3					ns
		XC4062XL	20.7					ns
XC4085XL	23.4	ns						

FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch

ADVANCE

IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). All XC4036XL values are preliminary.

			Speed Grade		-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Max	Max	Max	Max	Max			
Propagation Delays										
Pad to I1, I2 via transparent FCL and input latch, no delay	T _{PFLI}	All devices	4.4							ns
Pad to I1, I2 via transparent FCL and input latch, partial delay	T _{PPFLI}	XC4005XL	7.4							ns
		XC4010XL	8.7							ns
		XC4013XL	9.6							ns
		XC4020XL	10.5							ns
		XC4028XL	11.3							ns
		XC4036XL	12.3							ns
		XC4044XL	13.1							ns
		XC4052XL	13.9							ns
		XC4062XL	14.8							ns
		XC4085XL	16.5							ns
Propagation Delays										
Clock (IK) to I1, I2 (flip-flop)	T _{IKRI}	All devices	2.5							ns
Clock (IK) to I1, I2 (latch enable, active Low)	T _{IKLI}	All devices	2.7							ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T _{OKLI}	All devices	5.2							ns
Global Set/Reset										
Minimum GSR Pulse Width Delay from GSR input to any Q	T _{MRW} T _{RRI}	All devices	11.5							ns
		XC4005XL	8.4							ns
		XC4010XL	11.9							ns
		XC4013XL	14.3							ns
		XC4020XL	16.7							ns
		XC4028XL	19.0							ns
		XC4036XL	21.4							ns
		XC4044XL	23.8							ns
		XC4052XL	26.2							ns
		XC4062XL	28.5							ns
		XC4085XL	33.3							ns

FCL = Fast Capture Latch

ADVANCE

IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). All XC4036XL values are preliminary.

Speed Grade			-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Min	Min	Min	Min	Min	
Setup Times								
Pad to Clock (IK), no delay	T _{PICK}	All devices	2.0					ns
Pad to Clock (IK), partial delay	T _{PICKP}	XC4005XL	5.1					ns
		XC4010XL	6.4					ns
		XC4013XL	7.3					ns
		XC4020XL	8.1					ns
		XC4028XL	9.0					ns
		XC4036XL	10.0					ns
		XC4044XL	10.7					ns
		XC4052XL	11.6					ns
		XC4062XL	12.5					ns
		XC4085XL	14.2					ns
Pad to Clock (IK), full delay	T _{PICKD}	XC4005XL	6.9					ns
		XC4010XL	9.0					ns
		XC4013XL	10.3					ns
		XC4020XL	11.7					ns
		XC4028XL	13.1					ns
		XC4036XL	14.1					ns
		XC4044XL	15.8					ns
		XC4052XL	17.2					ns
		XC4062XL	18.6					ns
		XC4085XL	21.3					ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T _{PICKF}	All devices	3.3					ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	T _{PICKFP}	XC4005XL	6.3					ns
		XC4010XL	7.6					ns
		XC4013XL	8.5					ns
		XC4020XL	9.4					ns
		XC4028XL	10.2					ns
		XC4036XL	11.2					ns
		XC4044XL	12.0					ns
		XC4052XL	12.8					ns
		XC4062XL	13.7					ns
		XC4085XL	15.4					ns
Pad to Fast Capture Latch Enable (OK), no delay	T _{POCK}	All devices	0.7					ns
Setup Times								
Clock Enable (EC) to Clock (IK)	T _{ECIK}	All devices	0.2					ns
Hold Times								
All Hold Times		All devices	0	0	0	0	0	ns

ADVANCE

Notes: Input pad setup and hold times are specified with respect to the internal clock (IK). For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on pages 12 and 13.

IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000XL devices and are expressed in nanoseconds unless otherwise noted. All XC4036XL values are preliminary.

Speed Grade		-3		-2		-1		-.09		-08	
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Propagation Delays											
Clock (OK) to Pad	T _{OKPOF}		6.2								
Output (O) to Pad	T _{OPF}		5.1								
3-state to Pad hi-Z (slew-rate independent)	T _{TSHZ}		4.1								
3-state to Pad active and valid	T _{TSONF}		8.1								
Output MUX Select (OK) to Pad	T _{OFPF}		5.5								
Fast Path Output MUX Input (OK) to Pad	T _{OFPF}		5.1								
Slowest Path Output MUX Input to Pad	T _{OSPF}		6.0								
Setup and Hold Times											
Output (O) to clock (OK) setup time	T _{OOK}	0.5									
Output (O) to clock (OK) hold time	T _{OKO}	0									
Clock Enable (EC) to clock (OK) setup	T _{ECOK}	0									
Clock Enable (EC) to clock (OK) hold	T _{OKEC}	0.3									
Clock											
Clock High	T _{CH}	3.0									
Clock Low	T _{CL}	3.0									
Global Set/Reset											
Minimum GSR pulse width	T _{MRW}	11.5									
Delay from GSR input to any Pad	T _{RPO}										
XC4005XL		13.4									
XC4010XL		16.9									
XC4013XL		19.3									
XC4020XL		21.7									
XC4028XL		24.0									
XC4036XL		26.4									
XC4044XL		28.8									
XC4052XL		31.2									
XC4062XL		33.5									
XC4085XL		38.3									
Slew Rate Adjustment											
For output SLOW option add	T _{SLOW}		3.0								
ADVANCE											

Note: Output timing is measured at ~50% V_{CC} threshold, with 35pF external capacitive loads.

Horizontal Longline Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). All XC4036XL values are preliminary.

			Speed Grade		-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Max	Max	Max	Max	Max	Max		
TBUF driving a Horizontal Longline										
I going High or Low to Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T _{IO1}	XC4005XL	5.3						ns	
		XC4010XL	7.6						ns	
		XC4013XL	9.1						ns	
		XC4020XL	10.6						ns	
		XC4028XL	11.3						ns	
		XC4036XL	13.6						ns	
		XC4044XL	15.2						ns	
		XC4052XL	16.7						ns	
		XC4062XL	18.2						ns	
		XC4085XL	21.2						ns	
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T _{ON}	XC4005XL	5.7						ns	
		XC4010XL	8.3						ns	
		XC4013XL	9.8						ns	
		XC4020XL	10.4						ns	
		XC4028XL	12.1						ns	
		XC4036XL	14.6						ns	
		XC4044XL	16.2						ns	
		XC4052XL	17.8						ns	
		XC4062XL	19.5						ns	
		XC4085XL	22.7						ns	
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. (Note 1)	T _{PU2}	XC4005XL							ns	
		XC4010XL							ns	
		XC4013XL							ns	
		XC4020XL							ns	
		XC4028XL							ns	
		XC4036XL							ns	
		XC4044XL							ns	
		XC4052XL							ns	
		XC4062XL							ns	
		XC4085XL							ns	
			ADVANCE							

Note: These values include a minimum load of one output, spaced as far as possible from the active pullup(s). Use the static timing analyzer to determine the delay for each destination.

Note 1: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

Horizontal Longline Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). All XC4036XL values are preliminary.

			Speed Grade		-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Max	Max	Max	Max	Max			
TBUF driving half a Horizontal Longline										
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T _{HIO1}	XC4005XL	2.4					ns		
		XC4010XL	3.4					ns		
		XC4013XL	4.1					ns		
		XC4020XL	4.7					ns		
		XC4028XL	5.6					ns		
		XC4036XL	6.1					ns		
		XC4044XL	6.8					ns		
		XC4052XL	7.4					ns		
		XC4062XL	8.1					ns		
		XC4085XL	9.5					ns		
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T _{HON}	XC4005XL	2.7					ns		
		XC4010XL	3.8					ns		
		XC4013XL	4.6					ns		
		XC4020XL	5.4					ns		
		XC4028XL	6.4					ns		
		XC4036XL	6.9					ns		
		XC4044XL	7.6					ns		
		XC4052XL	8.4					ns		
		XC4062XL	9.2					ns		
		XC4085XL	10.7					ns		
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. (Note 1)	T _{HPU4}	XC4005XL						ns		
		XC4010XL						ns		
		XC4013XL						ns		
		XC4020XL						ns		
		XC4028XL						ns		
		XC4036XL						ns		
		XC4044XL						ns		
		XC4052XL						ns		
		XC4062XL						ns		
		XC4085XL						ns		
			ADVANCE							

Note: These values include a minimum load of one output, spaced as far as possible from the active pullup(s). Use the static timing analyzer to determine the delay for each destination.

Note 1: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

Wide Decoder Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). All XC4036XL values are preliminary.

Speed Grade			-3	-2	-1	-09	-08	Units
Description	Symbol	Device	Max	Max	Max	Max	Max	
Half length, two pull-ups, inputs from IOB I-pins	T _{WAO2}	XC4005XL						ns
		XC4010XL						ns
		XC4013XL						ns
		XC4020XL						ns
		XC4028XL						ns
		XC4036XL						ns
		XC4044XL						ns
		XC4052XL						ns
		XC4062XL						ns
		XC4085XL						ns
Half length, two pull-ups, inputs from internal logic	T _{WAO2L}	XC4005XL						ns
		XC4010XL						ns
		XC4013XL						ns
		XC4020XL						ns
		XC4028XL						ns
		XC4036XL						ns
		XC4044XL						ns
		XC4052XL						ns
		XC4062XL						ns
		XC4085XL						ns
Half length, two pull-ups, inputs from IOB I-pins	T _{WAO2}	XC4005XL						ns
		XC4010XL						ns
		XC4013XL						ns
		XC4020XL						ns
		XC4028XL						ns
		XC4036XL						ns
		XC4044XL						ns
		XC4052XL						ns
		XC4062XL						ns
		XC4085XL						ns
Half length, two pull-ups, inputs from internal logic	T _{WAO2L}	XC4005XL						ns
		XC4010XL						ns
		XC4013XL						ns
		XC4020XL						ns
		XC4028XL						ns
		XC4036XL						ns
		XC4044XL						ns
		XC4052XL						ns
		XC4062XL						ns
		XC4085XL						ns
			ADVANCE					

Notes: These delays are specified from the decoder input to the decoder output.
Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.