

Feature

- Third Generation Field-Programmable Gate Arrays
 - Select-RAM™ memory: on-chip ultra-fast RAM with
 - synchronous write options and dual port
 - Abundant flip-flops and flexible function generators
 - Dedicated high-speed carry logic
 - Wide edge decoders on each edge
 - Hierarchy of interconnects lines
 - Internal 3-state bus capability
- Almost twice the routing capacity of XC4000E devices
 - Buffered interconnect for maximum speed
 - New latch capability in CLBs
 - VersaRing™ I/O Interconnect improves pin locking
 - Flexible high-speed clock networks
 - 8 global low-skew clock or signal distribution networks
 - 8 additional Early Buffers for shorter clock delays
 - Optional multiplexer or 2-input function generator on device outputs
 - High-Speed Parallel Express™ configuration mode
 - Improved I/O set-up and clock-to-output global early buffers
- System Performance to 80 MHz
- Systems-Oriented Features
 - IEEE 1149.1-compatible boundary scan logic support
 - Individually programmable output slew rate
 - Programmable input pull-up or pull-down resistors
 - 12mA sink current
- Configured by Loading Binary File
 - Unlimited reprogrammability
- Readback Capability
- 5 V V_{CC}
 - For functionally identical 3.3 V devices, see the XC4000XL family

Description

The XC4028EX and XC4036EX devices extend the popular XC4000E family to the 18,000 to 65,000 gate capacity range, with up to 3,168 flip-flops. XC4000EX devices are electrically, structurally, and functionally a superset of the XC4000E family, offering additional and improved signal and clock routing resources, and a new, much faster, byte-wide express configuration mode.

XC4000-Series devices are implemented with a regular, flexible, programmable architecture of Configurable Logic Blocks (CLBs), interconnected by a power hierarchy of versatile routing resources, and surrounded by a perimeter of programmable Input/Output Blocks (IOBs). They have generous routing resources to accommodate the most complex interconnect patterns.

The devices are customized by loading configuration data into internal memory cells. The FPGA can either actively read its configuration data from an external serial or byte-parallel PROM (master modes), or the configuration data can be written into the FPGA from an external device (slave, peripheral and Express modes).

All XC4000-Series FPGAs are supported by powerful and sophisticated software, covering every aspects of design from schematic or behavioral entry, floorplanning, simulation, automatic block placement and routing of interconnects, to the creation, downloading, and readback of the configuration bit stream.

Because Xilinx FPGAs can be reprogrammed an unlimited number of times, they can be used in innovative designs where hardware is changed dynamically, or where hardware must be adapted to different user applications. FPGAs are ideal for shortening design and development cycles, and also offer a cost-effective solution for production rates well beyond 5,000 systems per month. For lower high-volume unit cost, a design can first be implemented in the XC4000E or XC 4000EX, then migrated to one of Xilinx's compatible HardWire mask-programmed devices.

Table 1: XC4000EX Field Programmable Gate Arrays

Device	Max. Logic Gates (No RAM)	Max. RAM Bits (No Logic)	Typical Gate Range (Logic and RAM)*	CLB Matrix	Total Logic Blocks	Number of Flip-Flops	Max.Decode Inputs per side	Max. User I/O
XC4028EX	28,000	32,768	18,000 - 50,000	32 x 32	1,024	2,560	96	256
XC4036EX	36,000	41,472	22,000 - 65,000	36 x 36	1,296	3,168	108	288

*Max values of Typical Gate Range include 20-30% of CLBs used as RAM

XC4000EX Switching Characteristics

Definition of Terms

In the following tables, some specifications may be designated as Advance or Preliminary. These terms are defined as follows:

Advance: Initial estimates based on simulation and/or extrapolation from other speed grades, devices, or device families. Values are subject to change. Use as estimates, not for production.

Preliminary: Based on preliminary characterization. Further changes are not expected.

Unmarked: Specifications not identified as either Advance or Preliminary are to be considered Final.

All specifications subject to change without notice.

Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	-0.5 to +7.0	V
V_{IN}	Input voltage relative to GND (Note 1)	-0.5 to V_{CC} +0.5	V
V_{TS}	Voltage applied to 3-state output (Note 1)	-0.5 to V_{CC} +0.5	V
V_{CCt}	Longest Supply Voltage Rise Time from 1 V to 4 V	50	ms
T_{STG}	Storage temperature (ambient)	-65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in. = 1.5 mm)	+260	°C
T_J	Junction temperature	Ceramic packages	+150
		Plastic packages	+125

Notes: 1. Maximum DC overshoot or undershoot above V_{CC} or below GND must be limited to either 0.5 V or 10 mA, whichever is easier to achieve. During transitions, the device pins may undershoot to -2.0 V or overshoot to V_{CC} + 2.0 V, provided this over- or undershoot lasts less than 20 ns.
2. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{CC}	Supply voltage relative to GND, $T_J = 0^\circ\text{C}$ to $+85^\circ\text{C}$	Commercial	4.75	5.25	V
	Supply voltage relative to GND, $T_J = -40^\circ\text{C}$ to $+100^\circ\text{C}$	Industrial	4.5	5.5	V
V_{IH}	High-level input voltage	TTL inputs	2.0	V_{CC}	V
		CMOS inputs	70%	100%	V_{CC}
V_{IL}	Low-level input voltage	TTL inputs	0	0.8	V
		CMOS inputs	0	20%	V_{CC}
T_{IN}	Input signal transition time			250	ns

Notes: At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.35% per °C. Input and output measurement thresholds for TTL are 1.5 V. Input and output measurement thresholds for CMOS are 2.5 V. All timing parameters are specified for Commercial temperature range only.

DC Characteristics Over Recommended Operating Conditions

Symbol	Description		Min	Max	Units
V_{OH}	High-level output voltage @ $I_{OH} = -4.0$ mA, V_{CC} min	TTL outputs	2.4		V
	High-level output voltage @ $I_{OH} = -1.0$ mA	CMOS outputs	$V_{CC}-0.5$		V
V_{OL}	Low-level output voltage @ $I_{OL} = 12.0$ mA, V_{CC} min (Note 1)	TTL outputs		0.4	V
		CMOS outputs		0.4	V
V_{DR}	Data Retention Supply Voltage (below which configuration data may be lost)		3.0		V
I_{CCO}	Quiescent FPGA supply current (Note 2)			25	mA
I_L	Input or output leakage current		-10	+10	μ A
C_{IN}	Input capacitance (sample tested)	BGA, SBGA, PQ, HQ, MQ packages		10	pF
		PGA packages		16	pF
I_{RPU}	Pad pull-up (when selected) @ $V_{in} = 0$ V (sample tested)		0.02	0.25	mA
I_{RPD}	Pad pull-down (when selected) @ $V_{in} = 5.5$ V (sample tested)		0.02	0.25	mA
I_{RLL}	Horizontal Longline pull-up (when selected) @ logic Low		0.3	2.0	mA

Note 1: With up to 64 pins simultaneously sinking 12 mA.

Note 2: With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND.

Global Buffer Switching Characteristic Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net.

When fewer vertical clock lines are connected, the clock distribution is faster; when multiple clock lines per column are driven from the same global clock, the delay is longer. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature).

Speed Grade			-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	
From pad through Global Low Skew buffer, to any clock K	T_{GLS}	XC4028EX	9.2	7.5	6.4		ns
		XC4036EX	9.8	7.9	7.1		ns
From pad through Global Early buffer, to any clock K in same quadrant	T_{GE}	XC4028EX	5.7	4.4	4.2		ns
		XC4036EX	5.9	4.6	4.4		ns

Longline and Wide Decoder Timing Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

Horizontal Longline Switching Characteristic Guidelines

		Speed Grade	-4	-3	-2	-1	Units
Description	Symbol	Device	Max	Max	Max	Max	
TBUF driving a Horizontal Longline							
I going High or Low to Horizontal Longline going High or Low,while T is Low. Buffer is constantly active.	T _{IO1}	XC4028EX	13.7	11.3	10.9		ns
		XC4036EX	16.5	13.6	13.2		ns
T going Low to Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T _{ON}	XC4028EX	14.7	12.1	11.7		ns
		XC4036EX	17.4	14.4	14.0		ns
T going High to Horizontal Longline going from Low to High, pulled up by two resistors. (Note 1)	T _{PU2}	XC4028EX XC4036EX					ns ns
TBUF driving Half a Horizontal Longline							
I going High or Low to half of a Horizontal Longline going High or Low, while T is Low. Buffer is constantly active.	T _{HIO1}	XC4028EX	6.3	5.6	4.6		ns
		XC4036EX	7.3	6.0	5.7		ns
T going Low to half of a Horizontal Longline going from resistive pull-up or floating High to active Low. TBUF configured as open-drain or active buffer with I = Low.	T _{HON}	XC4028EX	7.2	6.4	5.4		ns
		XC4036EX	8.2	6.8	6.5		ns
T going High to half of a Horizontal Longline going from Low to High, pulled up by four resistors. (Note 1)	T _{HPU4}	XC4028EX					ns
		XC4036EX					ns

Note: These values include a minimum load of one output, spaced as far as possible from the activated pullup(s). Use the static timing analyzer to determine the delay for each destination.

Note 1: Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

Wide Decoder Switching Characteristic Guidelines

Description	Speed Grade		-4	-3	-2	-1	Units
	Symbol	Device	Max	Max	Max	Max	
Full length, two pull-ups, inputs from IOB I-pins	T _{WAF2}	XC4028EX					ns
		XC4036EX					ns
Full length, two pull-ups, inputs from internal logic	T _{WAF2L}	XC4028EX					ns
		XC4036EX					ns
Half length, two pull-ups, inputs from IOB I-pins	T _{WAO2}	XC4028EX					ns
		XC4036EX					ns
Half length, two pull-ups, inputs from internal logic	T _{WAO2L}	XC4028EX					ns
		XC4036EX					ns

Notes: These delays are specified from the decoder input to the decoder output.

Fewer than the specified number of pullup resistors can be used, if desired. Using fewer pullups reduces power consumption but increases delays. Use the static timing analyzer to determine delays if fewer pullups are used.

CLB Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

		Speed Grade		-4		-3		-2		-1		Units
Description		Symbol	Min	Max	Min	Max	Min	Max	Min	Max		
Combinatorial Delays												
F/G inputs to X/Y outputs	T _{ILO}		2.2		1.8		1.5				ns	
F/G inputs via H' to X/Y outputs	T _{IHO}		3.8		3.2		2.7				ns	
F/G inputs via transparent latch to Q outputs	T _{ITO}		3.2		2.7		2.5				ns	
C inputs via SR/H0 via H' to X/Y outputs	T _{HH0O}		3.6		3.0		2.5				ns	
C inputs via H1 via H' to X/Y outputs	T _{HH1O}		3.0		2.5		2.3				ns	
C inputs via DIN/H2 via H' to X/Y outputs	T _{HH2O}		3.6		3.0		2.5				ns	
C inputs via EC, DIN/H2 to YQ, XQ output (bypass)	T _{CBYP}		2.0		1.6		1.4				ns	
CLB Fast Carry Logic												
Operand inputs (F1, F2, G1, G4) to COUT	T _{OPCY}		4.7		3.9		3.0				ns	
Add/Subtract input (F3) to COUT	T _{ASCY}		4.5		3.7		3.7				ns	
Initialization inputs (F1, F3) to COUT	T _{INCY}		3.2		2.6		2.6				ns	
CIN through function generators to X/Y outputs	T _{SUM}		4.7		3.9		3.0				ns	
CIN to COUT, bypass function generators	T _{BYP}		0.5		0.4		0.1				ns	
Sequential Delays												
Clock K to Flip-Flop outputs Q	T _{CKO}		2.2		1.9		1.7				ns	
Clock K to Latch outputs Q	T _{CKLO}		2.2		1.9		1.7				ns	
Setup Time before Clock K												
F/G inputs	T _{IJCK}	1.4		1.2		1.2					ns	
F/G inputs via H'	T _{IHCK}	3.2		2.6		2.3					ns	
C inputs via H0 through H'	T _{HH0CK}	3.0		2.5		2.2					ns	
C inputs via H1 through H'	T _{HH1CK}	2.4		2.0		1.9					ns	
C inputs via H2 through H'	T _{HH2CK}	3.0		2.5		2.2					ns	
C inputs via DIN	T _{DICK}	1.3		1.1		1.0					ns	
C inputs via EC	T _{ECCK}	1.5		1.2		1.2					ns	
C inputs via S/R, going Low (inactive)	T _{RCK}	1.3		1.1		1.0					ns	
CIN input via F'/G'	T _{CCK}	2.5		2.1		2.3					ns	
CIN input via F'/G' and H'	T _{CHCK}	4.2		3.5		3.5					ns	
Hold Time after Clock K												
F/G inputs	T _{CKI}	0		0		0					ns	
F/G inputs via H'	T _{CKIH}	0		0		0					ns	
C inputs via SR/H0 through H'	T _{CKHH0}	0		0		0					ns	
C inputs via H1 through H'	T _{CKHH1}	0		0		0					ns	
C inputs via DIN/H2 through H'	T _{CKHH2}	0		0		0					ns	
C inputs via DIN/H2	T _{CKDI}	0		0		0					ns	
C inputs via EC	T _{CKEC}	0		0		0					ns	
C inputs via SR, going Low (inactive)	T _{CKR}	0		0		0					ns	
Clock												
Clock High time	T _{CH}	3.5		3.0		3.0					ns	
Clock Low time	T _{CL}	3.5		3.0		3.0					ns	
Set/Reset Direct												
Width (High)	T _{RPW}	3.5		3.0		3.0					ns	
Delay from C inputs via S/R, going High to Q	T _{RIO}		4.0		3.6		3.4				ns	
Global Set/Reset												
Minimum GSR Pulse Width	T _{MRW}		13.0		11.5		11.5				ns	
Delay from GSR input to any Q (XC4028EX)	T _{MRQ}		22.8		19.0		19.0				ns	
Delay from GSR input to any Q (XC4036EX)	T _{MRQ}		24.0		21.0		21.0				ns	
Toggle Frequency (Note 1)		F _{TOG}		143		166		166			MHz	

Note 1: Maximum flip-flop toggle rate for export control purposes.

CLB RAM Synchronous (Edge-Triggered) Write Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

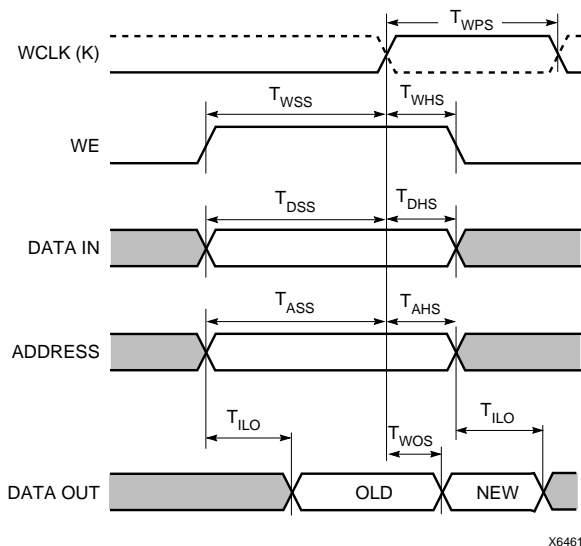
Single Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x2	T _{WCS}	11.0		9.0		9.0				ns
	32x1	T _{WCTS}	11.0		9.0		9.0				ns
Clock K pulse width (active edge)	16x2	T _{WPS}	5.5	1 ms	4.5	1 ms	4.5				ns
	32x1	T _{WPTS}	5.5	1 ms	4.5	1 ms	4.5				ns
Address setup time before clock K	16x2	T _{ASS}	2.6		2.2		2.2				ns
	32x1	T _{ASTS}	2.6		2.2		2.2				ns
Address hold time after clock K	16x2	T _{AHS}	0		0		0				ns
	32x1	T _{AHTS}	0		0		0				ns
DIN setup time before clock K	16x2	T _{DSS}	3.5		2.0		2.0				ns
	32x1	T _{DSTS}	3.0		2.5		2.5				ns
DIN hold time after clock K	16x2	T _{DHS}	0		0		0				ns
	32x1	T _{DHTS}	0		0		0				ns
WE setup time before clock K	16x2	T _{WSS}	2.4		2.0		2.0				ns
	32x1	T _{WSTS}	2.2		1.8		1.8				ns
WE hold time after clock K	16x2	T _{WHS}	0		0		0				ns
	32x1	T _{WHTS}	0		0		0				ns
Data valid after clock K	16x2	T _{WOS}		8.2		6.8		6.8			ns
	32x1	T _{WOTS}		8.4		7.0		7.0			ns

Notes: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.
Applicable Read timing specifications are identical to Level-Sensitive Read timing.

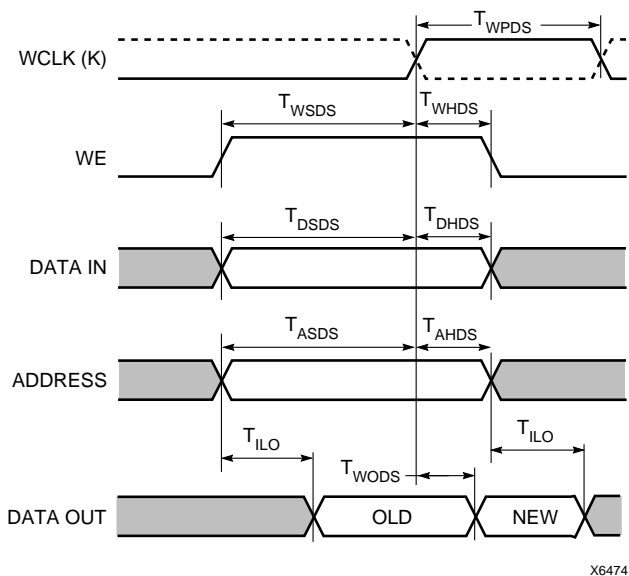
Dual-Port RAM	Speed Grade		-4		-3		-2		-1		Units
	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time (clock K period)	16x1	T _{WCDS}	11.0	1 ms	9.0	1 ms	9.0				ns
Clock K pulse width (active edge)	16x1	T _{WPDS}	5.5	1 ms	4.5	1 ms	4.5				ns
Address setup time before clock K	16x1	T _{ASDS}	3.0		2.5		2.5				ns
Address hold time after clock K	16x1	T _{AHDS}	0		0		0				ns
DIN setup time before clock K	16x1	T _{DSDS}	3.0		2.5		2.5				ns
DIN hold time after clock K	16x1	T _{DHDS}	0		0		0				ns
WE setup time before clock K	16x1	T _{WSDS}	2.2		1.8		1.8				ns
WE hold time after clock K	16x1	T _{WHDS}	0		0		0				ns
Data valid after clock K	16x1	T _{WODS}		9.4		7.8		7.8			ns

Note: Applicable Read timing specifications are identical to Level-Sensitive Read timing.

CLB RAM Synchronous (Edge-Triggered) Write Timing



CLB Dual-Port RAM Synchronous (Edge-Triggered) Write Timing



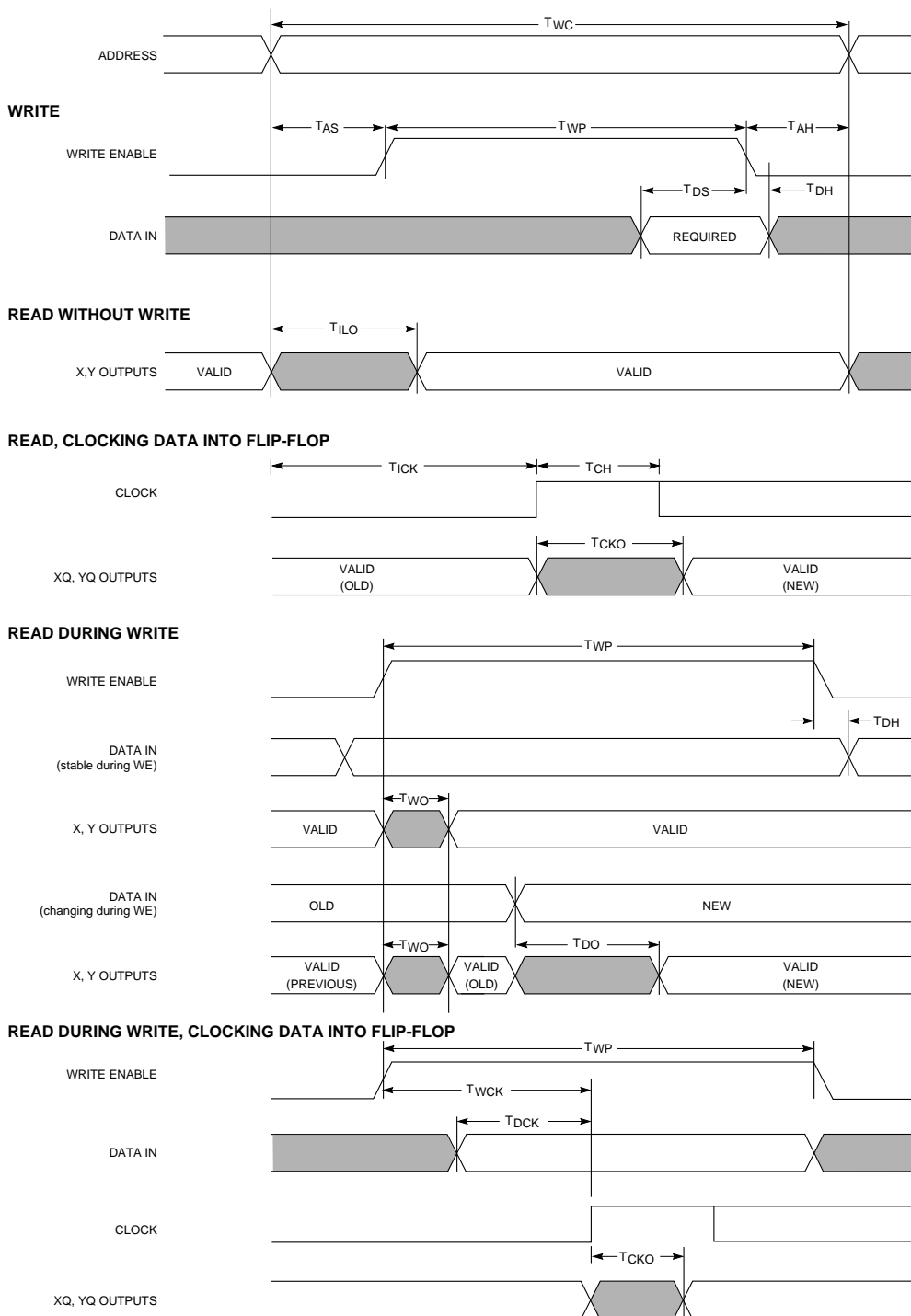
CLB RAM Asynchronous (Level-Sensitive) Write and Read Operation Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

Speed Grade			-4		-3		-2		-1		Units
Description	Size	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Write Operation											
Address write cycle time	16x2	T_{WC}	7.0		6.0		6.0				ns
	32x1	T_{WCT}	7.0		6.0		6.0				ns
Write Enable pulse width (High)	16x2	T_{WP}	3.5		3.0		3.0				ns
	32x1	T_{WPT}	3.5		3.0		3.0				ns
Address setup time before WE	16x2	T_{AS}	1.5		1.2		1.2				ns
	32x1	T_{AST}	1.6		1.4		1.4				ns
Address hold time after end of WE	16x2	T_{AH}	1.7		1.4		1.4				ns
	32x1	T_{AHT}	1.7		1.4		1.4				ns
DIN setup time before end of WE	16x2	T_{DS}	2.2		1.8		1.8				ns
	32x1	T_{DST}	2.2		1.8		1.8				ns
DIN hold time after end of WE	16x2	T_{DH}	2.3		1.9		1.9				ns
	32x1	T_{DHT}	2.3		1.9		1.9				ns
Read Operation											
Address read cycle time	16x2	T_{RC}	4.5		3.1		3.1				ns
	32x1	T_{RCT}	6.5		5.5		5.5				ns
Data valid after address change (no Write Enable)	16x2	T_{ILO}		2.2		1.8		1.5			ns
	32x1	T_{IHO}		3.8		3.2		2.7			ns
Read Operation, Clocking Data into Flip-Flop											
Address setup time before clock K	16x2	T_{ICK}	1.4		1.2		1.2				ns
	32x1	T_{IHCK}	3.1		2.6		2.6				ns
Read During Write											
Data valid after WE goes active (DIN stable before WE)	16x2	T_{WO}		2.8		2.3		2.0			ns
	32x1	T_{WOT}		2.8		2.3		2.0			ns
Data valid after DIN (DIN changes during WE)	16x2	T_{DO}		2.8		2.3		2.0			ns
	32x1	T_{DOT}		2.8		2.3		2.0			ns
Read During Write, Clocking Data into Flip-Flop											
WE setup time before clock K	16x2	T_{WCK}	2.1		1.7			1.7			ns
	32x1	T_{WCKT}	2.1		1.7			1.7			ns
Data setup time before clock K	16x2	T_{DCK}	2.1		1.7			1.7			ns
	32x1	T_{DCKT}	2.1		1.7			1.7			ns

Note: Timing for the 16x1 RAM option is identical to 16x2 RAM timing.

CLB RAM Asynchronous (Level-Sensitive) Timing Characteristics



X2640

Pin-to-Pin Output Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted.

Output Flip-Flop, Clock to Out

Description	Symbol	Device	Speed Grade				Units
			-4	-3	-2	-1	
Global Low Skew Clock to TTL Output (fast) using OFF	T_{ICKOF}	XC4028EX	16.1	13.7	12.4		ns
		XC4036EX	16.7	14.1	13.1		ns
Global Early Clock to TTL Output (fast) using OFF	T_{ICKEOF}	XC4028EX	12.6	10.6	10.2		ns
		XC4036EX	12.8	10.8	10.4		ns

OFF = Output Flip Flop

Output MUX, Clock to Out

Description	Symbol	Device	Speed Grade				Units
			-4	-3	-2	-1	
Global Low Skew Clock to TTL Output (fast) using OMUX	T_{PFPF}	XC4028EX	15.9	13.1	11.8		ns
		XC4036EX	16.5	13.5	12.5		ns
Global Early Clock to TTL Output (fast) using OMUX	T_{PEFPF}	XC4028EX	12.4	10.0	9.6		ns
		XC4036EX	12.6	10.2	9.8		ns

OMUX = Output MUX

Notes: Listed above are representative values where one global clock input drives one vertical clock line in each accessible column, and where all accessible IOB and CLB flip-flops are clocked by the global clock net. Output timing is measured at TTL threshold with 35 pF external capacitive load. Set-up time is measured with the fastest route and the lightest load. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Output Level and Slew Rate Adjustments

The following table must be used to adjust output parameters and output switching characteristics.

Description	Speed Grade		-4	-3	-2	-1	Units
	Symbol	Device	Max	Max	Max	Max	
For TTL output FAST add	T_{TTLOF}	All Devices	0	0	0		ns
For TTL output SLOW add	T_{TTLO}	All Devices	2.9	2.4	2.4		ns
For CMOS FAST output add	T_{CMOSOF}	All Devices	1.0	0.8	0.8		ns
For CMOS SLOW output add	T_{CMOSO}	All Devices	3.6	3.0	3.0		ns

Pin-to-Pin Input Parameter Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Pin-to-pin timing parameters are derived from measuring external and internal test patterns and are guaranteed over worst-case operating conditions (supply voltage and junction temperature). Listed below are representative values for typical pin locations and normal clock loading. For more specific, more precise, and worst-case guaranteed data, reflecting the actual routing structure, use the values provided by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. Values apply to all XC4000EX devices unless otherwise noted

Global Low Skew Clock, Set-Up and Hold

Description	Speed Grade		-4	-3	-2	-1	Units
	Symbol	Device	Min	Min	Min	Min	
Input Setup Time, using Global Low Skew clock and IFF (full delay)	T _{PSD}	XC4028EX	8.0	6.8	6.8		ns
		XC4036EX	8.0	6.8	6.8		ns
Input Hold Time, using Global Low Skew clock and IFF (full delay)	T _{PHD}	XC4028EX	0	0	0		ns
		XC4036EX	0	0	0		ns

IFF = Flip-Flop or Latch

Global Early Clock, Set-Up and Hold for IFF

Description	Speed Grade		-4	-3	-2	-1	Units
	Symbol	Device	Min	Min	Min	Min	
Input Setup Time, using Global Early clock and IFF (partial delay)	T _{PSEP}	XC4028EX	6.5	5.4	5.4		ns
		XC4036EX	6.5	5.4	5.4		ns
Input Hold Time, using Global Early clock and IFF (partial delay)	T _{PHEP}	XC4028EX	0	0	0		ns
		XC4036EX	0	0	0		ns

IFF = Flip-Flop or Latch

Note: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.6 ns for BUFGE #s 1, 2, 5 and 6.

Global Early Clock, Set-Up and Hold for FCL

Description	Speed Grade		-4	-3	-2	-1	Units
	Symbol	Device	Min	Min	Min	Min	
Input Setup Time, using Global Early clock and FCL (partial delay)	T _{PFSEP}	XC4028EX	6.5	5.4	5.4		ns
		XC4036EX	6.5	5.4	5.4		ns
Input Hold Time, using Global Early clock and FCL (partial delay)	T _{PFHEP}	XC4028EX	0	0	0		ns
		XC4036EX	0	0	0		ns

FCL = Fast Capture Latch

Notes: For CMOS output levels, see the Output Level and Slew Rate Adjustments tables on page 10 .

Setup time is measured with the fastest route and the lightest load. Use the static timing analyzer to determine the setup time under given design conditions. Hold time is measured using the farthest distance and a reference load of one clock pin per two IOBs. Use the static timing analyzer to determine the setup and hold times under given design conditions.

Note: Set-up parameters are for BUFGE #s 3, 4, 7 and 8. Add 1.2 ns for BUFGE #s 1, 2, 5 and 6.

Input Threshold and Slew Rate Adjustments

The following table must be used to adjust input parameters and input switching characteristics.

Description	Speed Grade		-4	-3	-2	-1	Units
	Symbol	Device	Max	Max	Max	Max	
For TTL input add	T _{TTLI}	All Devices	0	0	0		ns
For CMOS input add	T _{CMOSI}	All Devices	0.3	0.2	0.2		ns

IOB Input Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

		Speed Grade	-4	-3	-2	-1	Units
Description	Symbol	Device	Min	Min	Min	Min	
Clocks							
Delay from FCL enable (OK) active edge to IFF clock (IK) active edge	T _{OKIK}	All devices	3.2	2.6	2.6		ns
Propagation Delays			Max	Max	Max	Max	
Pad to I1, I2	T _{PID}	All devices	2.2	1.9	1.8		ns
Pad to I1, I2 via transparent input latch, no delay	T _{PLI}	All devices	3.8	3.2	3.0		ns
Pad to I1, I2 via transparent input latch, partial delay	T _{PPLI}	XC4028EX	13.3	11.1	10.9		ns
		XC4036EX	14.5	12.1	11.9		ns
Pad to I1, I2 via transparent input latch, full delay	T _{PDLI}	XC4028EX	18.2	15.2	14.9		ns
		XC4036EX	19.4	16.2	15.9		ns
Pad to I1, I2 via transparent FCL and input latch, no delay	T _{PFLI}	All devices	5.3	4.4	4.2		ns
Pad to I1, I2 via transparent FCL and input latch, partial delay	T _{PPFLI}	XC4028EX	13.6	11.3	11.1		ns
		XC4036EX	14.8	12.3	12.1		ns
Propagation Delays							
Clock (IK) to I1, I2 (flip-flop)	T _{IKRI}	All devices	3.0	2.5	2.4		ns
Clock (IK) to I1, I2 (latch enable, active Low)	T _{IKLI}	All devices	3.2	2.7	2.6		ns
FCL Enable (OK) active edge to I1, I2 (via transparent standard input latch)	T _{OKLI}	All devices	6.2	5.2	5.0		ns
Global Set/Reset							
Minimum GSR Pulse Width	T _{MRW}	All devices	13.0	11.5	11.5		ns
Delay from GSR input to any Q	T _{RRI}	XC4028EX	22.8	19.0	19.0		ns
Delay from GSR input to any Q	T _{RRI}	XC4036EX	24.0	21.0	21.0		ns

FCL = Fast Capture Latch, IFF = Input Flip-Flop or Latch

Notes: For CMOS output levels, see the Output Level and Slew Rate Adjustments table on page 10.

For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 11.

IOB Input Switching Characteristic Guidelines (Continued)

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). Values apply to all XC4000EX devices unless otherwise noted.

Speed Grade			-4	-3	-2	-1	Units
Description	Symbol	Device	Min	Min	Min	Min	
Setup Times							
Pad to Clock (IK), no delay	T _{PICK}	All devices	2.5	2.0	2.0		ns
Pad to Clock (IK), partial delay	T _{PICKP}	XC4028EX	10.8	9.0	9.0		ns
		XC4036EX	12.0	10.0	10.0		ns
Pad to Clock (IK), full delay	T _{PICKD}	XC4028EX	15.7	13.1	13.1		ns
		XC4036EX	16.9	14.1	14.1		ns
Pad to Clock (IK), via transparent Fast Capture Latch, no delay	T _{PICKF}	All devices	3.9	3.3	3.3		ns
Pad to Clock (IK), via transparent Fast Capture Latch, partial delay	T _{PICKFP}	XC4028EX	12.3	10.2	10.2		ns
		XC4036EX	13.5	11.2	11.2		ns
Pad to Fast Capture Latch Enable (OK), no delay	T _{POCK}	All devices	0.8	0.7	0.7		ns
Pad to Fast Capture Latch Enable (OK), partial delay	T _{POCKP}	XC4028EX	9.1	7.6	7.6		ns
		XC4036EX	10.3	8.6	8.6		ns
Setup Times (TTL or CMOS Inputs)							
Clock Enable (EC) to Clock (IK)	T _{ECIK}	All devices	0.3	0.2	0.2		ns
Hold Times							
Pad to Clock (IK), no delay partial delay full delay	T _{IKPI}	All devices	0	0	0		ns
	T _{IKPIP}	All devices	0	0	0		ns
	T _{IKPID}	All devices	0	0	0		ns
Pad to Clock (IK) via transparent Fast Capture Latch, no delay partial delay full delay	T _{IKFPI}	All devices	0	0	0		ns
	T _{IKFPIP}	All devices	0	0	0		ns
	T _{IKFPID}	All devices	0	0	0		ns
Clock Enable (EC) to Clock (IK), no delay partial delay full delay	T _{IKEC}	All devices	0	0	0		ns
	T _{IKECP}	All devices	0	0	0		ns
	T _{IKECD}	All devices	0	0	0		ns
Pad to Fast Capture Latch Enable (OK), no delay partial delay	T _{OKPI}	All devices	0	0	0		ns
	T _{OKPIP}	All devices	0	0	0		ns

Notes: For CMOS output levels, see the Output Level and Slew Rate Adjustments table on page 10.

For setup and hold times with respect to the clock input pin, see the Global Low Skew Clock and Global Early Clock Set-up and Hold tables on page 11.

IOB Output Switching Characteristic Guidelines

Testing of switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Internal timing parameters are derived from measuring internal test patterns. Listed below are representative values. For more specific, more precise, and worst-case guaranteed data, use the values reported by the static timing analyzer (TRCE in the Xilinx Development System) and back-annotated to the simulation netlist. These path delays, provided as a guideline, have been extracted from the static timing analyzer report. All timing parameters assume worst-case operating conditions (supply voltage and junction temperature). For Propagation Delays, slew-rate = fast unless otherwise noted. Values apply to all XC4000EX devices unless otherwise noted.

Speed Grade		-4		-3		-2		-1		Units
Description	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	
Propagation Delays										
Clock (OK) to Pad	T _{OKPOF}		7.4		6.2		6.0			ns
Output (O) to Pad	T _{OPF}		6.2		5.2		5.0			ns
3-state to Pad hi-Z (slew-rate independent)	T _{TSHZ}		4.9		4.1		4.1			ns
3-state to Pad active and valid	T _{TSO NF}		6.2		5.2		5.0			ns
Output MUX Select (OK) to Pad	T _{OKFPF}		6.7		5.6		5.4			ns
Fast Path Output MUX Input (EC) to Pad	T _{CEFPF}		6.2		5.1		5.0			ns
Slowest Path Output MUX Input (O) to Pad	T _{OFFP}		7.3		6.0		5.9			ns
Setup and Hold Times										
Output (O) to clock (OK) setup time	T _{OOK}	0.6		0.5		0.5				ns
Output (O) to clock (OK) hold time	T _{OKO}	0		0		0				ns
Clock Enable (EC) to clock (OK) setup	T _{ECOK}	0		0		0				ns
Clock Enable (EC) to clock (OK) hold	T _{OKEC}	0		0		0				ns
Clock										
Clock High	T _{CH}	3.5		3.0		3.0				ns
Clock Low	T _{CL}	3.5		3.0		3.0				ns
Global Set/Reset										
Minimum GSR pulse width	T _{MRW}	13.0		11.5		11.5				ns
Delay from GSR input to any Pad (XC4028EX)	T _{RP O}	28.8		24.0		24.0				ns
Delay from GSR input to any Pad (XC4036EX)	T _{RP O}	30.0		26.0		26.0				ns

Notes: Output timing is measured at TTL threshold, with 35pF external capacitive loads.

For CMOS output levels, see the Output Level and Slew Rate Adjustments table on page 10

XC4000EX Output I/V Characteristics

Pull-down (Sink) (Voltage measured upward from ground)

Voltage	I(Typ)	I(Min)	I(Max)
0.100	8.284e-03	7.037e-03	9.525e-03
0.200	1.636e-02	1.387e-02	1.885e-02
0.300	2.423e-02	2.049e-02	2.797e-02
0.400	3.189e-02	2.690e-02	3.689e-02
0.500	3.934e-02	3.310e-02	4.560e-02
0.600	4.657e-02	3.909e-02	5.410e-02
0.700	5.359e-02	4.487e-02	6.239e-02
0.800	6.040e-02	5.043e-02	7.047e-02
0.900	6.699e-02	5.579e-02	7.834e-02
1.000	7.337e-02	6.093e-02	8.599e-02
1.200	8.546e-02	7.058e-02	1.006e-01
1.400	9.668e-02	7.938e-02	1.144e-01
1.600	1.070e-01	8.733e-02	1.273e-01
1.800	1.165e-01	9.442e-02	1.393e-01
2.000	1.250e-01	1.007e-01	1.503e-01
2.200	1.327e-01	1.061e-01	1.605e-01
2.400	1.394e-01	1.106e-01	1.697e-01
2.600	1.453e-01	1.143e-01	1.779e-01
2.800	1.503e-01	1.170e-01	1.853e-01
3.000	1.540e-01	1.188e-01	1.917e-01
3.200	1.562e-01	1.200e-01	1.965e-01
3.400	1.577e-01	1.209e-01	1.992e-01
3.600	1.588e-01	1.216e-01	2.009e-01
3.800	1.597e-01	1.222e-01	2.021e-01
4.000	1.603e-01	1.227e-01	2.030e-01
4.200	1.609e-01	1.231e-01	2.037e-01
4.400	1.614e-01	1.235e-01	2.043e-01
4.600	1.618e-01	1.238e-01	2.048e-01
4.800	1.622e-01	1.242e-01	2.053e-01
5.000	1.625e-01	1.245e-01	2.057e-01

Note: Values equal maximum sink current at V_{CC} .

Values are based on Spice simulation and can change without notice, especially when designs are migrated to a new process or foundry.

Pull-up (Source) (Voltage measured downward from ground)

Voltage	I(Typ)	I(Min)	I(Max)
0.100	-9.722e-04	-8.605e-04	-1.085e-03
0.200	-1.931e-03	-1.706e-03	-2.159e-03
0.300	-2.857e-03	-2.536e-03	-3.220e-03
0.400	-3.806e-03	-3.350e-03	-4.269e-03
0.500	-4.722e-03	-4.148e-03	-5.305e-03
0.600	-5.623e-03	-4.930e-03	-6.328e-03
0.700	-6.510e-03	-5.695e-03	-7.338e-03
0.800	-7.381e-03	-6.444e-03	-8.335e-03
0.900	-8.236e-03	-7.175e-03	-9.317e-03
1.000	-9.076e-03	-7.892e-03	-1.029e-02
1.200	-1.077e-02	-9.436e-03	-1.219e-02
1.400	-1.313e-02	-1.207e-02	-1.448e-02
1.600	-1.787e-02	-1.647e-02	-1.918e-02
1.800	-2.427e-02	-2.208e-02	-2.653e-02
2.000	-3.184e-02	-2.861e-02	-3.539e-02
2.200	-4.026e-02	-3.586e-02	-4.526e-02
2.400	-4.931e-02	-4.367e-02	-5.580e-02
2.600	-5.882e-02	-5.192e-02	-6.680e-02
2.800	-6.689e-02	-6.052e-02	-7.812e-02
3.000	-7.883e-02	-6.941e-02	-8.966e-02
3.200	-8.916e-02	-7.853e-02	-1.013e-01
3.400	-9.964e-02	-8.783e-02	-1.131e-01
3.600	-1.102e-01	-9.730e-02	-1.249e-01
3.800	-1.209e-01	-1.070e-01	-1.368e-01
4.000	-1.316e-01	-1.169e-01	-1.486e-01
4.200	-1.370e-01	-1.219e-01	-1.545e-01
4.400	-1.534e-01	-1.373e-01	-1.722e-01
4.600	-1.645e-01	-1.477e-01	-1.840e-01
4.800	-1.757e-01	-1.577e-01	-1.959e-01
5.000	-1.870e-01	-1.670e-01	-2.078e-01

Note: Values equal maximum source current at V_{CC} .