

Features

- Ultra-high-speed FPGA family with two members
 - 50-85 MHz system clock rates
 - 270 to 325 MHz guaranteed flip-flop toggle rates
 - 2.2 to 2.7 ns logic delays
- 4 mA output sink current and 4 mA source current
- JEDEC compliant 3.3 V version of XC3100A FPGA family
- The XC3100L is 100% architecture, pin-out and bitstream compatible with the XC3000A, XC3000L and XC3100A families
- Advanced, 0.6 μ TLM CMOS technology
- XC3100L combines the features of the XC3000L and XC3100A families.
- Additional interconnect resources for TBUFs and CE inputs
- Error checking of the configuration bitstream
- Soft startup holds all outputs slew-rate limited during initial power-up
- More advanced CMOS process

Description

XC3100L is a performance-optimized relative of the XC3000L and XC3100A families. While all families are footprint compatible, the XC3100L family extends the typical system performance beyond 80 MHz.

The XC3100L family follows the XC4000 speed-grade nomenclature, indicating device performance with a number that is based on the internal logic-block delay, in ns.

The XC3100L family offers the following enhancements over the popular XC3000 family.

The XC3100L family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3100L devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in all XC3000 families, determined by the individual configuration option.

Any bitstream used to configure an XC3000, XC3000A, XC3000L or XC3100A device, will configure the same-size XC3100L device exactly the same way.

Device	Max Logic Gates	Typical Gate Range	CLBs	Array	User I/Os Max	Flip-Flops	Horizontal Longlines	Configuration Data Bits
XC3142L	3,000	2,000 - 3,000	144	12 x 12	96	480	24	30,784
XC3190L	6,000	5,000 - 6,000	320	16 x 20	144	928	40	64,160

XC3100L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3100L Operating Conditions

Symbol	Description	Min	Max	Units
V_{CC}	Supply voltage relative to GND Commercial 0°C to +85°C junction	3.0	3.6	V
V_{IH}	High-level input voltage	2.0	$V_{CC} + 0.3$	V
V_{IL}	Low-level input voltage	-0.3	0.8	V
T_{IN}	Input signal transition time		250	ns

- Notes:**
1. At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
 2. Although the present (1996) devices operate over the full supply voltage range from 3.0 V to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 and 3.6 V range later, when smaller device geometries might preclude operation @ 5 V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3100L DC Characteristics Over Operating Conditions

Symbol	Description	Min	Max	Units
V_{OH}	High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min)	2.4		V
	High-level output voltage (@ $I_{OH} = -100.0$ μ A, V_{CC} min)	$V_{CC} - 0.2$		V
V_{OL}	Low-level output voltage (@ $I_{OH} = 4.0$ mA, V_{CC} min)		0.40	V
	Low-level output voltage (@ $I_{OH} = +100.0$ μ A, V_{CC} min)		0.2	V
V_{CCPD}	Power-down supply voltage (PWRDWN must be Low)	2.30		V
I_{CCO}	Quiescent FPGA supply current Chip thresholds programmed as CMOS levels ¹		1.5	mA
I_{IL}	Input Leakage Current	-10	+10	μ A
C_{IN}	Input capacitance, all packages except PGA175 (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		10 15	pF pF
	Input capacitance, PGA175 (sample tested) All pins except XTL1 and XTL2 XTL1 and XTL2		15 20	pF pF
I_{RIN}	Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested)	0.02	0.17	mA
I_{RLL}	Horizontal long line pull-up (when selected) @ logic Low	0.20	2.80	mA

- Notes:**
1. With no output current loads, no active input or long line pull-up resistors, all package pins at V_{CC} or GND, and the FPGA configured with a MakeBits tie option.
 2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source current may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3142L to the XC3190L.

XC3100L Absolute Maximum Ratings

Symbol	Description		Units
V_{CC}	Supply voltage relative to GND	–0.5 to +7.0	V
V_{IN}	Input voltage with respect to GND	–0.5 to $V_{CC} + 0.5$	V
V_{TS}	Voltage applied to 3-state output	–0.5 to $V_{CC} + 0.5$	V
T_{STG}	Storage temperature (ambient)	–65 to +150	°C
T_{SOL}	Maximum soldering temperature (10 s @ 1/16 in.)	+260	°C
T_J	Junction temperature plastic	+125	°C
	Junction temperature ceramic	+150	°C

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3100L Global Buffer Switching Characteristics Guidelines

		Speed Grade	-3	-2	
Description	Symbol		Max	Max	Units
Global and Alternate Clock Distribution ¹ Either: Normal IOB input pad through clock buffer to any CLB or IOB clock input Or: Fast (CMOS only) input pad through clock buffer to any CLB or IOB clock input	T_{PID}		5.6	4.7	ns
	T_{PIDC}		4.3	3.7	ns
TBUF driving a Horizontal Longline (L.L.) ¹ I to L.L. while T is Low (buffer active) T↓ to L.L. active and valid with single pull-up resistor T↑ to L.L. High with single pull-up resistor	T_{IO}		3.1	3.1	ns
	T_{ON}		4.2	4.2	ns
	T_{PUS}		11.4	11.4	ns
BIDI Bidirectional buffer delay	T_{BIDI}		1.0	0.9	ns
			Advance		

Notes: 1. Timing is based on the XC3142L, for other devices see XACT timing calculator.
2. The use of two pull-up resistors per longline, available on other XC3000 devices, is not a valid option for XC3100L devices.

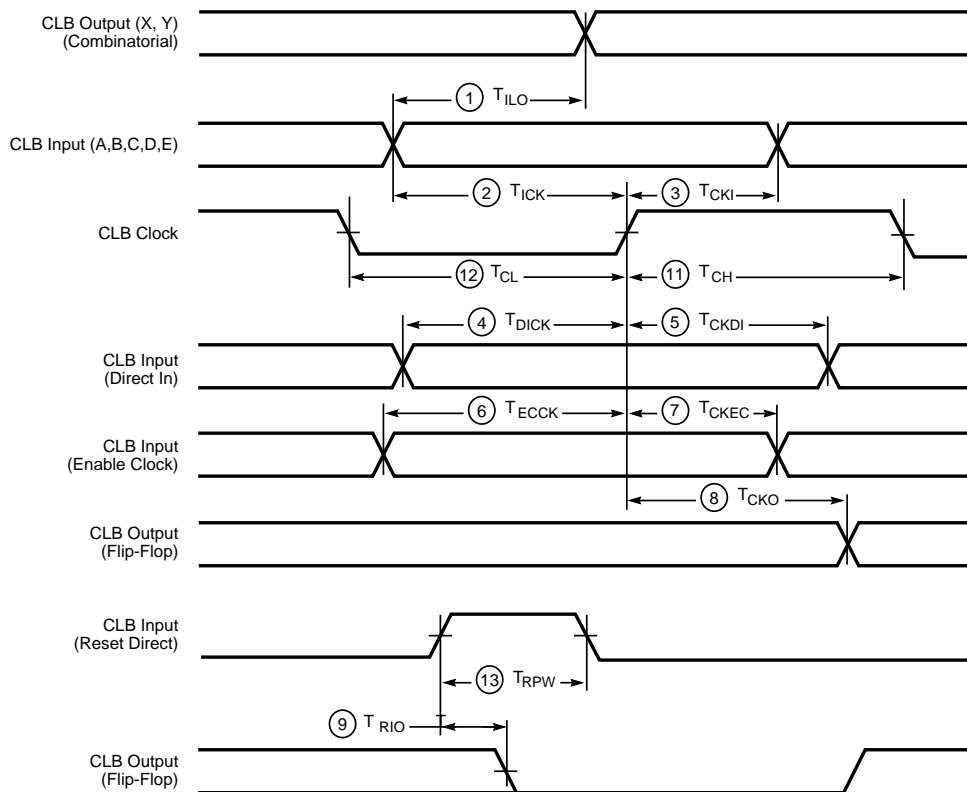
XC3100L CLB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

Speed Grade			-3		-2		Units
Description	Symbol		Min	Max	Min	Max	
Combinatorial Delay Logic Variables A, B, C, D, E, to outputs X or Y	1	T_{ILO}		2.7		2.2	ns
Sequential delay Clock k to outputs X or Y	8	T_{CKO}		2.1		1.7	ns
Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y		T_{QLO}		4.3		3.5	ns
Set-up time before clock K Logic Variables A, B, C, D, E	2	T_{ICK}	2.1		1.8		ns
Data In DI	4	T_{DICK}	1.4		1.3		ns
Enable Clock EC	6	T_{ECCK}	2.7		2.5		ns
Reset Direct Inactive RD			1.0		1.0		ns
Hold Time after clock K Logic Variables A, B, C, D, E	3	T_{CKI}	0		0		ns
Data In DI	5	T_{CKDI}	0.9		0.9		ns
Enable Clock EC	7	T_{CKEC}	0.7		0.7		ns
Clock Clock High time	11	T_{CH}	1.6		1.3		ns
Clock Low time	12	T_{CL}	1.6		1.3		ns
Max. flip-flop toggle rate		F_{CLK}	270		325		MHz
Reset Direct (RD) RD width	13	T_{RPW}	2.7		2.3		ns
delay from RD to outputs X or Y	9	T_{RIO}		3.1		2.7	ns
Global Reset (\overline{RESET} Pad) \overline{RESET} width (Low) (XC3142L) delay from \overline{RESET} pad to outputs X or Y		T_{MRW} T_{MRQ}	12.0	12.0	12.0	12.0	ns ns
Advance							

- Notes:
1. The CLB K to Q delay (T_{CKO} , #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI} , #5) of any CLB on the same die.
 2. T_{ILO} , T_{QLO} and T_{ICK} are specified for 4-input functions. For 5-input functions or base FGM functions, each of these specifications for the XC3100L family increase by 0.35 ns (-3) and 0.29 ns (-2).

XC3100L CLB Switching Characteristics Guidelines (continued)



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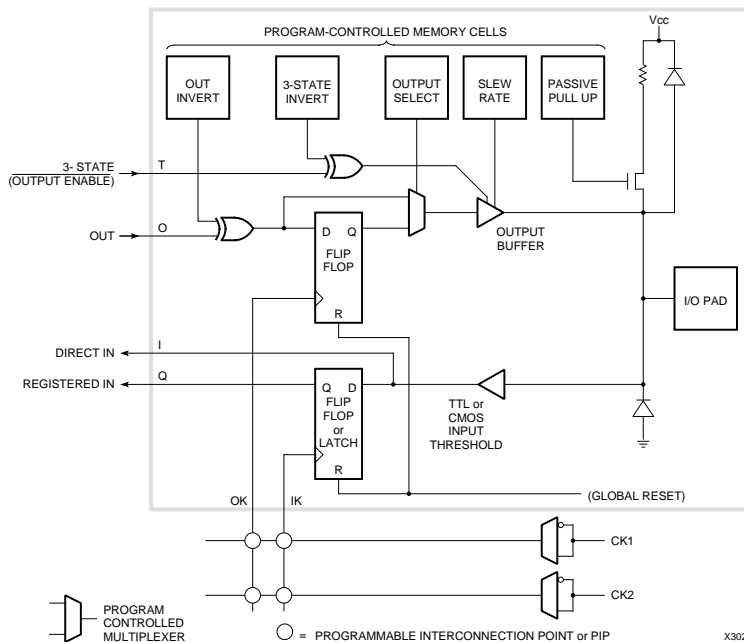
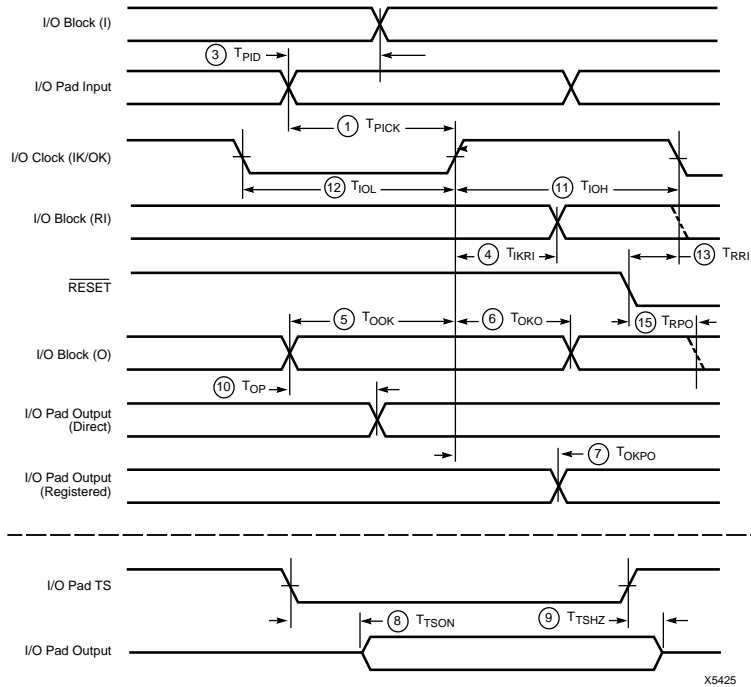
XC3100L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

		Speed Grade	-3		-2		
Description		Symbol	Min	Max	Min	Max	Units
Propagation Delays (Input)							
Pad to Direct In (I)	3	T _{PID}		2.2		2.0	ns
Pad to Registered In (Q) with latch (XC3100L) transparent		T _{PTG}		11.0		11.0	ns
Clock (IK) to Registered In (Q)	4	T _{IKRI}		2.2		1.9	ns
Set-up Time (Input)							
Pad to Clock (IK) set-up time	1	T _{PICK}					
XC3142L			9.5		9.0		ns
XC3190L			9.9		9.4		ns
Propagation Delays (Output)							
Clock (OK) to Pad (fast)	7	T _{OKPO} T _{OK}		4.4		4.0	ns
same (slew rate limited)	7	T _{PO}		10.0		9.7	ns
Output (O) to Pad (fast)	10	T _{OPF}		3.3		3.0	ns
same (slew-rate limited)(XC3100L)	10	T _{OPF}		9.0		8.7	ns
3-state to Pad begin hi-Z (fast)	9	T _{TSHZ}		5.5		5.0	ns
same (slew-rate limited)	9	T _{TSHZ}		5.5		5.0	ns
3-state to Pad active and valid (fast)(XC3100L)	8	T _{TSON}		9.0		8.5	ns
same (slew -rate limited)	8	T _{TSON}		15.0		14.2	ns
Set-up and Hold Times (Output)							
Output (O) to clock (OK) set-up time (XC3100L)	5	T _{OOK}	4.0		3.6		ns
Output (O) to clock (OK) hold time	6	T _{OKO}	0		0		ns
Clock							
Clock High time	11	T _{IOH}	1.6		1.3		ns
Clock Low time	12	T _{IOL}	1.6		1.3		ns
Export Control Maximum flip-flop toggle rate		F _{TOG}	270		325		MHz
Global Reset Delays							
RESET Pad to Registered In (Q) (XC3142L)	13	T _{RRRI}		16.0		16.0	ns
(XC3190L)				21.0		21.0	ns
RESET Pad to output pad (fast)	15	T _{RPO}		17.0		17.0	ns
(slew-rate limited)	15	T _{RPO}		23.0		23.0	ns
Advance							

- Notes:**
- Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
 - Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
 - Input pad set-up time is specified with respect to the internal clock (IK). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (IK) is negative. This means that pad level changes immediately before the internal clock edge (IK) will not be recognized.

XC3100L IOB Switching Characteristics Guidelines (continued)



Product Availability

PINS		44	64	68	84		100			
TYPE		PLAST. PLCC	PLAST. VQFP	PLAST. PLCC	PLAST. PLCC	CERAM PGA	PLAST. PQFP	PLAST. TQFP	PLAST. VQFP	TOP- BRAZED CQFP
CODE		PC44	VQ64	PC68	PC84	PG84	PQ100	TQ100	VQ100	CB100
XC3142L	-3				C				C	
	-2				C				C	
XC3190L	-3				C					
	-2				C					
	Adv.									

PINS		132		144	160	164	175		176	208	223
TYPE		PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	TOP- BRAZED CQFP	PLAST. PGA	CERAM. PGA	PLAST. TQFP	PLAST. PQFP	CERAM. PGA
CODE		PP132	PG132	TQ144	PQ160	CB164	PP175	PG175	TQ176	PQ208	PG223
XC3142L	-3			C							
	-2			C							
XC3190L	-3			C					C		
	-2			C					C		
	Adv.										

Note: C = Commercial, $T_J = 0^\circ$ to $+85^\circ\text{C}$

Ordering Information

Example:

XC3142L-3PC84C

