

Features

- Part of the Zero+ family of 3.3 V FPGAs
 - JEDEC-compliant 3.3 V version of the XC3000A FPGA family
 - Logic densities from 1,000 to 6,000 gates
 - Up to 144 user-definable I/Os
- Advanced, low power 0.8 μ and 0.6 μ CMOS static memory technology
 - Very low quiescent current consumption, $\leq 20\mu$ A
 - Operating power consumption 56% less than XC3000A, 66% less than previous generation 5 V FPGAs
- Superset of the industry-leading XC3000 family
 - Identical to the basic XC3000A in structure, pinout, design methodology, and software tools
 - 100% compatible with all XC3000, XC3000A, XC3100L and XC3100A bitstreams
 - Improved routing and additional features
- Additional programmable interconnection points (PIPs)
 - Improved access to Longlines and CLB clock enable inputs
 - Most efficient XC3000-class solution to bus-oriented designs
- XC3000L-specific features
 - Guaranteed over the 3.0 to 3.6 V V_{cc} range
 - 4 mA output sink and source current
 - Error checking of the configuration bitstream
 - Soft startup starts all outputs in slew-limited mode upon power-up
 - Easy migration to the XC3400 series of HardWire mask programmed devices for high-volume production

Description

The XC3000L family of FPGAs is optimized for operation from a nominally 3.3 V supply. Aside from the electrical and timing parameters listed in this data sheet, the XC3000L

family is in all respects identical with the XC3000A family, and is a superset of the XC3000 family.

The operating power consumption of Xilinx FPGAs is almost exclusively dynamic, and it changes with the square of the supply voltage. For a given complexity and clock speed, the XC3000L consumes, therefore, only 44% of the power used by the equivalent XC3000A device. In accordance with its use in battery-powered equipment, the XC3000L family was designed for the lowest possible power-down and quiescent current consumption.

In mixed supply-voltage systems, the XC3000L, fed by a 3.3 V (nominal) supply, can directly drive any device with TTL-like input thresholds. When a 5 V device drives the XC3000L, a current-limiting resistor (1 k Ω) or a voltage divider is required to prevent excessive input current.

Like the XC3000A family, XC3000L offers the following functional improvements over the popular XC3000 family:

The XC3000L family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000L devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

The XC3000L family is a superset of the XC3000 family. Any bitstream used to configure an XC3000 device configures an XC3000L device the same way.

| Device | Max Logic Gates | Typical Gate Range | CLBs | Array | User I/Os Max | Flip-Flops | Horizontal Longlines | Configuration Data Bits |
|---------|-----------------|--------------------|------|---------|---------------|------------|----------------------|-------------------------|
| XC3020L | 1,500 | 1,000 - 1,500 | 64 | 8 x 8 | 64 | 256 | 16 | 14,779 |
| XC3030L | 2,000 | 1,500 - 2,000 | 100 | 10 x 10 | 80 | 360 | 20 | 22,176 |
| XC3042L | 3,000 | 2,000 - 3,000 | 144 | 12 x 12 | 96 | 480 | 24 | 30,784 |
| XC3064L | 5,000 | 4,000 - 5,000 | 224 | 16 x 14 | 120 | 688 | 32 | 46,064 |
| XC3090L | 6,000 | 5,000 - 6,000 | 320 | 16 x 20 | 144 | 928 | 40 | 64,160 |

XC3000L Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

XC3000L Operating Conditions

| Symbol | Description | Min | Max | Units |
|----------|---|------|--------------|-------|
| V_{CC} | Supply voltage relative to GND Commercial 0°C to +85°C junction | 3.0 | 3.6 | V |
| V_{IH} | High-level input voltage — TTL configuration | 2.0 | $V_{CC}+0.3$ | V |
| V_{IL} | Low-level input voltage — TTL configuration | -0.3 | 0.8 | V |
| T_{IN} | Input signal transition time | | 250 | ns |

- Notes:**
- At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.
 - Although the present (1996) devices operate over the full supply voltage range from 3.0 to 5.25 V, Xilinx reserves the right to restrict operation to the 3.0 to 6.0 V range later, when smaller device geometries might preclude operation at 5V. Operating conditions are guaranteed in the 3.0 – 3.6 V V_{CC} range.

XC3000L DC Characteristics Over Operating Conditions

| Symbol | Description | Min | Max | Units |
|------------|--|----------------|----------|----------|
| V_{OH} | High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min) | 2.40 | | V |
| V_{OL} | Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min) | | 0.40 | V |
| V_{OH} | High-level output voltage (@ $I_{OH} = -4.0$ mA, V_{CC} min) | $V_{CC} - 0.2$ | | V |
| V_{OL} | Low-level output voltage (@ $I_{OL} = 4.0$ mA, V_{CC} min) | | 0.2 | V |
| V_{CCPD} | Power-down supply voltage (PWRDWN must be Low) | 2.30 | | V |
| I_{CCPD} | Power-down supply current ($V_{CC(MAX)}$ @ T_{MAX}) | | 10 | μA |
| I_{CCO} | Quiescent FPGA supply current in addition to I_{CCPD}^1 Chip thresholds programmed as CMOS levels | | 20 | μA |
| I_{IL} | Input Leakage Current | -10 | +10 | μA |
| C_{IN} | Input capacitance, all packages except PGA175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2 | | 10 15 | pF pF |
| | Input capacitance, PGA 175 (sample tested) All Pins except XTL1 and XTL2 XTL1 and XTL2 | | 15 20 | pF pF |
| I_{RIN} | Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested) | 0.02 | 0.17 | mA |
| I_{RLL} | Horizontal Longline pull-up (when selected) @ logic Low | | 2.50 | mA |

- Notes:**
- With no output current loads, no active input or Longline pull-up resistors, all package pins at V_{CC} or GND, and the FPGA device configured with a MakeBits tie option. I_{CCO} is in addition to I_{CCPD} .
 - Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per V_{CC} pin. The number of ground pins varies from the XC3020L to the XC3090L.

XC3000L Absolute Maximum Ratings

| Symbol | Description | | Units |
|-----------|---|------------------------|-------|
| V_{CC} | Supply voltage relative to GND | −0.5 to +7.0 | V |
| V_{IN} | Input voltage with respect to GND | −0.5 to $V_{CC} + 0.5$ | V |
| V_{TS} | Voltage applied to 3-state output | −0.5 to $V_{CC} + 0.5$ | V |
| T_{STG} | Storage temperature (ambient) | −65 to +150 | °C |
| T_{SOL} | Maximum soldering temperature (10 s @ 1/16 in.) | +260 | °C |
| T_J | Junction temperature plastic | +125 | °C |
| | Junction temperature ceramic | +150 | °C |

Note: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

XC3000L Global Buffer Switching Characteristics Guidelines

| | | Speed Grade | -8 | |
|--|-----------------------------------|---------------------|----------------|--|
| Description | Symbol | Max | Units | |
| Global and Alternate Clock Distribution ¹ Either: Normal IOB input pad through clock buffer to any CLB or IOB clock input Or: Fast (CMOS only) input pad through clock buffer to any CLB or IOB clock input | T_{PID} | 9.0 | ns | |
| | T_{PIDC} | 7.0 | ns | |
| TBUF driving a Horizontal Longline (L.L.) ¹ I to L.L. while T is Low (buffer active) T↓ to L.L. active and valid with single pull-up resistor T↑ to L.L. High with single pull-up resistor | T_{IO} T_{ON} T_{PUS} | 5.0 12.0 24.0 | ns ns ns | |
| BIDI Bidirectional buffer delay | T_{BIDI} | 2.0 | ns | |

1. Timing is based on the XC3042A, for other devices see XACT timing calculator.

2. The use of two pull-up resistors per Longline, available on other XC3000 devices, is not a valid option for XC3000L devices.

XC3000L CLB Switching Characteristics Guidelines

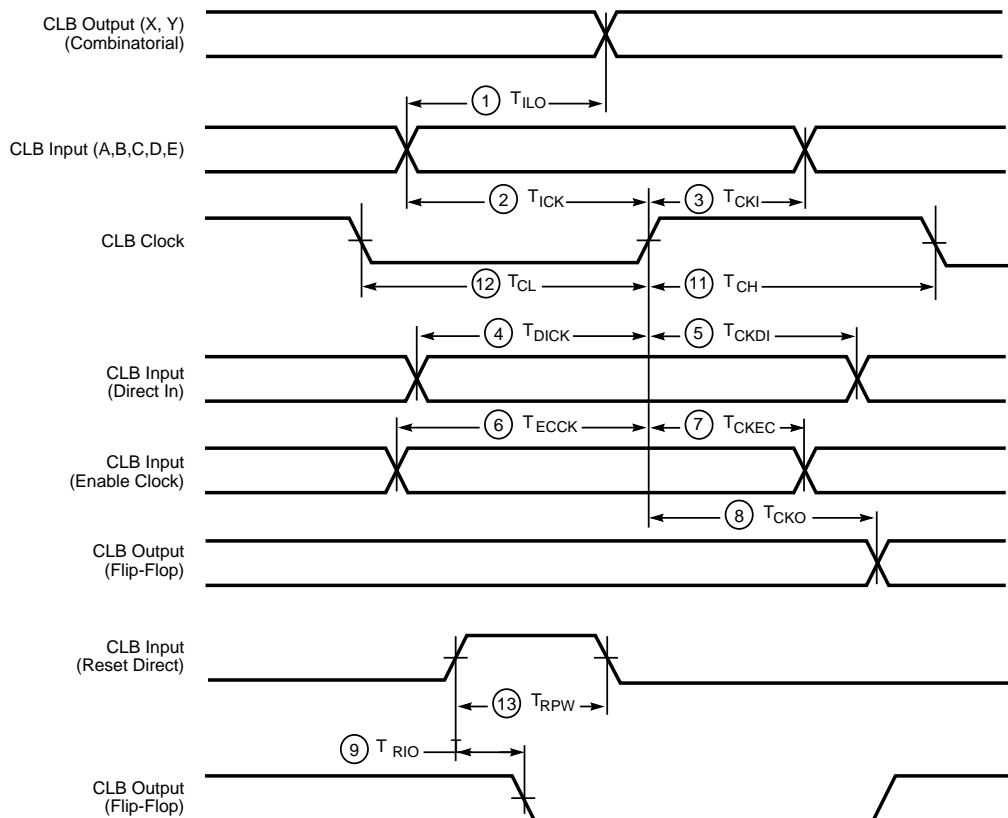
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

| | | Speed Grade | | -8 | | |
|--|--|-------------|------------------------|------------|--------------|----------|
| Description | | Symbol | | Min | Max | Units |
| Combinatorial Delay Logic Variables A, B, C, D, E, to outputs X or Y FG Mode F and FGM Mode | | 1 | T_{ILO} | | 6.7 7.5 | ns ns |
| | | 8 | T_{CKO} | | 7.5 | ns |
| | | | T_{QLO} | | 14.0 14.8 | ns ns |
| Sequential delay Clock k to outputs X or Y Clock k to outputs X or Y when Q is returned through function generators F or G to drive X or Y FG Mode F and FGM Mode | | | | | | |
| | | | | | | |
| | | | | | | |
| | | | | | | |
| Set-up time before clock K Logic Variables A, B, C, D, E FG Mode F and FGM Mode Data In DI Enable Clock EC | | 2 | T_{ICK} | 5.0 5.8 | | ns ns |
| | | 4 | T_{DICK} | 5.0 | | ns |
| | | 6 | T_{ECCK} | 6.0 | | ns |
| | | | | | | |
| Hold Time after clock K Logic Variables A, B, C, D, E Data In DI ² Enable Clock EC | | 3 | T_{CKI} | 0 | | ns |
| | | 5 | T_{CKDI} | 2.0 | | ns |
| | | 7 | T_{CKEC} | 2.0 | | ns |
| Clock Clock High time Clock Low time Max. flip-flop toggle rate | | 11 | T_{CH} | 5.0 | | ns |
| | | 12 | T_{CL} | 5.0 | | ns |
| | | | F_{CLK} | 80.0 | | MHz |
| Reset Direct (RD) RD width delay from RD to outputs X or Y | | 13 | T_{RPW} | 7.0 | | ns |
| | | 9 | T_{RIO} | 7.0 | | ns |
| Global Reset (\overline{RESET} Pad) ¹ \overline{RESET} width (Low) delay from \overline{RESET} pad to outputs X or Y | | | T_{MRW} T_{MRQ} | 16.0 | | ns ns |
| | | | | | 23.0 | |

Notes: 1. Timing is based on the XC3042L, for other devices see XACT timing calculator.

2. The CLB K to Q output delay (T_{CKO} , #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement (T_{CKDI} , #5) of any CLB on the same die.

XC3000L CLB Switching Characteristics Guidelines (continued)



X5424

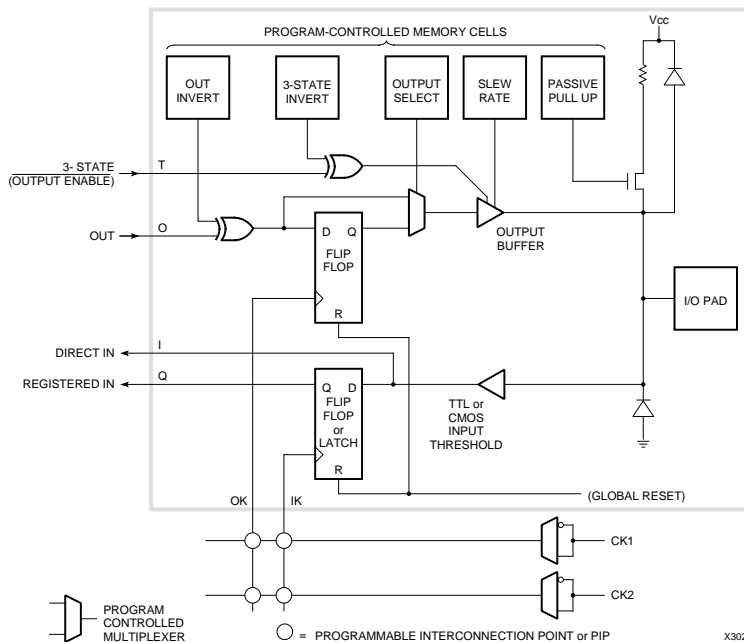
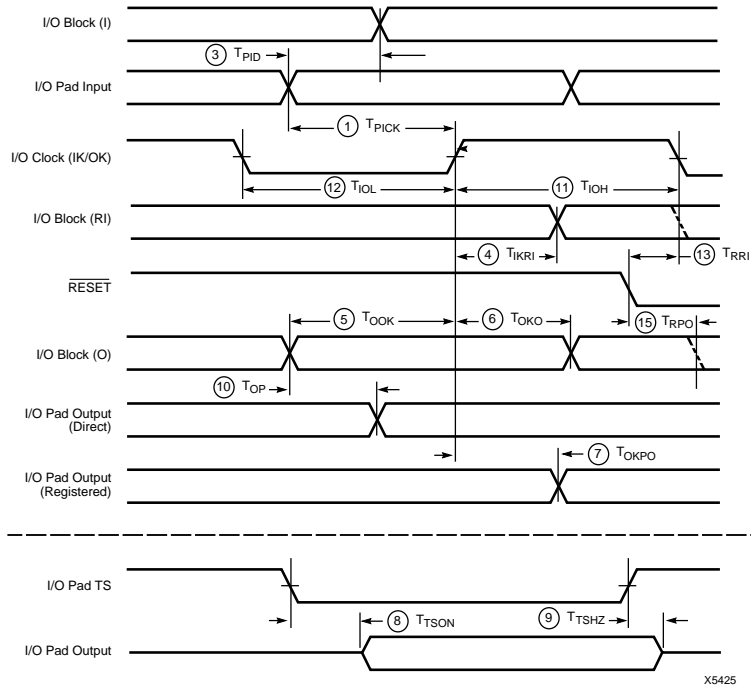
XC3000L IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

| Description | Speed Grade | | -8 | | Units |
|---|-------------|-------------|------|------|-------|
| | Symbol | | Min | Max | |
| Propagation Delays (Input) | | | | | |
| Pad to Direct In (I) | 3 | T_{PID} | | 5.0 | ns |
| Pad to Registered In (Q) with latch transparent | | T_{PTG} | | 24.0 | ns |
| Clock (IK) to Registered In (Q) | 4 | T_{IKRI} | | 6.0 | ns |
| Set-up Time (Input) | | | | | |
| Pad to Clock (IK) set-up time | 1 | T_{PICK} | 22.0 | | ns |
| Propagation Delays (Output) | | | | | |
| Clock (OK) to Pad (fast) | 7 | T_{OKPO} | | 12.0 | ns |
| same (slew rate limited) | 7 | T_{OKPO} | | 28.0 | ns |
| Output (O) to Pad (fast) | 10 | T_{OPF} | | 9.0 | ns |
| same (slew-rate limited) | 10 | T_{OPS} | | 25.0 | ns |
| 3-state to Pad begin hi-Z (fast) | 9 | T_{TSHZ} | | 12.0 | ns |
| same (slew-rate limited) | 9 | T_{TSHZ} | | 28.0 | ns |
| 3-state to Pad active and valid (fast) | 8 | T_{TSOIN} | | 16.0 | ns |
| same (slew -rate limited) | 8 | T_{TSOIN} | | 32.0 | ns |
| Set-up and Hold Times (Output) | | | | | |
| Output (O) to clock (OK) set-up time | 5 | T_{OOK} | 12.0 | | ns |
| Output (O) to clock (OK) hold time | 6 | T_{OKO} | 0 | | ns |
| Clock | | | | | |
| Clock High time | 11 | T_{IOH} | 5.0 | | ns |
| Clock Low time | 12 | T_{IOL} | 5.0 | | ns |
| Max. flip-flop toggle rate | | F_{CLK} | 80.0 | | MHz |
| Global Reset Delays (based on XC3042A) | | | | | |
| RESET Pad to Registered In (Q) | 13 | T_{RRI} | | 25.0 | ns |
| RESET Pad to output pad (fast) | 15 | T_{RPO} | | 35.0 | ns |
| (slew-rate limited) | 15 | T_{RPO} | | 51.0 | ns |

- Notes:**
- Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
 - Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
 - Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
 - T_{PID} , T_{PTG} , and T_{PICK} are 3 ns higher for XTL2 when the pin is configured as a user input.

XC3000L IOB Switching Characteristics Guidelines (continued)



Product Availability

| PINS | 44 | 64 | 68 | 84 | | 100 | | | |
|---------|----------------|----------------|----------------|----------------|--------------|----------------|----------------|----------------|------------------------|
| TYPE | PLAST. PLCC | PLAST. VQFP | PLAST. PLCC | PLAST. PLCC | CERAM PGA | PLAST. PQFP | PLAST. TQFP | PLAST. VQFP | TOP- BRAZED CQFP |
| CODE | PC44 | VQ64 | PC68 | PC84 | PG84 | PQ100 | TQ100 | VQ100 | CB100 |
| XC3020L | | | | C | | | | | |
| XC3030L | | C | | C | | | | C | |
| XC3042L | | | | C | | | | C | |
| XC3064L | | | | C | | | | | |
| XC3090L | | | | C | | | | | |

| PINS | 132 | | 144 | 160 | 164 | 175 | | 176 | 208 | 223 |
|---------|---------------|---------------|----------------|----------------|------------------------|---------------|---------------|----------------|----------------|---------------|
| TYPE | PLAST. PGA | CERAM. PGA | PLAST. TQFP | PLAST. PQFP | TOP- BRAZED CQFP | PLAST. PGA | CERAM. PGA | PLAST. TQFP | PLAST. PQFP | CERAM. PGA |
| CODE | PP132 | PG132 | TQ144 | PQ160 | CB164 | PP175 | PG175 | TQ176 | PQ208 | PG223 |
| XC3020L | | | | | | | | | | |
| XC3030L | | | | | | | | | | |
| XC3042L | | | C | | | | | | | |
| XC3064L | | | C | | | | | | | |
| XC3090L | | | C | | | | | C | | |

Note: C = Commercial, $T_J = 0^\circ$ to $+85^\circ\text{C}$

Ordering Information

Example:

XC3042L-8VQ100C

