

## Features

- Enhanced, high performance FPGA family with five device types
  - Improved redesign of the basic XC3000 FPGA family
  - Logic densities from 1,000 to 6,000 gates
  - Up to 144 user-definable I/Os
- Superset of the industry-leading XC3000 family
  - Identical to the basic XC3000 in structure, pin out, design methodology, and software tools
  - 100% compatible with all XC3000, XC3000L, and XC3100A bitstreams
  - Improved routing and additional features
- Additional programmable interconnection points (PIPs)
  - Improved access to longlines and CLB clock enable inputs
  - Most efficient XC3000-class solution to bus-oriented designs
- Advanced 0.8  $\mu$  and 0.6  $\mu$  CMOS static memory technology
  - Low quiescent and active power consumption
- Performance specified by logic delays, faster than corresponding XC3000 versions
- XC3000A-specific features
  - 4 mA output sink and source current
  - Error checking of the configuration bitstream
  - Soft startup starts all outputs in slew-limited mode upon power-up
  - Easy migration to the XC3400 series of HardWire mask programmed devices for high-volume production.

## Description

The XC3000A family offers the following enhancements over the popular XC3000 family:

The XC3000A family has additional interconnect resources to drive the I-inputs of TBUFs driving horizontal Longlines. The CLB Clock Enable input can be driven from a second vertical Longline. These two additions result in more efficient and faster designs when horizontal Longlines are used for data bussing.

During configuration, the XC3000A devices check the bitstream format for stop bits in the appropriate positions. Any error terminates the configuration and pulls INIT Low.

When the configuration process is finished and the device starts up in user mode, the first activation of the outputs is automatically slew-rate limited. This feature, called Soft Startup, avoids the potential ground bounce when all outputs are turned on simultaneously. After start-up, the slew rate of the individual outputs is, as in the XC3000 family, determined by the individual configuration option.

The XC3000A family is a superset of the XC3000 family. Any bitstream used to configure an XC3000, XC3100 or XC3100A device configures an XC3000A device exactly the same way.

| Device  | Max Logic Gates | Typical Gate Range | CLBs | Array   | User I/Os Max | Flip-Flops | Horizontal Longlines | Configuration Data Bits |
|---------|-----------------|--------------------|------|---------|---------------|------------|----------------------|-------------------------|
| XC3020A | 1,500           | 1,000 - 1,500      | 64   | 8 x 8   | 64            | 256        | 16                   | 14,779                  |
| XC3030A | 2,000           | 1,500 - 2,000      | 100  | 10 x 10 | 80            | 360        | 20                   | 22,176                  |
| XC3042A | 3,000           | 2,000 - 3,000      | 144  | 12 x 12 | 96            | 480        | 24                   | 30,784                  |
| XC3064A | 5,000           | 4,000 - 5,000      | 224  | 16 x 14 | 120           | 688        | 32                   | 46,064                  |
| XC3090A | 6,000           | 5,000 - 6,000      | 320  | 16 x 20 | 144           | 928        | 40                   | 64,160                  |

## XC3000A Switching Characteristics

Xilinx maintains test specifications for each product as controlled documents. To insure the use of the most recently released device performance parameters, please request a copy of the current test-specification revision.

### XC3000A Operating Conditions

| Symbol    | Description  | Min  | Max      | Units    |
|-----------|--|------|----------|----------|
| $V_{CC}$  | Supply voltage relative to GND Commercial 0°C to +85°C junction    | 4.75 | 5.25     | V        |
|           | Supply voltage relative to GND Industrial -40°C to +100°C junction | 4.5  | 5.5      | V        |
| $V_{IHT}$ | High-level input voltage — TTL configuration                       | 2.0  | $V_{CC}$ | V        |
| $V_{ILT}$ | Low-level input voltage — TTL configuration                        | 0    | 0.8      | V        |
| $V_{IHC}$ | High-level input voltage — CMOS configuration                      | 70%  | 100%     | $V_{CC}$ |
| $V_{ILC}$ | Low-level input voltage — CMOS configuration                       | 0    | 20%      | $V_{CC}$ |
| $T_{IN}$  | Input signal transition time                                       |      | 250      | ns       |

**Note:** At junction temperatures above those listed as Operating Conditions, all delay parameters increase by 0.3% per °C.

### XC3000A DC Characteristics Over Operating Conditions

| Symbol     | Description  | Min   | Max  | Units |
|------------|--|-------|------|-------|
| $V_{OH}$   | High-level output voltage (@ $I_{OH} = -4.0$ mA, $V_{CC}$ min)   | 3.86  |      | V     |
| $V_{OL}$   | Low-level output voltage (@ $I_{OL} = 4.0$ mA, $V_{CC}$ min)     |       | 0.40 | V     |
| $V_{OH}$   | High-level output voltage (@ $I_{OH} = -4.0$ mA, $V_{CC}$ min)   | 3.76  |      | V     |
| $V_{OL}$   | Low-level output voltage (@ $I_{OL} = 4.0$ mA, $V_{CC}$ min)     |       | 0.40 | V     |
| $V_{CCPD}$ | Power-down supply voltage (PWRDWN must be Low)                   | 2.30  |      | V     |
| $I_{CCPD}$ | Power-down supply current<br>( $V_{CC(MAX)}$ @ $T_{MAX}$ )       |       |      |       |
|            |  | 3020A | 100  | μA    |
|            |  | 3030A | 160  | μA    |
|            |  | 3042A | 240  | μA    |
|            |  | 3064A | 340  | μA    |
|            |  | 3090A | 500  | μA    |
| $I_{CCO}$  | Quiescent FPGA supply current in addition to $I_{CCPD}$          |       | 500  | μA    |
|            | Chip thresholds programmed as CMOS levels                        |       | 10   | μA    |
| $I_{IL}$   | Input Leakage Current  | -10   | +10  | μA    |
|            | Chip thresholds programmed as TTL levels                         |       |      |       |
| $C_{IN}$   | Input capacitance, all packages except PGA175<br>(sample tested) |       |      |       |
|            | All Pins except XTL1 and XTL2                                    |       | 10   | pF    |
|            | XTL1 and XTL2  |       | 15   | pF    |
|            | Input capacitance, PGA 175<br>(sample tested)                    |       |      |       |
| $I_{RIN}$  | All Pins except XTL1 and XTL2                                    |       | 16   | pF    |
|            | XTL1 and XTL2  |       | 20   | pF    |
| $I_{RIN}$  | Pad pull-up (when selected) @ $V_{IN} = 0$ V (sample tested)     | 0.02  | 0.17 | mA    |
| $I_{RLL}$  | Horizontal Longline pull-up (when selected) @ logic Low          |       | 3.4  | mA    |

**Notes:**

1. With no output current loads, no active input or Longline pull-up resistors, all package pins at  $V_{CC}$  or GND, and the FPGA device configured with a MakeBits tie option.
2. Total continuous output sink current may not exceed 100 mA per ground pin. Total continuous output source may not exceed 100 mA per  $V_{CC}$  pin. The number of ground pins varies from the XC3020A to the XC3090A.

## XC3000A Absolute Maximum Ratings

| Symbol    | Description                                     |                        | Units |
|-----------|---|------------------------|-------|
| $V_{CC}$  | Supply voltage relative to GND                  | -0.5 to +7.0           | V     |
| $V_{IN}$  | Input voltage with respect to GND               | -0.5 to $V_{CC} + 0.5$ | V     |
| $V_{TS}$  | Voltage applied to 3-state output               | -0.5 to $V_{CC} + 0.5$ | V     |
| $T_{STG}$ | Storage temperature (ambient)                   | -65 to +150            | °C    |
| $T_{SOL}$ | Maximum soldering temperature (10 s @ 1/16 in.) | +260                   | °C    |
| $T_J$     | Junction temperature plastic                    | +125                   | °C    |
|           | Junction temperature ceramic                    | +150                   | °C    |

**Note:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions is not implied. Exposure to Absolute Maximum Ratings conditions for extended periods of time may affect device reliability.

## XC3000A Global Buffer Switching Characteristics Guidelines

| Description  | Speed Grade | -7   | -6   | Units |
|--|-------------|------|------|-------|
|  | Symbol      | Max  | Max  |       |
| Global and Alternate Clock Distribution <sup>1</sup><br>Either: <b>Normal</b> IOB input pad through clock buffer<br>to any CLB or IOB clock input<br>Or: <b>Fast</b> (CMOS only) input pad through clock<br>buffer to any CLB or IOB clock input | $T_{PID}$   | 7.5  | 7.0  | ns    |
|  | $T_{PIDC}$  | 6.0  | 5.7  | ns    |
| <b>TBUF</b> driving a Horizontal Longline (L.L.) <sup>1</sup><br>I to L.L. while T is Low (buffer active)  | $T_{IO}$    | 4.5  | 4.0  | ns    |
| $T\downarrow$ to L.L. active and valid with single pull-up resistor  | $T_{ON}$    | 9.0  | 8.0  | ns    |
| $T\downarrow$ to L.L. active and valid with pair of pull-up resistors  | $T_{ON}$    | 11.0 | 10.0 | ns    |
| $T\uparrow$ to L.L. High with single pull-up resistor  | $T_{PUS}$   | 16.0 | 14.0 | ns    |
| $T\uparrow$ to L.L. High with pair of pull-up resistors  | $T_{PUF}$   | 10.0 | 8.0  | ns    |
| <b>BIDI</b><br>Bidirectional buffer delay  | $T_{BIDI}$  | 1.7  | 1.5  | ns    |

**Note:** 1. Timing is based on the XC3042A, for other devices see XACT timing calculator.

## XC3000A CLB Switching Characteristics Guidelines

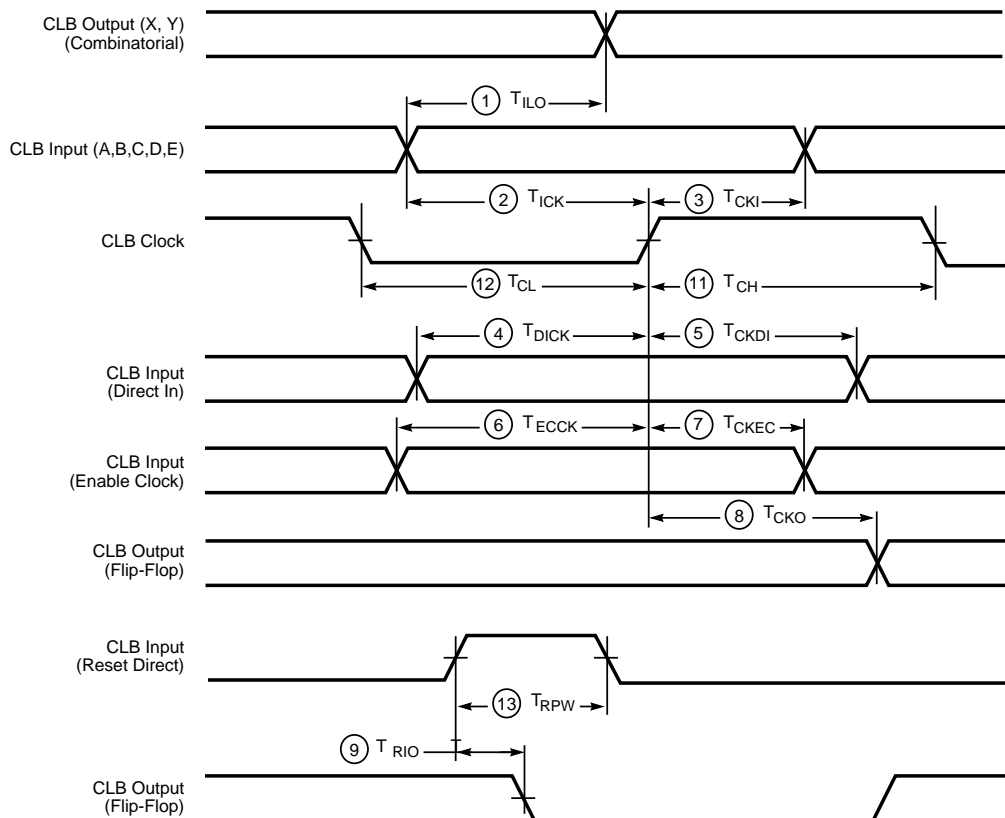
Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

|  |  | Speed Grade |            | -7    |      | -6    |      |       |
|--|--|-------------|------------|-------|------|-------|------|-------|
| Description  |  | Symbol      |            | Min   | Max  | Min   | Max  | Units |
| Combinatorial Delay<br>Logic Variables A, B, C, D, E, to outputs X or Y<br>FG Mode<br>F and FGM Mode   |  | 1           | $T_{ILO}$  |       | 5.1  |       | 4.1  | ns    |
|  |  |             |            |       | 5.6  |       | 4.6  | ns    |
|  |  |             |            |       |      |       |      |       |
| Sequential delay<br>Clock k to outputs X or Y<br>Clock k to outputs X or Y when Q is returned<br>through function generators F or G to drive X or Y<br>FG Mode<br>F and FGM Mode |  | 8           | $T_{CKO}$  |       | 4.5  |       | 4.0  | ns    |
|  |  |             |            |       | 9.5  |       | 8.0  | ns    |
|  |  |             |            |       | 10.0 |       | 8.5  | ns    |
| Set-up time before clock K<br>Logic Variables A, B, C, D, E<br>FG Mode<br>F and FGM Mode<br>Data In DI<br>Enable Clock EC  |  | 2           | $T_{ICK}$  | 4.5   |      | 3.5   |      | ns    |
|  |  |             |            | 5.0   |      | 4.0   |      | ns    |
|  |  | 4           | $T_{DICK}$ | 4.0   |      | 3.0   |      | ns    |
|  |  | 6           | $T_{ECCK}$ | 4.5   |      | 4.0   |      | ns    |
| Hold Time after clock K<br>Logic Variables A, B, C, D, E<br>Data In $DI^2$<br>Enable Clock EC  |  | 3           | $T_{CKI}$  | 0     |      | 0     |      | ns    |
|  |  | 5           | $T_{CKDI}$ | 1.0   |      | 1.0   |      | ns    |
|  |  | 7           | $T_{CKEC}$ | 2.0   |      | 2.0   |      | ns    |
| Clock<br>Clock High time<br>Clock Low time<br>Max. flip-flop toggle rate   |  | 11          | $T_{CH}$   | 4.0   |      | 3.5   |      | ns    |
|  |  | 12          | $T_{CL}$   | 4.0   |      | 3.5   |      | ns    |
|  |  |             | $F_{CLK}$  | 113.0 |      | 135.0 |      | MHz   |
| Reset Direct (RD)<br>RD width<br>delay from RD to outputs X or Y   |  | 13          | $T_{RPW}$  | 6.0   |      | 5.0   |      | ns    |
|  |  | 9           | $T_{RIO}$  |       | 6.0  |       | 5.0  | ns    |
| Global Reset ( $\overline{RESET}$ Pad) <sup>1</sup><br>$\overline{RESET}$ width (Low)<br>delay from $\overline{RESET}$ pad to outputs X or Y                                     |  |             | $T_{MRW}$  | 16.0  |      | 14.0  |      | ns    |
|  |  |             | $T_{MRQ}$  |       | 19.0 |       | 17.0 | ns    |

**Notes:** 1. Timing is based on the XC3042A, for other devices see XACT timing calculator.

2. The CLB K to Q output delay ( $T_{CKO}$ , #8) of any CLB, plus the shortest possible interconnect delay, is always longer than the Data In hold time requirement ( $T_{CKDI}$ , #5) of any CLB on the same die.

## XC3000A CLB Switching Characteristics Guidelines (continued)



X5424

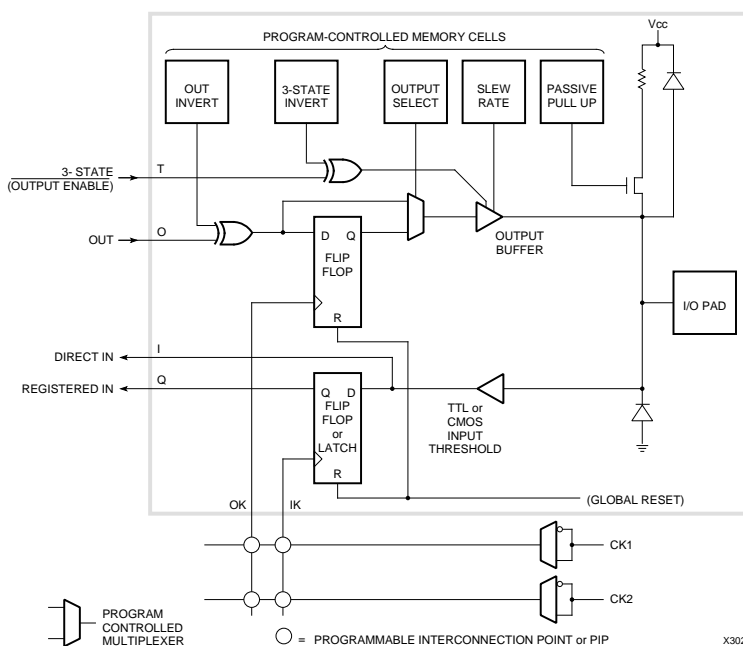
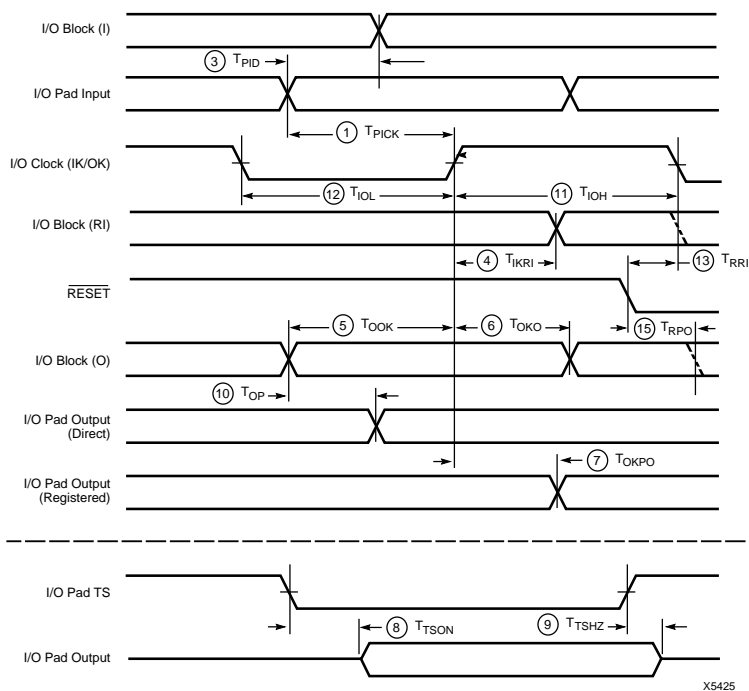
## XC3000A IOB Switching Characteristics Guidelines

Testing of the switching parameters is modeled after testing methods specified by MIL-M-38510/605. All devices are 100% functionally tested. Since many internal timing parameters cannot be measured directly, they are derived from benchmark timing patterns. The following guidelines reflect worst-case values over the recommended operating conditions. For more detailed, more precise, and more up-to-date timing information, use the values provided by the XACT timing calculator and used in the simulator.

| Description                                     | Speed Grade |             | -7    |      | -6    |      | Units |
|---|-------------|-------------|-------|------|-------|------|-------|
|   | Symbol      |             | Min   | Max  | Min   | Max  |       |
| Propagation Delays (Input)                      |             |             |       |      |       |      |       |
| Pad to Direct In (I)                            | 3           | $T_{PID}$   |       | 4.0  |       | 3.0  | ns    |
| Pad to Registered In (Q) with latch transparent |             | $T_{PTG}$   |       | 15.0 |       | 14.0 | ns    |
| Clock (IK) to Registered In (Q)                 | 4           | $T_{IKRI}$  |       | 3.0  |       | 2.5  | ns    |
| Set-up Time (Input)                             |             |             |       |      |       |      |       |
| Pad to Clock (IK) set-up time                   | 1           | $T_{PICK}$  | 14.0  |      | 12.0  |      | ns    |
| Propagation Delays (Output)                     |             |             |       |      |       |      |       |
| Clock (OK) to Pad (fast)                        | 7           | $T_{OKPO}$  |       | 8.0  |       | 7.0  | ns    |
| same (slew rate limited)                        | 7           | $T_{OKPO}$  |       | 18.0 |       | 15.0 | ns    |
| Output (O) to Pad (fast)                        | 10          | $T_{OPF}$   |       | 6.0  |       | 5.0  | ns    |
| same (slew-rate limited)                        | 10          | $T_{OPS}$   |       | 16.0 |       | 13.0 | ns    |
| 3-state to Pad begin hi-Z (fast)                | 9           | $T_{TSHZ}$  |       | 10.0 |       | 9.0  | ns    |
| same (slew-rate limited)                        | 9           | $T_{TSHZ}$  |       | 20.0 |       | 12.0 | ns    |
| 3-state to Pad active and valid (fast)          | 8           | $T_{TSOIN}$ |       | 11.0 |       | 10.0 | ns    |
| same (slew -rate limited)                       | 8           | $T_{TSOIN}$ |       | 21.0 |       | 18.0 | ns    |
| Set-up and Hold Times (Output)                  |             |             |       |      |       |      |       |
| Output (O) to clock (OK) set-up time            | 5           | $T_{OOK}$   | 8.0   |      | 7.0   |      | ns    |
| Output (O) to clock (OK) hold time              | 6           | $T_{OKO}$   | 0     |      | 0     |      | ns    |
| Clock   |             |             |       |      |       |      |       |
| Clock High time                                 | 11          | $T_{IOH}$   | 4.0   |      | 3.5   |      | ns    |
| Clock Low time                                  | 12          | $T_{IOL}$   | 4.0   |      | 3.5   |      | ns    |
| Max. flip-flop toggle rate                      |             | $F_{CLK}$   | 113.0 |      | 135.0 |      | MHz   |
| Global Reset Delays (based on XC3042A)          |             |             |       |      |       |      |       |
| RESET Pad to Registered In (Q)                  | 13          | $T_{RRI}$   |       | 24.0 |       | 23.0 | ns    |
| RESET Pad to output pad (fast)                  | 15          | $T_{RPO}$   |       | 33.0 |       | 29.0 | ns    |
| (slew-rate limited)                             | 15          | $T_{RPO}$   |       | 43.0 |       | 37.0 | ns    |

- Notes:
1. Timing is measured at pin threshold, with 50 pF external capacitive loads (incl. test fixture). Typical slew rate limited output rise/fall times are approximately four times longer.
  2. Voltage levels of unused (bonded and unbonded) pads must be valid logic levels. Each can be configured with the internal pull-up resistor or alternatively configured as a driven output or driven from an external source.
  3. Input pad set-up time is specified with respect to the internal clock (ik). In order to calculate system set-up time, subtract clock delay (pad to ik) from the input pad set-up time value. Input pad holdtime with respect to the internal clock (ik) is negative. This means that pad level changes immediately before the internal clock edge (ik) will not be recognized.
  4.  $T_{PID}$ ,  $T_{PTG}$ , and  $T_{PICK}$  are 3 ns higher for XTL2 when the pin is configured as a user input.

## XC3000A IOB Switching Characteristics Guidelines (continued)



## Product Availability

| PINS    |    | 44             | 64             | 68             | 84             |              | 100            |                |                |                        |
|---------|----|----------------|----------------|----------------|----------------|--------------|----------------|----------------|----------------|------------------------|
| TYPE    |    | PLAST.<br>PLCC | PLAST.<br>VQFP | PLAST.<br>PLCC | PLAST.<br>PLCC | CERAM<br>PGA | PLAST.<br>PQFP | PLAST.<br>TQFP | PLAST.<br>VQFP | TOP-<br>BRAZED<br>CQFP |
| CODE    |    | PC44           | VQ64           | PC68           | PC84           | PG84         | PQ100          | TQ100          | VQ100          | CB100                  |
| XC3020A | -7 |                |                | C I            | C I            | C I          | C I            |                |                |                        |
|         | -6 |                |                | C              | C              | C            | C              |                |                |                        |
| XC3030A | -7 | C I            | C I            | C I            | C I            | C I          | C I            |                | C I            |                        |
|         | -6 | C              | C              | C              | C              | C            | C              |                | C              |                        |
| XC3042A | -7 |                |                |                | C I            | C I          | C I            |                | C I            |                        |
|         | -6 |                |                |                | C              | C            | C              |                | C              |                        |
| XC3064A | -7 |                |                |                | C I            |              |                |                |                |                        |
|         | -6 |                |                |                | C              |              |                |                |                |                        |
| XC3090A | -7 |                |                |                | C I            |              |                |                |                |                        |
|         | -6 |                |                |                | C              |              |                |                |                |                        |

| PINS    |    | 132           |               | 144            | 160            | 164                    | 175           |               | 176            | 208            | 223           |
|---------|----|---------------|---------------|----------------|----------------|------------------------|---------------|---------------|----------------|----------------|---------------|
| TYPE    |    | PLAST.<br>PGA | CERAM.<br>PGA | PLAST.<br>TQFP | PLAST.<br>PQFP | TOP-<br>BRAZED<br>CQFP | PLAST.<br>PGA | CERAM.<br>PGA | PLAST.<br>TQFP | PLAST.<br>PQFP | CERAM.<br>PGA |
| CODE    |    | PP132         | PG132         | TQ144          | PQ160          | CB164                  | PP175         | PG175         | TQ176          | PQ208          | PG223         |
| XC3020A | -7 |               |               |                |                |                        |               |               |                |                |               |
|         | -6 |               |               |                |                |                        |               |               |                |                |               |
| XC3030A | -7 |               |               |                |                |                        |               |               |                |                |               |
|         | -6 |               |               |                |                |                        |               |               |                |                |               |
| XC3042A | -7 | C I           | C I           | C I            |                |                        |               |               |                |                |               |
|         | -6 | C             | C             | C              |                |                        |               |               |                |                |               |
| XC3064A | -7 | C I           | C I           | C I            | C I            |                        |               |               |                |                |               |
|         | -6 | C             | C             | C              | C              |                        |               |               |                |                |               |
| XC3090A | -7 |               |               | C I            | C I            |                        | C I           | C I           | C I            | C I            |               |
|         | -6 |               |               | C              | C              |                        | C             | C             | C              | C              |               |

**Note:** C = Commercial,  $T_J = 0^\circ$  to  $+85^\circ\text{C}$  I = Industrial,  $T_J = -40^\circ$  to  $+100^\circ\text{C}$

## Ordering Information

Example:

