

Introduction

The ball grid array (BGA) package is the latest in a series of innovative programmable logic packaging options to be offered by Xilinx. As the newest alternative for high density surface mount packaging, the BGA offers higher density than the plastic quad flat package (PQFP). The BGA also eliminates handling and assembly issues commonly associated with PQFPs. The BGA will rapidly become the preferred package for applications requiring greater than 200 pins in a surface mount configuration.

The BGA uses solder balls on the underside of a small substrate, instead of leads, to connect to a PC board. The inherent mechanical ruggedness of the balls, along with a wide pin-to-pin pitch of 1.5 mm, results in improved manufacturing yields. In addition, PC board space is reduced and electrical and thermal performance is improved compared with the PQFP. A cross sectional diagram of the BGA is shown below which illustrates some of the key features of this package.

Evolution of the BGA

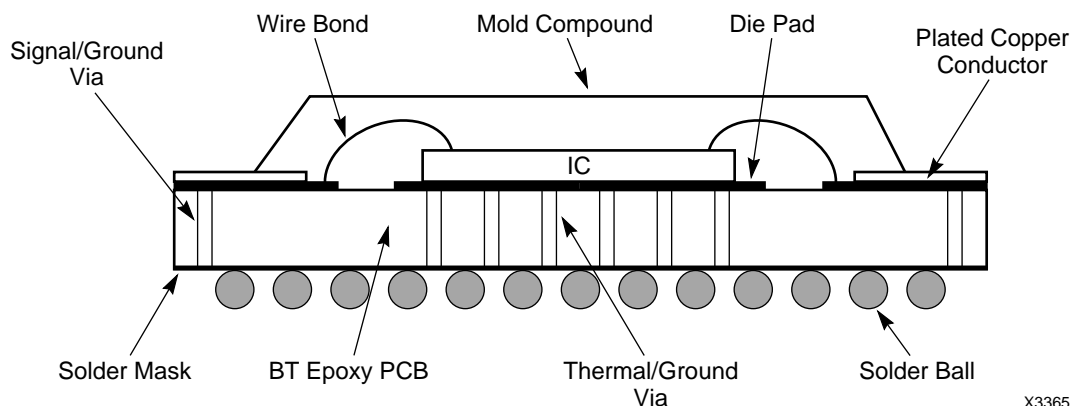
High density surface mount packages are critical to many portable applications, such as cellular telephones and pagers, hand-held computers and personal digital assistants and computer add-ons such as PCMCIA cards. These applications all require high density surface mount packaging, and in many cases also require "thin" packaging. Thin QFPs (TQFPs) and very thin QFPs (VQFPs) with thicknesses of 1.5 mm and 1.0 mm, respectively, have been developed and introduced by Xilinx in response to this market need. The BGA package also offers a thinner

profile than conventional PQFPs (1.9 mm versus 3.7 mm) which makes the package ideal for high pin count portable applications.

High pin count, surface mount packages are clearly the direction in which ASICs and programmable logic are heading. Since high volume ASICs have traditionally provided the lead in this area, current forecasts of ASIC package type and pin count are relevant to the high density programmable logic market. According to Dataquest (June, 1993) less than 2% of MOS gate array designs targeted the BGA package in 1992, but over 15% will be targeting BGA by 1997. With the added Erasable Programmable Logic Device (EPLD) requirements to program high pin count devices in a programmer prior to assembly, Xilinx expects the new design start rate for EPLDs to be significantly higher.

High Density EPLDs and the BGA

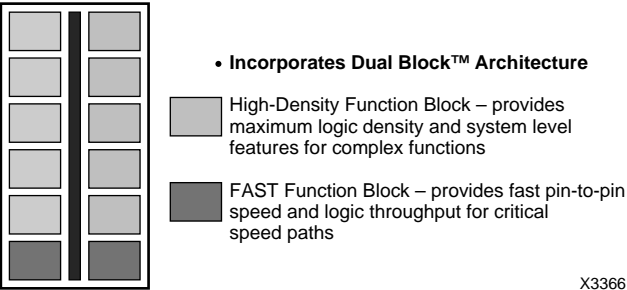
EPLDs are typically used in applications requiring very fast pin-to-pin timing and predictable performance. For example, system performance which is easily determined and which remains fixed independent of routing within the chip. EPLDs typically are programmed in a device programmer, and then inserted into the PC board for prototyping or production. Since individual devices require some handling prior to insertion, there is a risk of lead damage with fine pitch packaging. There have been solutions proposed in the past consisting of special "device carriers" and sockets, but the BGA provides the best solution by completely eliminating problems associated with handling PQFPs.



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Figure 1. Ball Grid Array Package

The Xilinx XC73108™ is the first EPLD to be offered in the BGA package. It consists of 108 macrocells, and is offered in the 225 pin BGA. This device has been in production in PLCC, PQFP, and PGA packages, and will be available in the BGA in Q4 1993. Highlights of the XC73108 architecture and features are shown below:



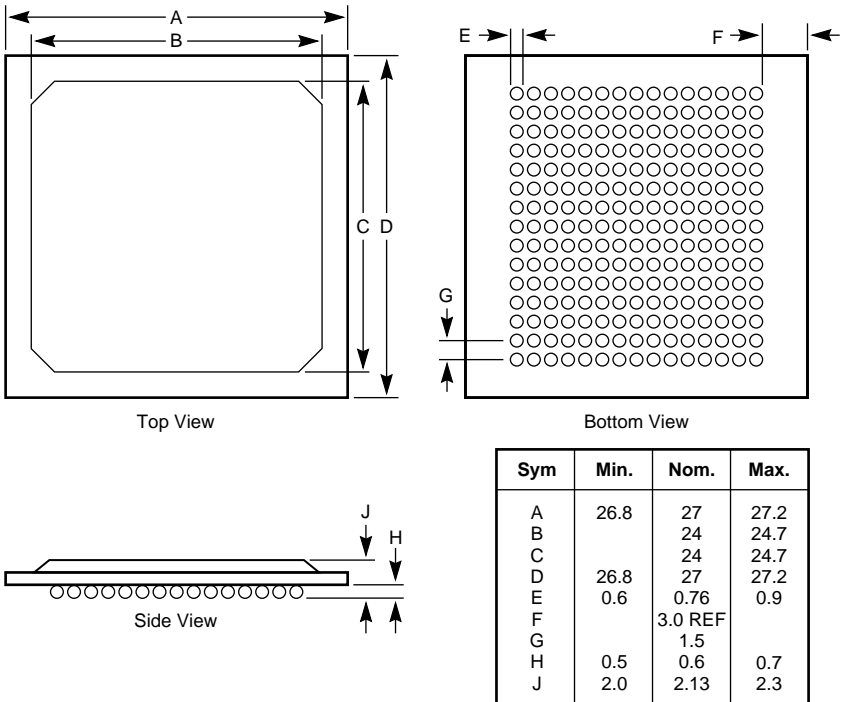
- Equivalent PALs 12
- Macrocells 108
- Registers 198
- t_{PD} 12 ns
- t_{CYC} 80 MHz
- 100% Routable Universal Interconnect Matrix
- High-speed ALU with Fast Carry Network
- 18 Outputs with 24 mA Drive
- 3.3 V or 5 V Operation
- Power Management

BGA Package Advantages

The need to increase the lead count on the perimeter of PQFP packages without increasing the package body size and board space required, has resulted in a very fine lead pitch of 0.5 mm for the 208 lead PQFP. This lead pitch results in very fragile connections which are subject to mechanical damage when handling or testing. Mishandling can result in a loss of lead coplanarity, which can adversely affect manufacturing yields. The primary advantage of the BGA is the solder-bumped package can be IR reflowed in standard production environments with extremely low solder defect levels. The high solder assembly yield of the BGA is due to the use of a tin/lead eutectic solder bump technology which reduces the impact of three major factors for yield loss with conventional PQFPs: opens due to inadequate lead coplanarity, shorting between terminations due to solder bridging, and opens due to package misplacement. Coplanarity problems are eliminated by replacing leads with solder balls which collapse approximately 0.2 mm during assembly. Solder bridging is reduced due to the wide pad pitch compared to PQFPs. Package placement is not as critical due to the wide pitch and to the self alignment capability during reflow due to solder wetting forces aligning package pads to PC board lands.

There are a host of other BGA advantages versus PQFP packaging which are summarized in the following table.

Figure 2. XC73108 EPLD in a 225-Pin BGA



All measurements in millimeters
 Actual dimensions may vary and should be reconfirmed prior to PCB layout.

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Figure 3. Package Outline 225-Pin BGA

Table 1. BGA Package Advantages vs. PQFP

Smaller Package Size	BGA	PQFP
Area	729 mm ² (225 BGA)	952 mm ² (208 PQFP)
Height	1.9 mm	3.7 mm
Improved Performance	169 BGA	160 PQFP
Lead Inductance	5.4 nH	10 nH
Capacitance	1.1 pF	1.6 pF
Theta J/A	23° C/W	35° C/W
Improved Manufacturing	BGA	PQFP
Lead Pitch	1.5 mm	0.5 mm (208 PQFP)
Programmer Insertion	Easy	Potential Lead Damage
Lead Coplanarity	No Issue	Difficult to Maintain
Pick and Place	Trays or Tape & Reel	Trays Only
Placement Tolerance	0.3 mm	0.075 mm
Solder Defects	< 20 ppm	> 500 ppm

BGA Prototyping and Manufacturing Support

The advantages of the BGA for complex PLDs will result in rapid acceptance of this new package technology. The Ball Grid Array has been proposed for JEDEC registration, and supporting test hardware is available. In addition, a BGA socket adapter for the standard Xilinx EPLD Programmer will be available Q1, 1994, to support customer designs using the XC73108. Third party programming support will follow in the first half of 1994.

Table 2. Test Socket Support

Test Sockets:

3M/Textool 225 BGA – part # 2-0225-08172-000-019-002

BGA Adapters:

Emulation Technology ZIF & production sockets

Summary

The Ball Grid Array package represents a significant step forward in high pin count surface mount assembly technology. The package has proven to be usable with existing production surface mount equipment and flows with a minimum of change. Several semiconductor companies, including Xilinx, have announced the intention to support this technology and, with the continuing trend toward high pin count system requirements, growth rates for this package should be even greater than those for PQFPs at a similar point in time. Customers using high density EPLDs potentially gain the most from this package, allowing device programming without the risk of introducing pin coplanarity problems.