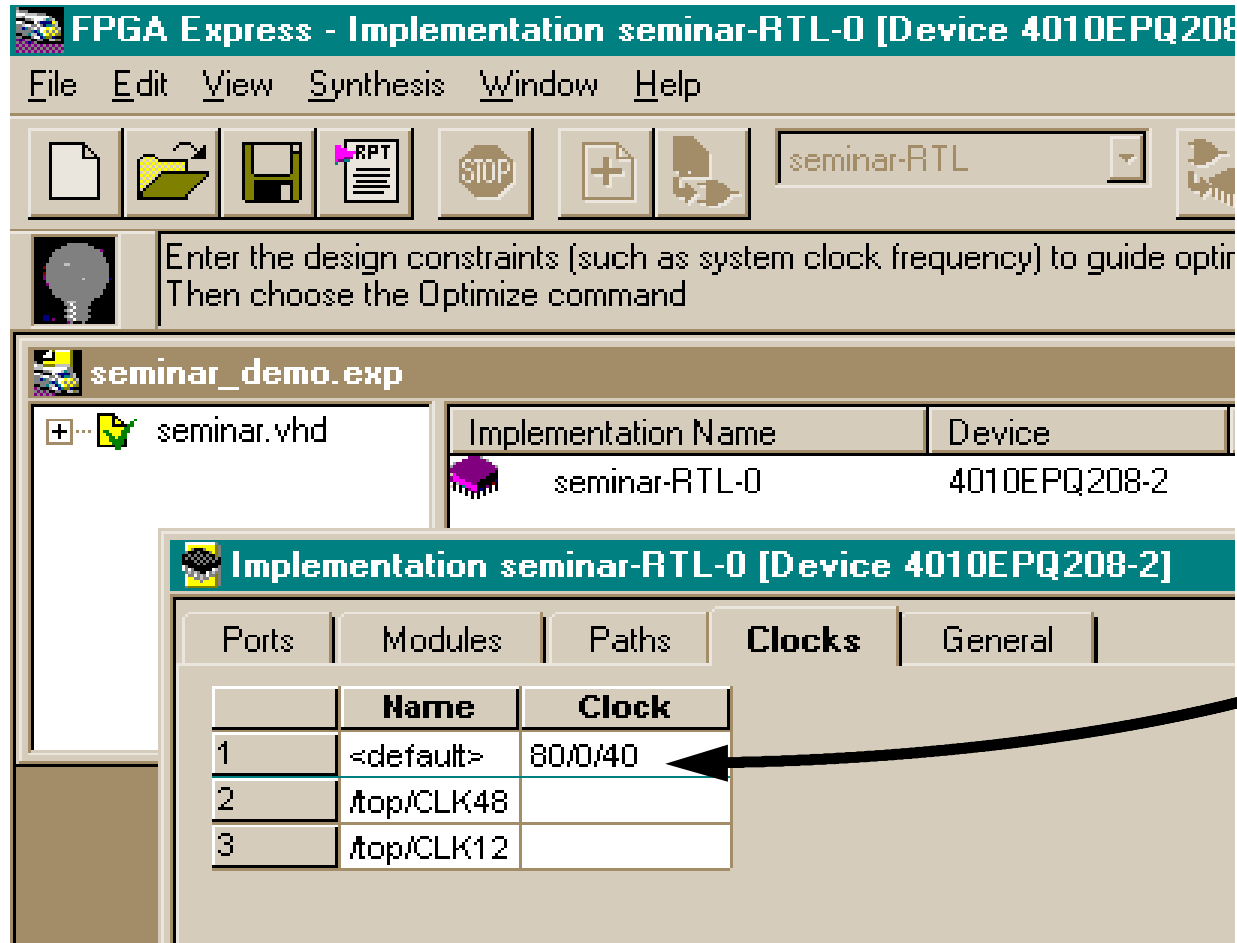


Demonstration Screens

Constraint Entry using Synopsys FPGA Express

FPGA Express Supports Global Constraints



80 ns clock constraint
applies to all flip-flops
in this design

Predefined Group Constraints Derived From Clock

FPGA Express - Implementation seminar-RTL-0 [Device 4010EPQ208-2]

File Edit View Synthesis Window Help

semnar-RTL

Enter the design constraints (such as system clock frequency) to guide optimization.
Then choose the Optimize command

semnar_demo.exp

semnar.vhd

Implementation Name	Device	Modify Date
semnar-RTL-0	4010EPQ208-2	4/11/97 1:15:56 PM

Implementation seminar-RTL-0 [Device 4010EPQ208-2]

Ports	Modules	Paths	Clocks	General
From	To	Delay		
1 All Input Ports	All Output Ports	80		
2 All Input Ports	FF's clocked by rising /top/CLK12	80		
3 FF's clocked by rising /top/CLK48	All Output Ports	80		
4 FF's clocked by rising /top/CLK48	FF's clocked by rising /top/CLK48	80		
5 FF's clocked by rising /top/CLK12	All Output Ports	80		
6 FF's clocked by rising /top/CLK12	FF's clocked by rising /top/CLK12	80		

Default groups are constrained based on default clock period.

FFs grouped by source clock signal

Individual Pin Control of Input & Output Delays

seminar_demo.exp

seminar.vhd

Implementation Name	Device	Modi
seminar-RTL-0	4010EPQ208-2	4/11

Implementation seminar-RTL-0 [Device 4010EPQ208-2]

Ports | Modules | Paths | Clocks | General

View: [] Define Custom...

	Name	Direction	Input Delay (ns)	Output Delay (ns)
1	<default>			
2	CLK12	input	80/(RC, CLK12)	
3	CLK48	input	80/(RC, CLK12)	
4	CLR	input	80/(RC, CLK12)	
5	X_7	input	80/(RC, CLK12)	
6	X_6	input	80/(RC, CLK12)	
7	X_5	input	80/(RC, CLK12)	

Input delay (pad-FF)
and
Output delay (FF-pad)
controllable per pin

Defining Tighter Constraints for 48 MHz Logic

The screenshot shows the Xilinx ISE software interface. The main window displays a project named 'seminar_demo.exp' with a file 'seminar.vhd'. Below this, a table lists the implementation details:

Implementation Name	Device	Modify Date
seminar-RTL-0	4010EPQ208-2	4/11/97 1:15:56 PM

The 'Implementation seminar-RTL-0 [Device 4010EPQ208-2]' window is open, showing a table of clock constraints:

Ports	Modules	Paths	Clocks
1	<default>	80/0/40	
2	/top/CLK48	20/0/10	
3	/top/CLK12		

The 'Define Clock' dialog box is open, showing the 'Times in ns' section with the following values:

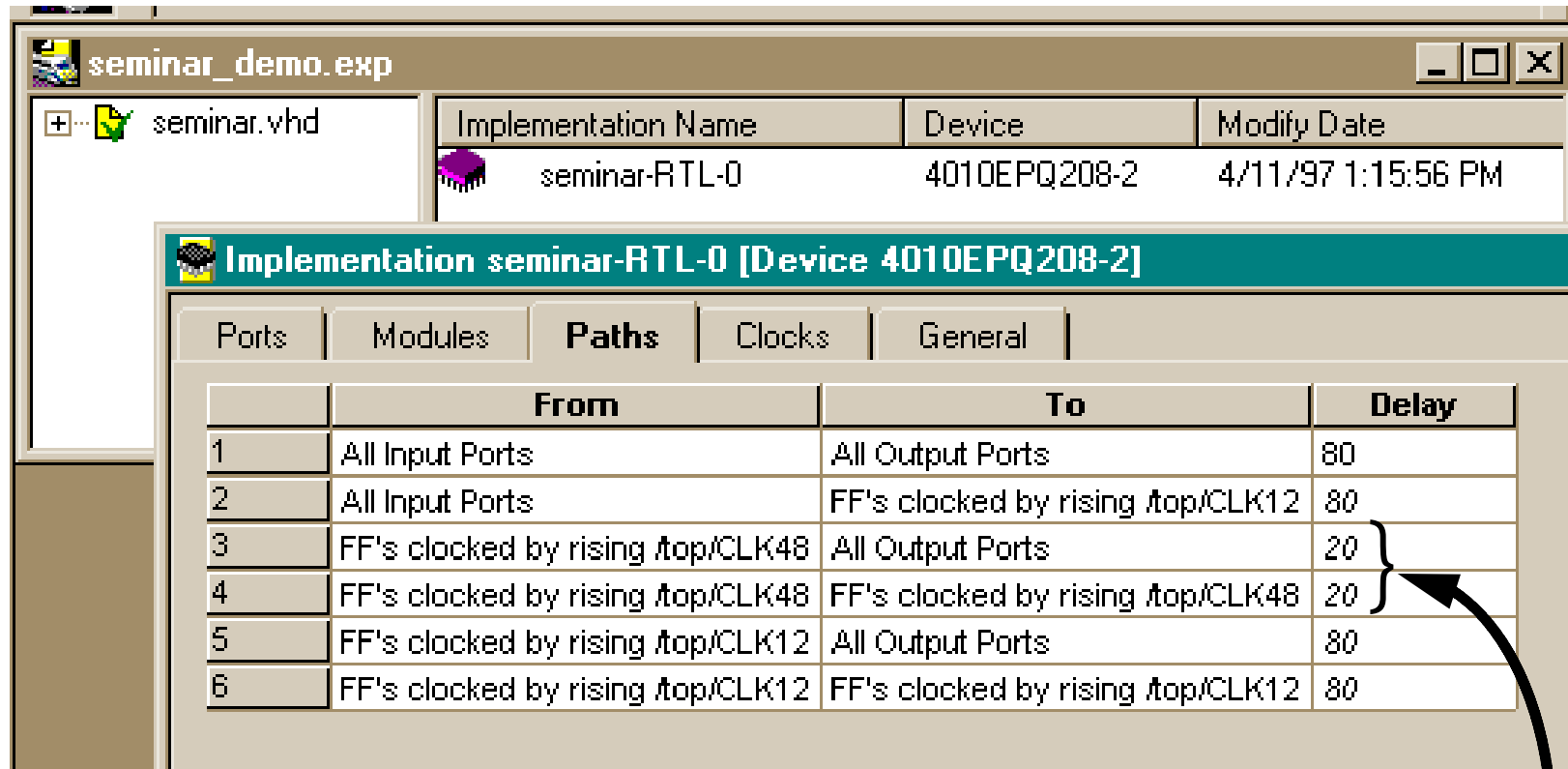
Period	Rise at	Fall at
20	0	10

Below the input fields is a timing diagram showing a square wave. The diagram is labeled with 'Period', 'Rise', and 'Fall' times. The 'Period' is the total width of one cycle, 'Rise' is the time from low to high, and 'Fall' is the time from high to low.

At the bottom of the dialog box are the 'OK', 'Cancel', and 'Help' buttons.

For Help, press F1

Path-Specific Constraints Applied to Desired Elements



The screenshot shows the Xilinx ISE implementation constraints editor for a project named 'seminar_demo.exp'. The implementation name is 'seminar-RTL-0' on a '4010EPQ208-2' device, with a modify date of '4/11/97 1:15:56 PM'. The 'Paths' tab is selected, displaying a table of constraints. The table has columns for 'From', 'To', and 'Delay'. A bracket on the right side of the table groups rows 3 and 4, with an arrow pointing to the text below.

	From	To	Delay
1	All Input Ports	All Output Ports	80
2	All Input Ports	FF's clocked by rising /top/CLK12	80
3	FF's clocked by rising /top/CLK48	All Output Ports	20
4	FF's clocked by rising /top/CLK48	FF's clocked by rising /top/CLK48	20
5	FF's clocked by rising /top/CLK12	All Output Ports	80
6	FF's clocked by rising /top/CLK12	FF's clocked by rising /top/CLK12	80

Tighter 20 ns (50 MHz) constraint now applied to only those FFs clocked by CLK48

Defining Fast Setup for CLK48 Input

seminar-RTL-0 4010EPQ208-2 4/11/97 1:15:56 PM

Implementation seminar-RTL-0 [Device 4010EPQ208-2]

Ports Modules Paths Clocks General

View: Define Custom...

	Name	Direction	Input Delay (ns)
1	<default>		
2	CLK12	input	80/(RC,CLK12)
3	CLK48	input	80/(RC,CLK12)
4	CLR	input	80/(RC,CLK12)
5	X_7	input	80/(RC,CLK12)
6	X_6	input	80/(RC,CLK12)
7	X_5	input	80/(RC,CLK12)

Define Delay

Maximum Delay
15 ns

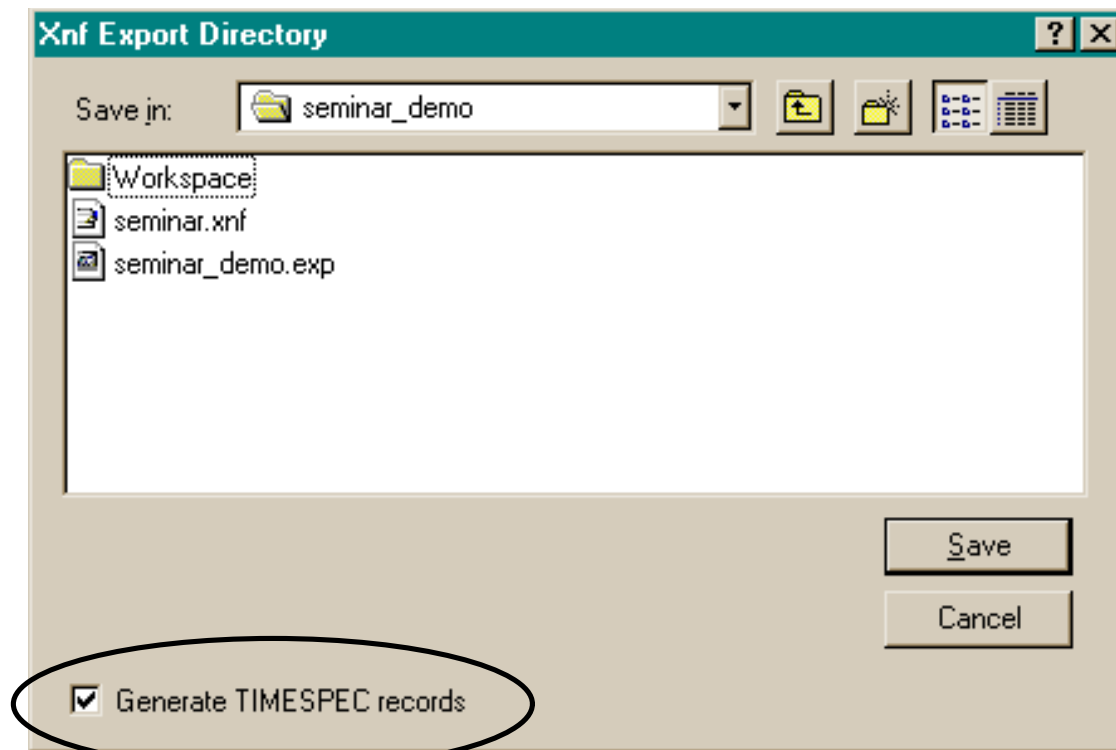
Relative to group:
(RC,CLK48) - FF's clocked by rising /top/CLK48

OK
Cancel
Help

(0) - All Output Ports
(RC,CLK48) - FF's clocked by rising /top/CLK48
(RC,CLK12) - FF's clocked by rising /top/CLK12

15 ns input delay (setup) constraint now applied
to CLK48 input pin

FPGA Express Writes Constraints Into Design Netlist



TIMESPECs (constraints) will be written into
design netlist output