

Case Studies

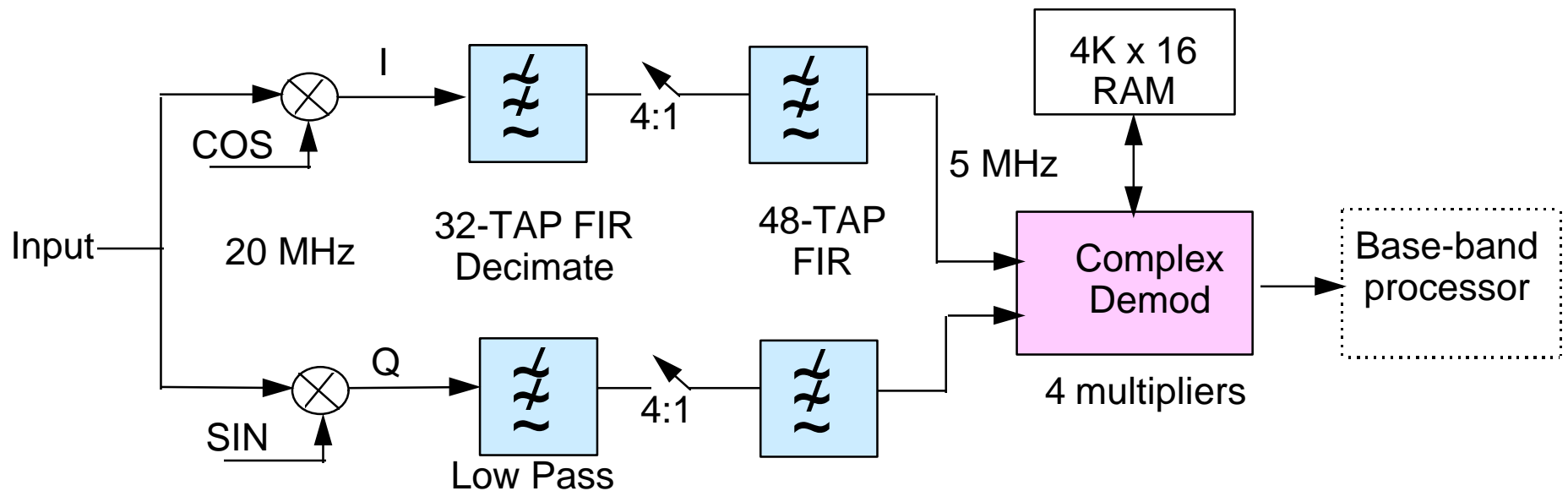
- DRAM Controller: XC9500 ISP CPLD
- Universal Serial Bus: XC4000E/X FPGA
- Peripheral Component Interconnect: XC4000E/X FPGA
- **Digital Signal Processing: XC4000XL FPGA**

Case Study #4 - DSP

- Satellite modem uses distributed arithmetic processing
- Demonstrates how FPGAs can achieve much higher performance than dedicated DSP processors

Satellite Modem Receiver

$$(20 \times 32 / 4) + (48 \times 5) = 400 \text{ Million MACs per second}$$



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DSP System Design Challenges

■ Performance

- Previous design: 1 processor, 1 channel, 5 MHz, 48 taps
- New design: 2 channels (I & Q), 20MHz, 80 taps each
- Would need 12 DSP C16-type processors

■ Cost

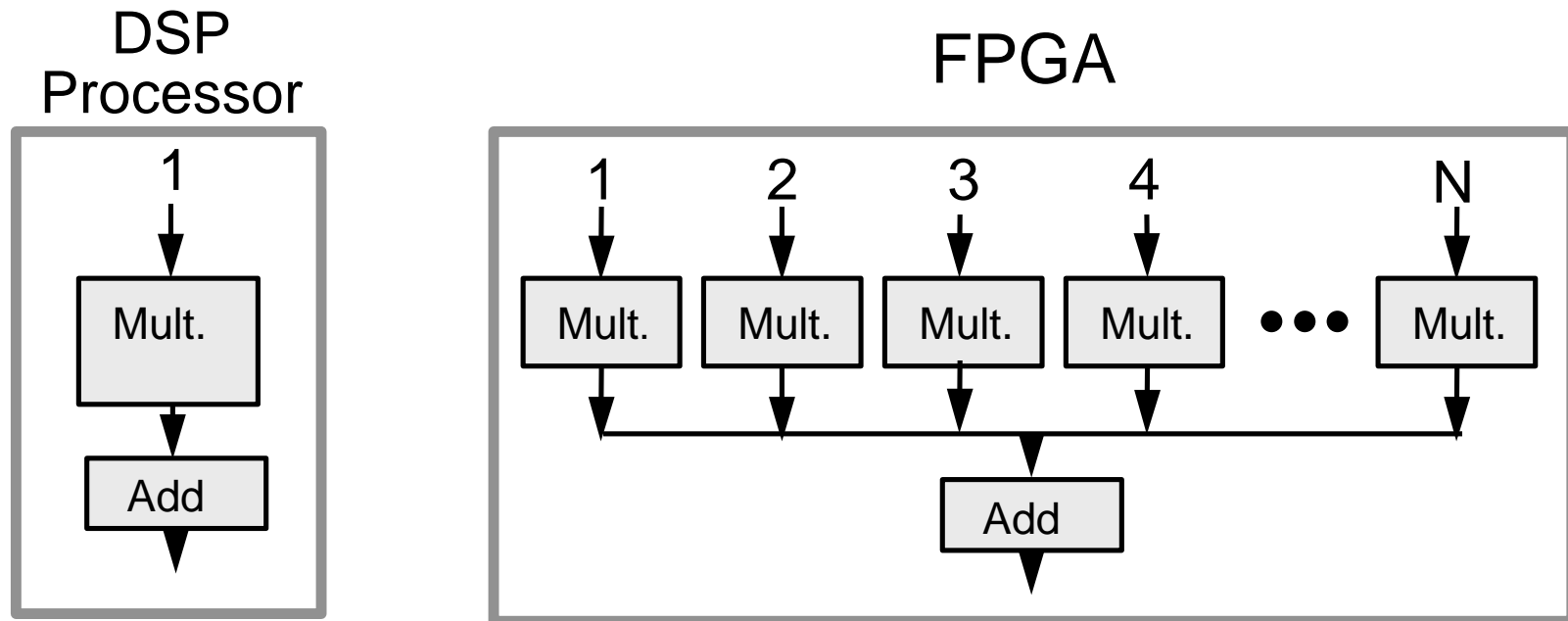
- 12 DSP processors are cost prohibitive
- Space limitation (12 CPUs, memory, I/O won't fit)
- Power dissipation issue with 12 DSP processors

■ Schedule / Risk

- Complicated real time, multi-processor software

Xilinx DSP is the enabling technology

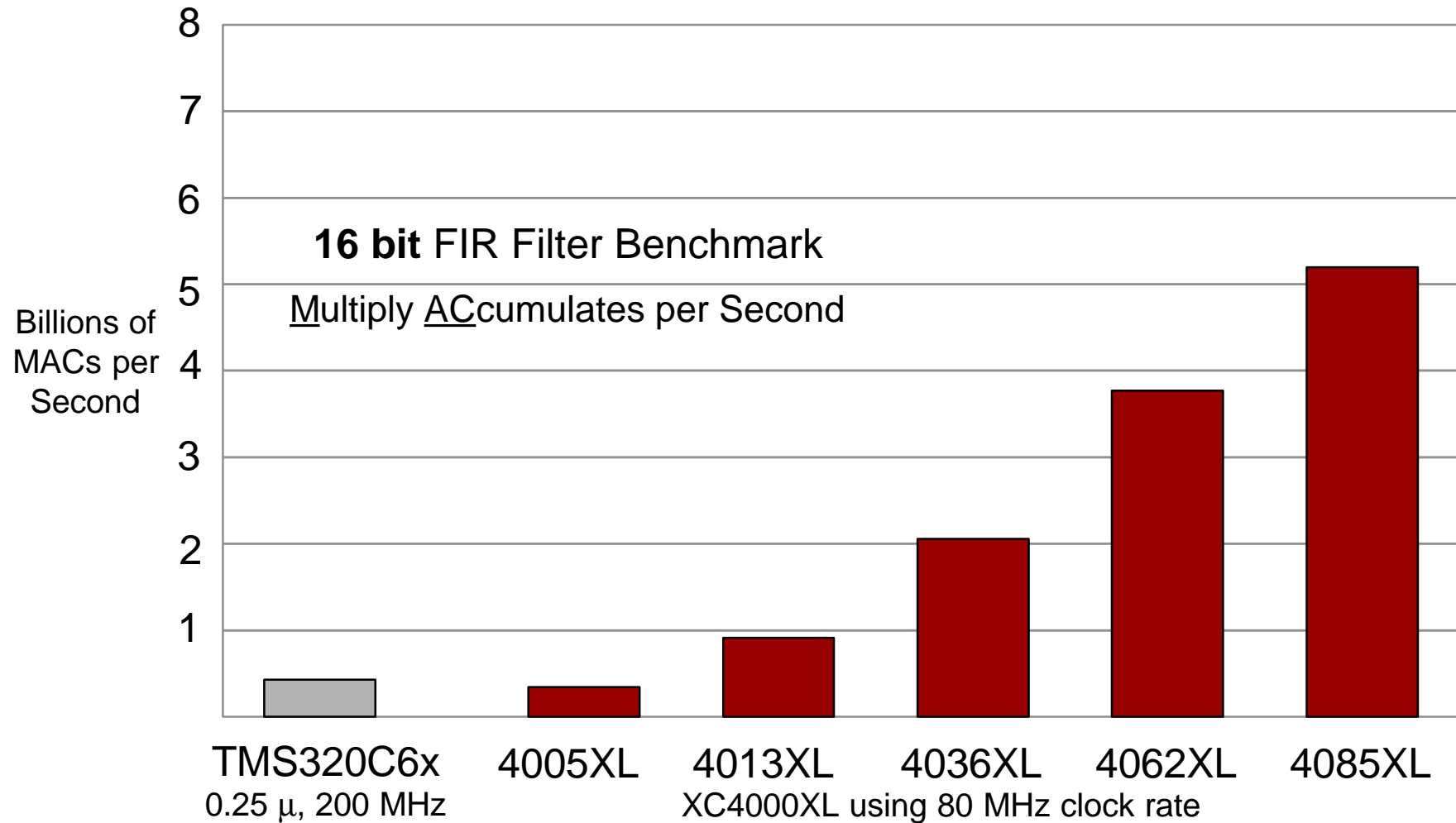
FPGAs Provide Outstanding Performance



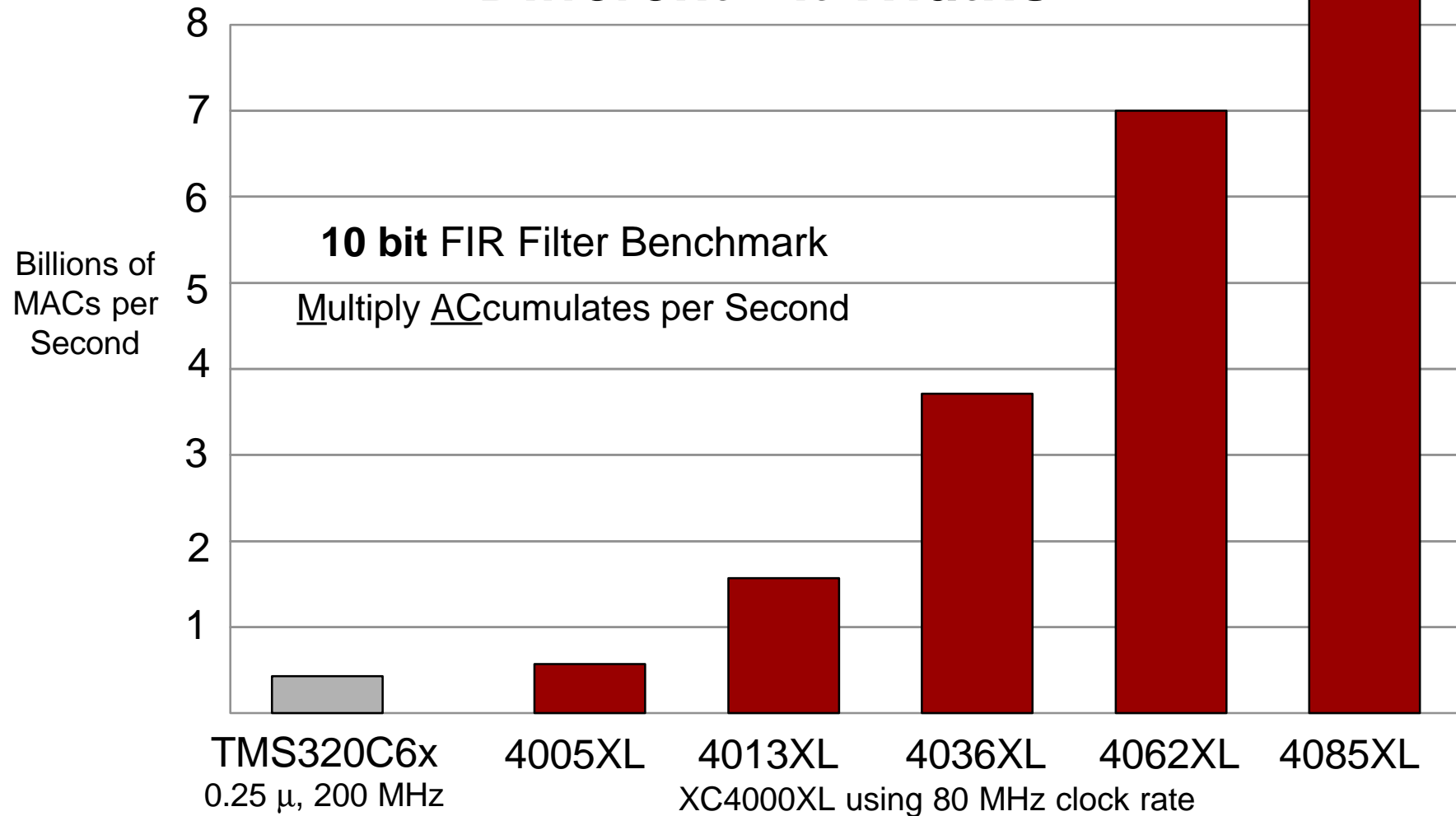
- Sequential processing
- Fixed architecture
- Complex real time software

- Parallel processing
- Configurable to specific needs
- No software programming

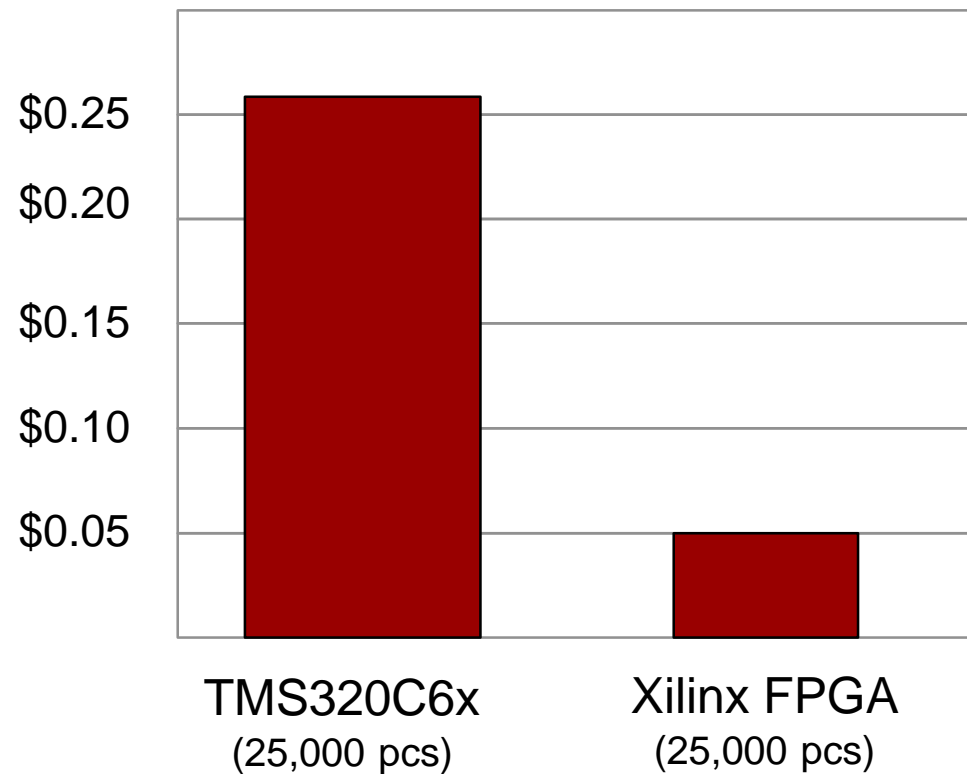
XC4085XL 10 Times Faster Than TMS320C6x



FPGAs Advantage Increases for Different Bit Widths

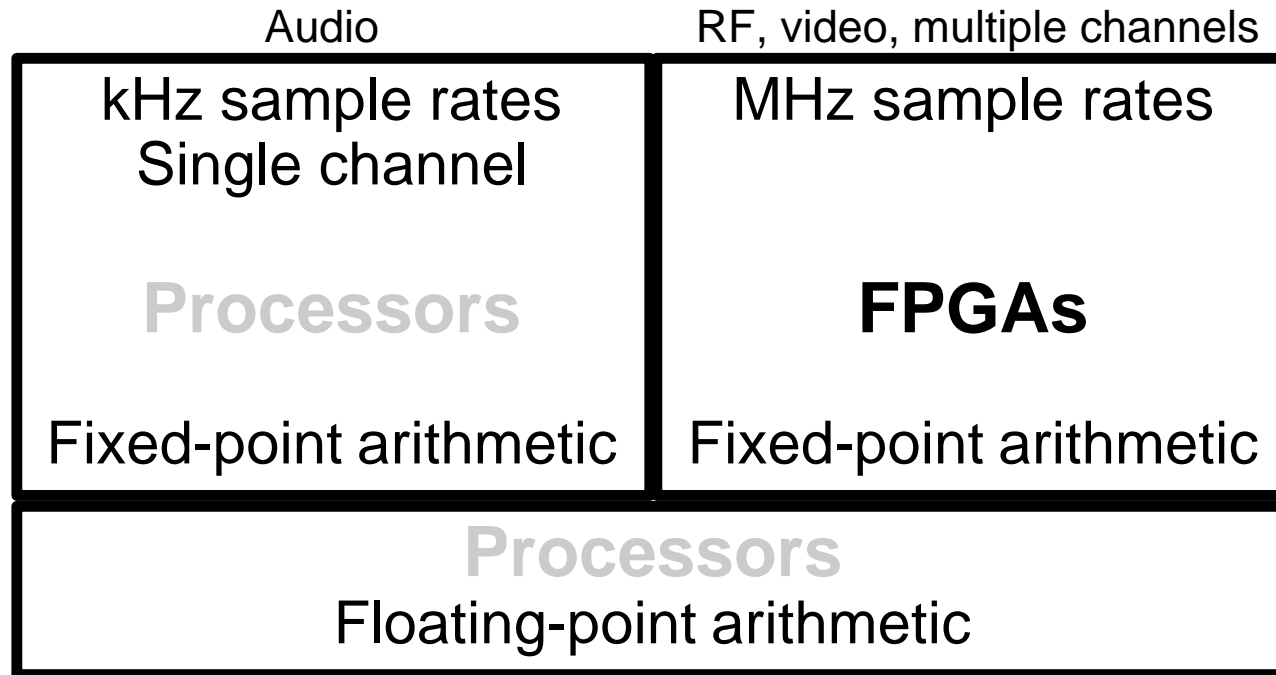


FPGA DSP is Lower Cost



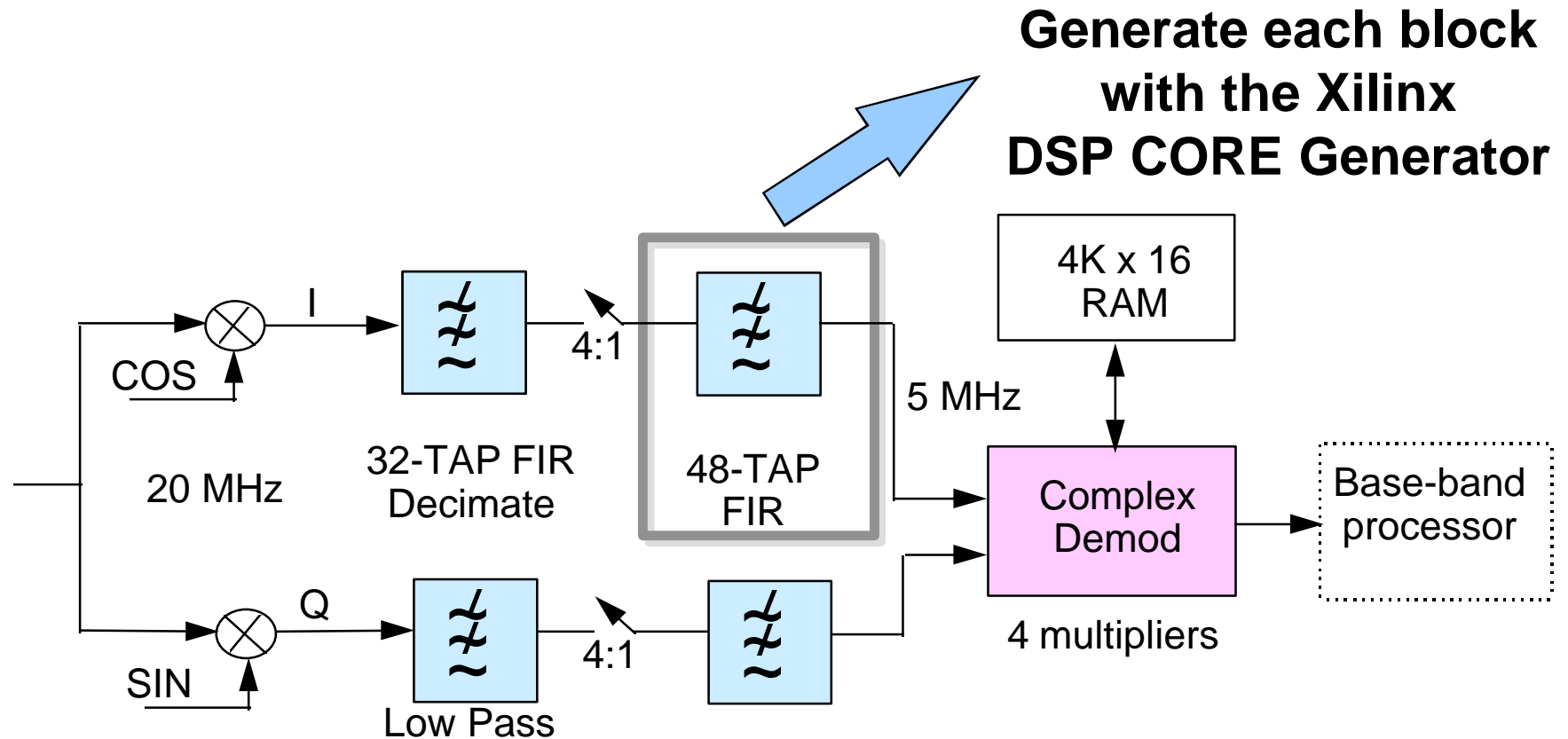
Price per Million MACs per Second - 16-bit word

Where FPGA Solutions Fit



FPGAs ideal for video rate and above using fixed-point arithmetic

Xilinx Makes DSP Design Easy



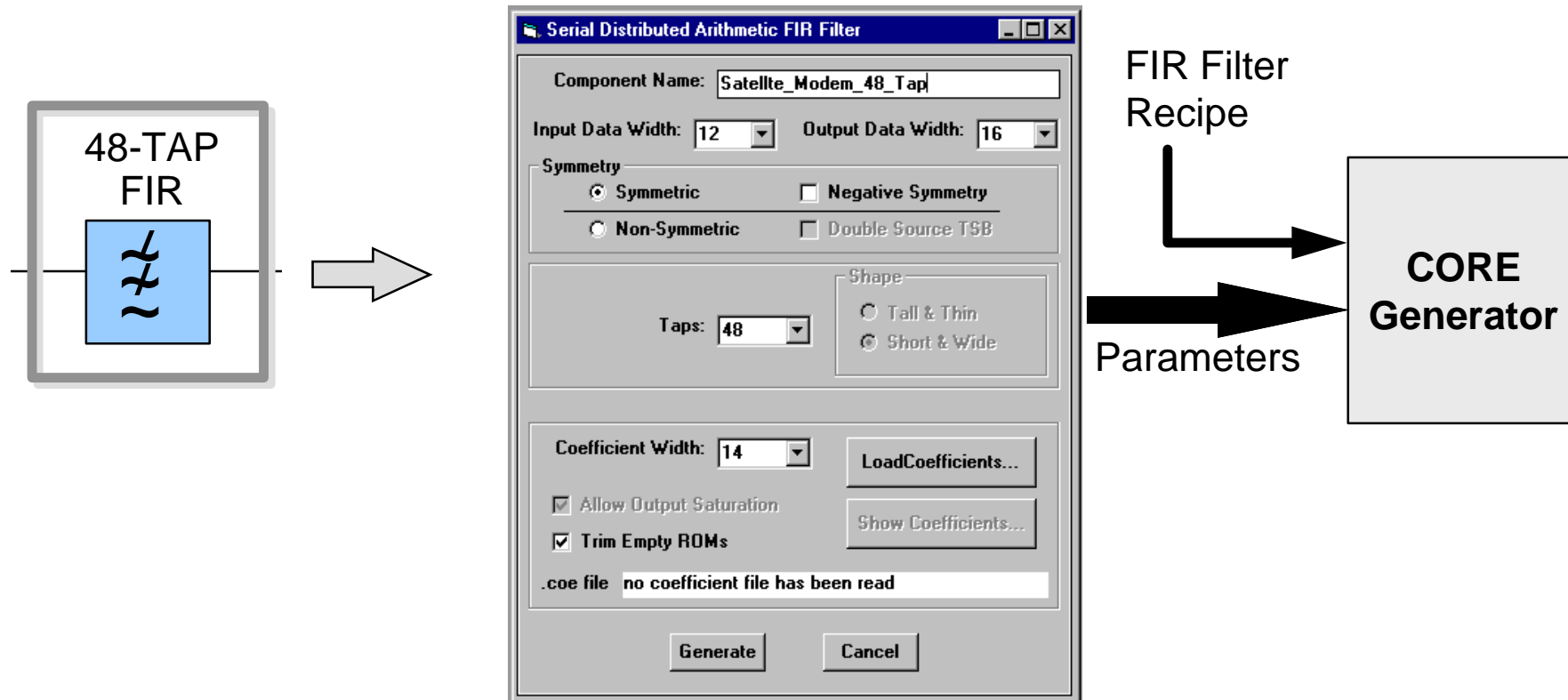
Complete design occupies 60% of XC4062XL

Xilinx CORE Generator For DSP

- Generates and delivers Xilinx DSP COREs
- Fully parameterized DSP COREs
 - Logic optimized for Xilinx FPGAs
 - Reduces overall design time - more successful turns-per-day
- Supports common design methodologies
 - VHDL, Verilog HDL
 - Schematic Capture (Foundation, Viewlogic, others...)

Simple, 2-Step CORE Generation Process

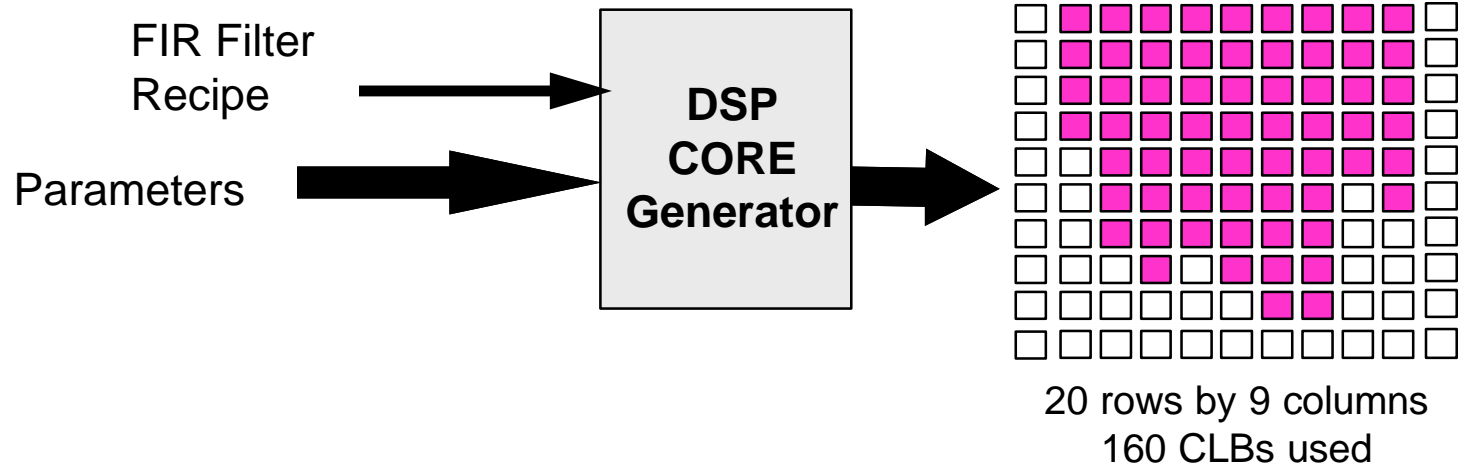
Parameterization Screen



1. Input the parameters that define the block
2. Generate the CORE

DSP CORE Generator Outputs

- Schematic symbol
- VHDL or Verilog HDL instantiation code
- Simulation model
- Design netlist with constraints



Use CORE as a system building block

FPGA DSP Solution Summary

- Performance: One FPGA equals 12 DSP CPUs
- Board Space: > 90% reduction
 - Single chip replaces 12 DSP CPUs
- Significant reduction in power consumption
- No multi-processor, real-time DSP software
 - Reduced technical and schedule risk
- Cost: > 50% cost savings over DSP CPU solution
 - HardWire cost reduction path available

FPGAs are the logical choice for DSP