

Case Studies

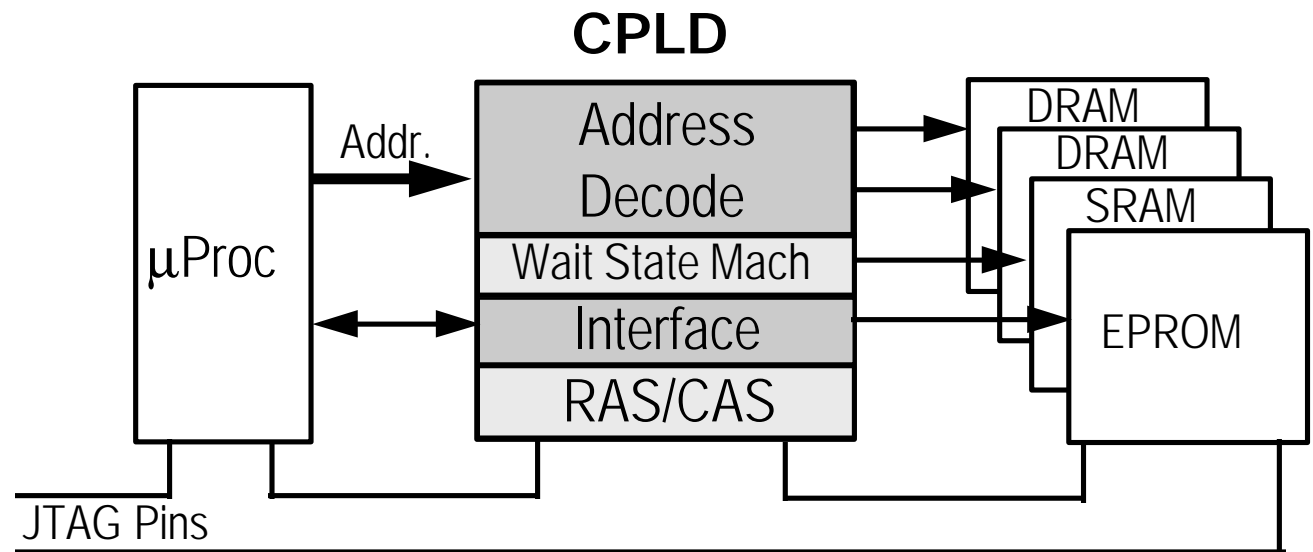
- **DRAM Controller: XC9500 ISP CPLD**
- Universal Serial Bus: XC4000E/X FPGA
- Peripheral Component Interconnect: XC4000E/X FPGA
- Digital Signal Processing: XC4000XL FPGA

Case Study #1 - DRAM Controller XC9500 CPLD

- Fast memory controller designed using Foundation VHDL tools
- Demonstrates XC9500 in-system programmability and pin-locking strengths

DRAM Controller Design Requirements

- User-reconfigurable memory space
- Fast address decode
 - 66 MHz
 - $t_{PD} \leq 7.5 \text{ ns}$
- Design on PC
- VHDL entry
- Low price



XC9500: A Perfect Fit

Requirement

- User-reconfigurable design
(memory space allocation)
- Fast address decode
 - 66 MHz
 - $t_{PD} \leq 7.5$ ns
- VHDL design entry on PC
- Low price

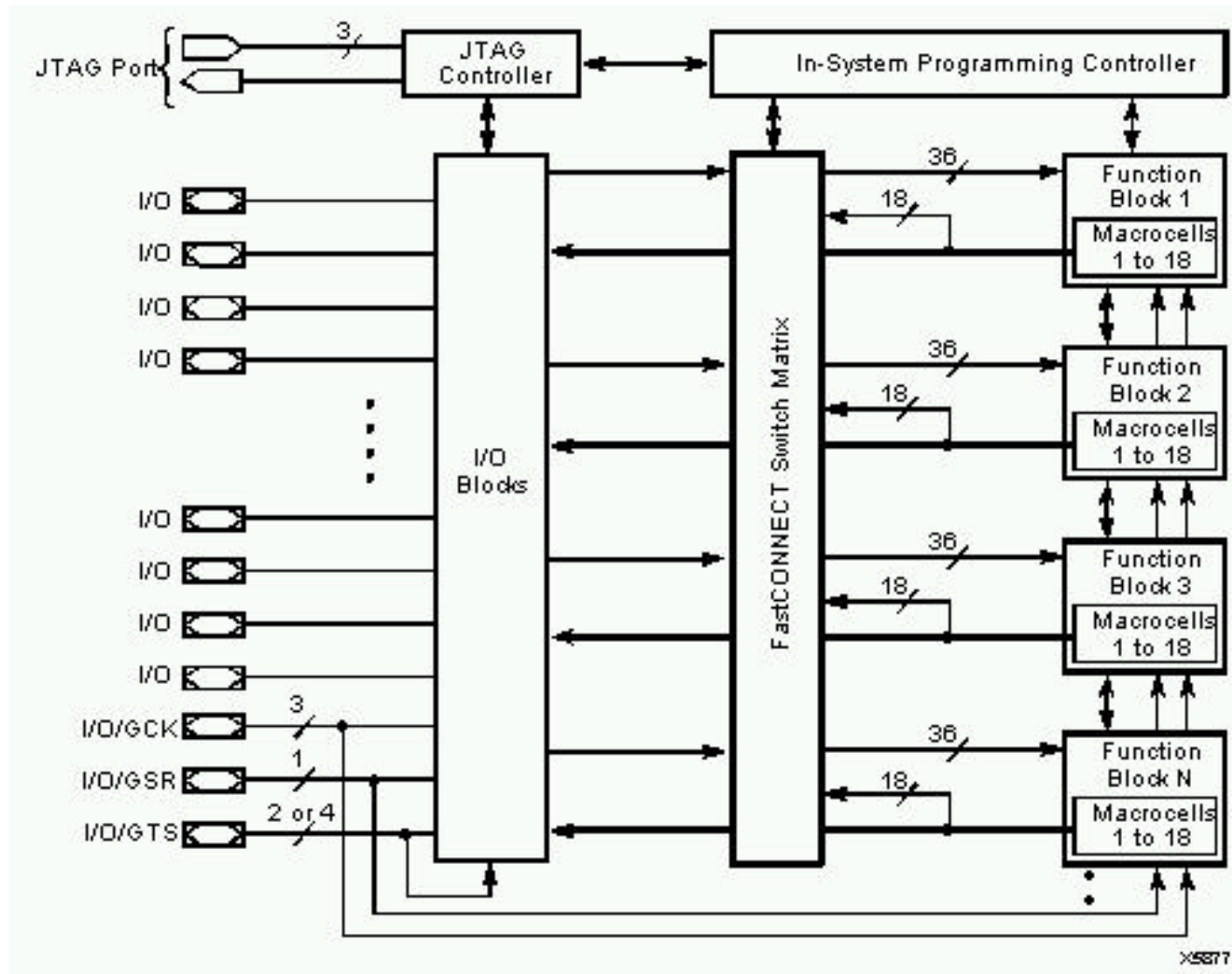
Solution

- 5 V In-System Programmable (ISP) CPLDs
- Industry's best pin-locking architecture
- Highest reprogramming reliability
 - 10,000 program/erase cycles
- High Performance: 5ns pin-to-pin
- High Density: up to 288 macrocells
- Xilinx Foundation Series Design Software
- Lowest-cost CPLD solution

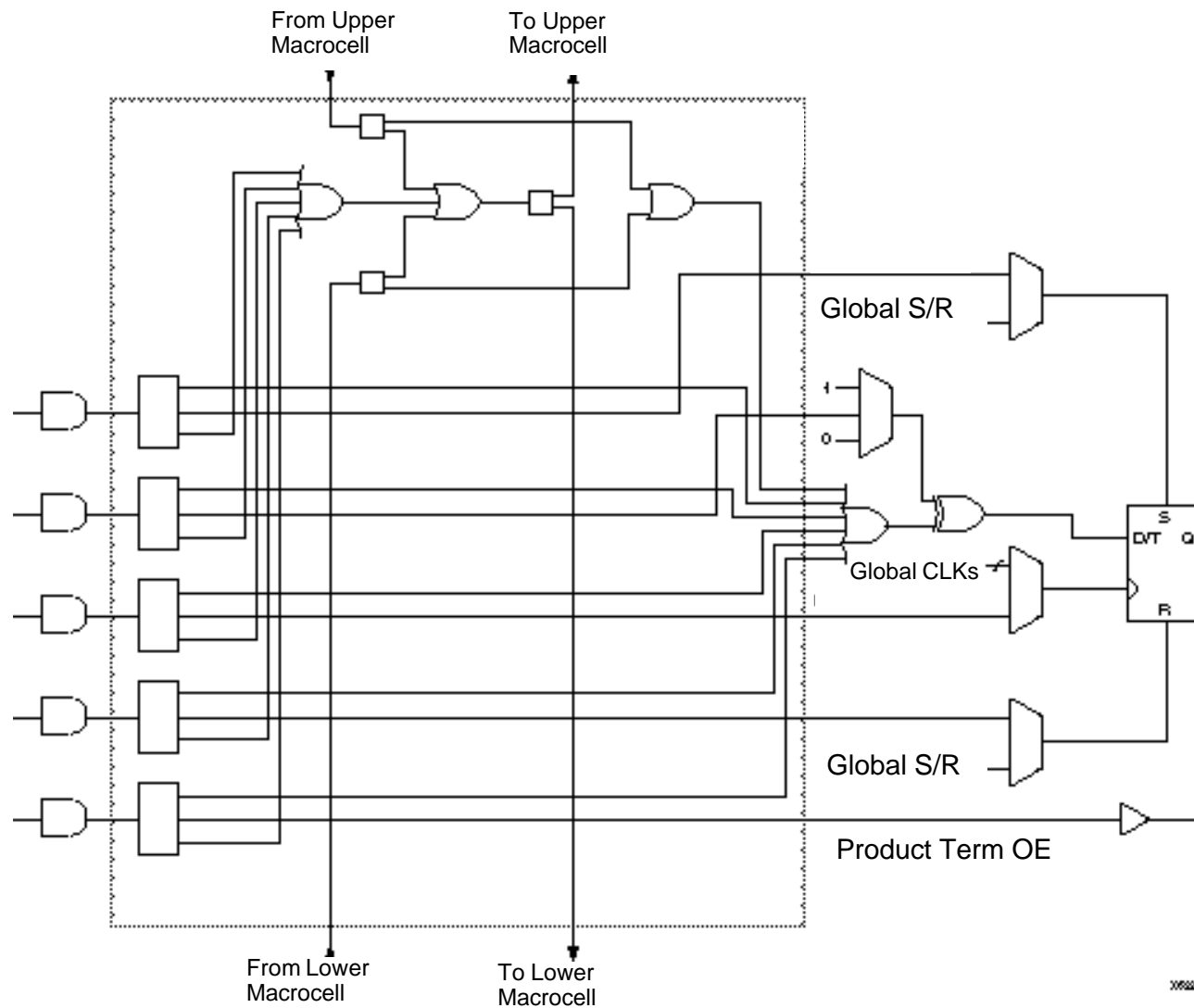
DRAM Controller Challenges

- Accommodate changing address ranges via in-system programming
- Maintain pinouts
- Maintain performance

XC9500: A Uniform CPLD Architecture



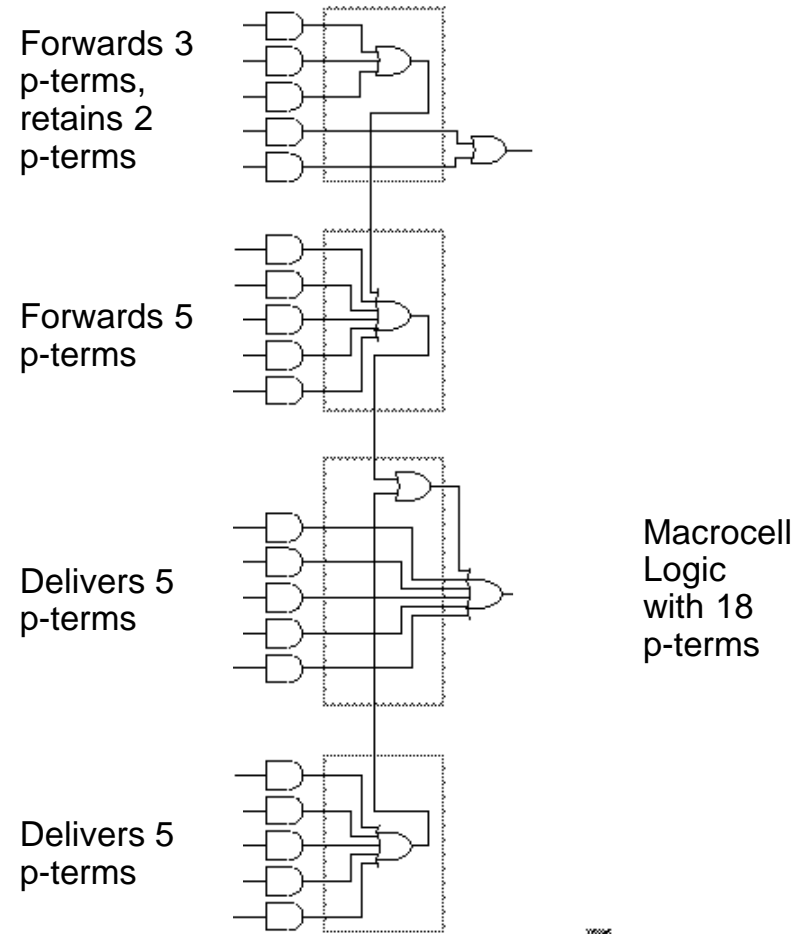
XC9500 Advanced Macrocell



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Flexible Cascading

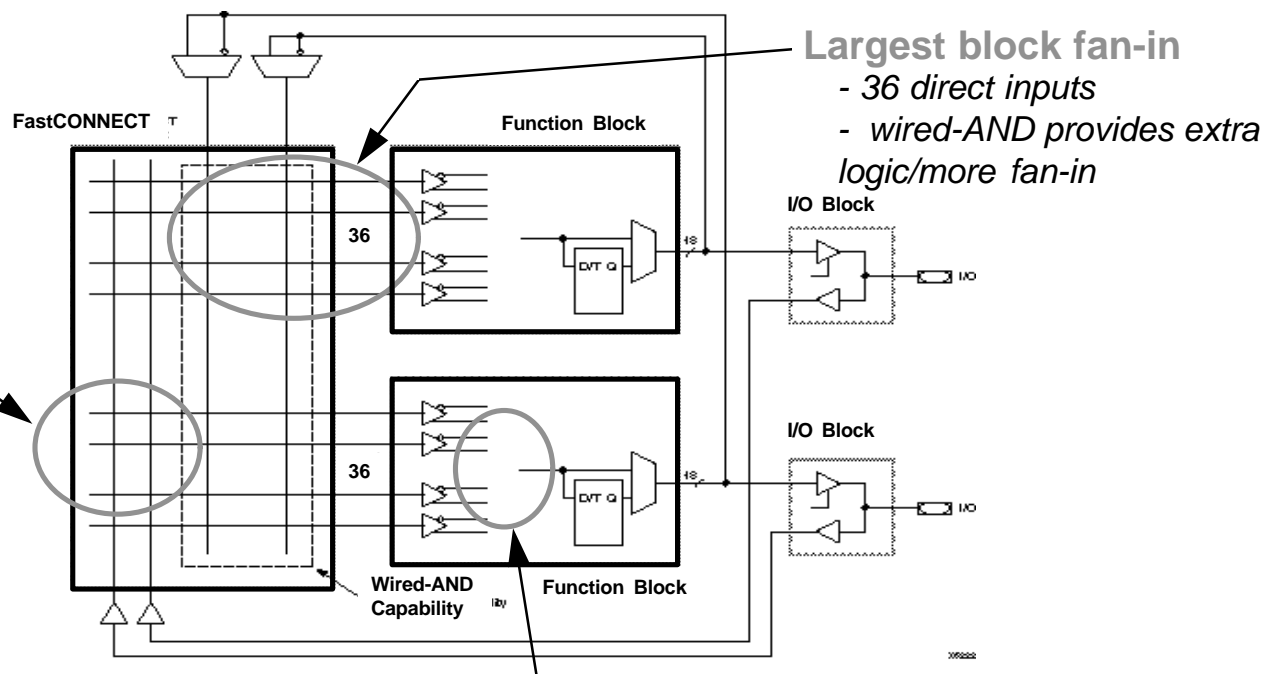
- Fast
- Bi-directional cascade
 - Collects / delivers available p-terms
- Automatically controlled by software
- One p-term granularity level



Leading Edge Features Support Superior Pin Locking for ISP

3X more routing switches

- superior input/feedback routability



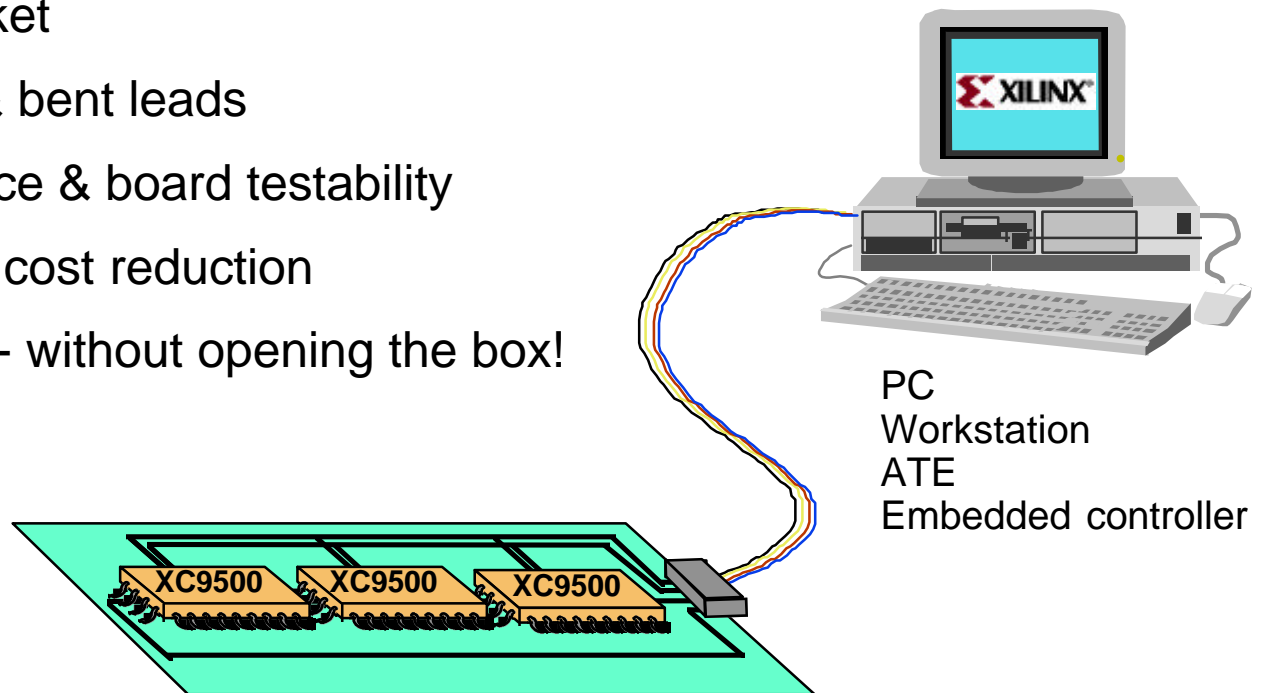
Largest block fan-in

- 36 direct inputs
- wired-AND provides extra logic/more fan-in

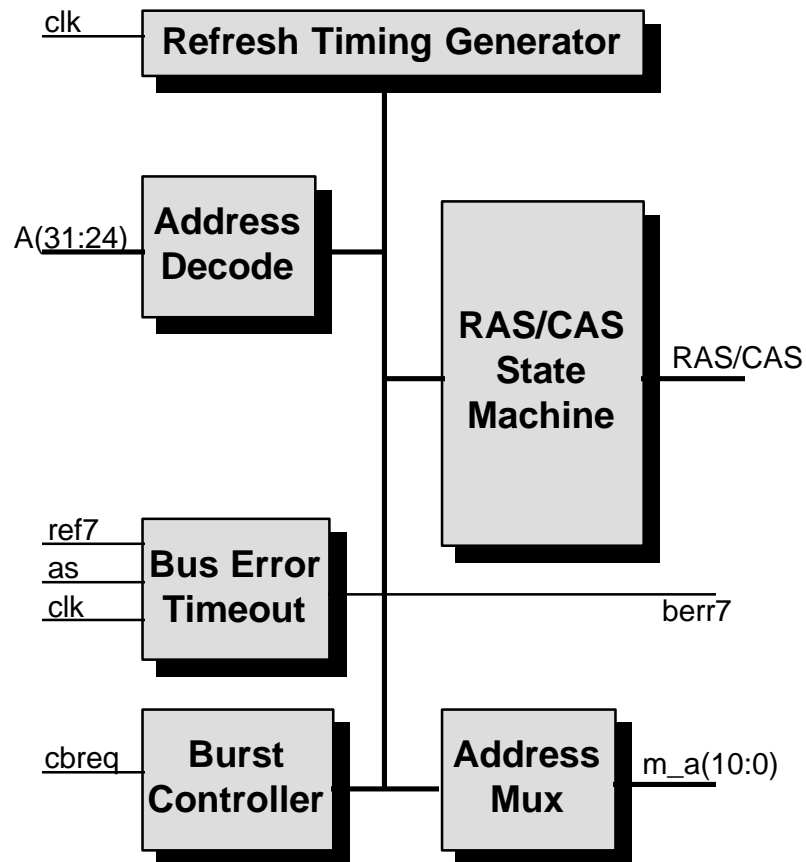
Powerful bi-directional logic allocation
- any number of p-terms (up to 90 max.)

XC9500 In-System Programming

- Faster, easier system prototyping
- Quicker time-to-market
- Eliminates sockets & bent leads
- JTAG improves device & board testability
- Significant inventory cost reduction
- Easy field upgrades - without opening the box!



DRAM Controller Block Diagram



Top Level VHDL Code

```
begin
dram_state_machine: dram_state port map
(reset, ref_rq, as, dram_rq, i25_clk, burst, siz, a (1
downto 0), ds, r_w, ras, cas, we, ref_cycle, cpu_cycle,
mux, cpu_ok, i_oe, dir);

burst_control_state_machine: burst_control port map
( reset, cbreq, cpu_ok, i25_clk, a (3 downto 2), burst,
bmx, cback, sterm, ba);

address_decoder: address_decode port map
(a (31 downto 24), as, i25_clk, dram_rq);

multiplexor : address_mux port map
(mux, bmx, a (23 downto 2), ba, m_a);

refresh_machine : refresh_gen port map
(i25_clk, ref_cycle, i_ref7, ref_rq);

buserr_machine: bus_error port map
(i_ref7, as, i25_clk, berr);

end behavior;
```

XC9500 Pin-Locking at Work

Retains Pinouts at Full Speed

```
11
12 architecture decode_arch of address_decode is
13 begin
14
15     process
16     begin
17         wait until i_as event and i_as = '1';
18         if i_a = "11111111" then dram_rq <= '1';
19         else dram_rq <= '0';
20         end if;
21     end process;
22
```

Design Change

```
11
12 architecture decode_arch of address_decode is
13 begin
14
15     process
16     begin
17         wait until i_as event and i_as = '1';
18         if i_a = "11000011" then dram_rq <= '1';
19         else dram_rq <= '0';
20         end if;
21     end process;
22
```

Minimum Clock Period: 13.5ns
Maximum Internal Clock Speed: 74.0Mhz
(Limited by Cycle Time)
Estimated Maximum External Clock Speed: 71.4Mhz
(Limited by Clock Pad to Output Pad)

No Performance Change

Minimum Clock Period: 13.5ns
Maximum Internal Clock Speed: 74.0Mhz
(Limited by Cycle Time)
Estimated Maximum External Clock Speed: 71.4Mhz
(Limited by Clock Pad to Output Pad)

So...What Changed?

***** FB1 *****

Number of function block inputs used/remaining: 36/0

Number of signals used by logic mapping into function block: 36

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pwr Mode	Pin #	Pin Type	Pin Use
DRAM_STATE_MACHINE/WAIT_COUNT<1>	9	4<-	0	0	FB1_1	STD	4	I/O	I
CBACK	4	0	1	0	FB1_2	STD	1	I/O	O
ADDRESS_DECODER/DRAM_RQ	1	0	0	4	FB1_3	STD	6	I/O	I
BUSERR_MACHINE/COUNTER<2>	2	0	0	3	FB1_4	STD	7	I/O	(b)
STERM	2	0	0	3	FB1_5	STD	2	I/O	O
BUSERR_MACHINE/COUNTER<1>	2	0	0	3	FB1_6	STD	3	I/O	I
M_A<0>	2	0	0	3	FB1_7	STD	11	I/O	O
BUSERR_MACHINE/COUNTER<0>	2	0	0	3	FB1_8	STD	5	I/O	I

All Pins
Remained
The Same

Nodes/P-terms
Remapped
Automatically

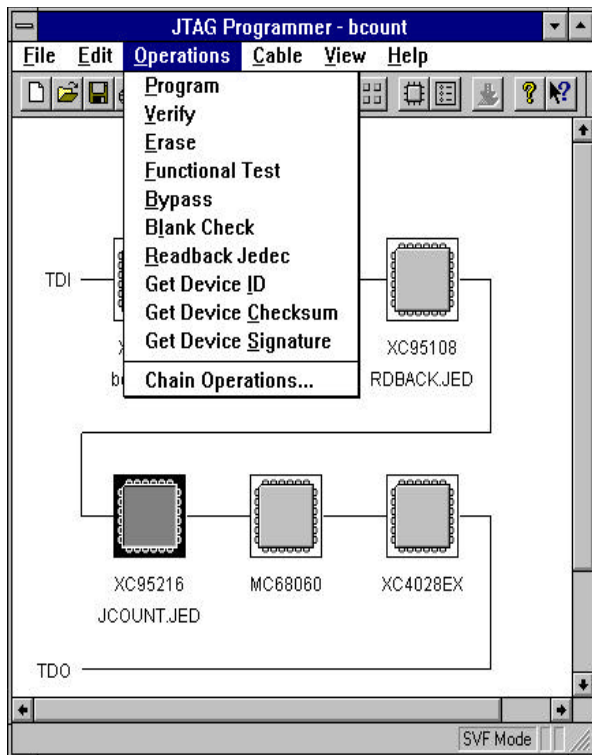
***** FB1 *****

Number of function block inputs used/remaining: 36/0

Number of signals used by logic mapping into function block: 36

Signal Name	Total Pt	Imp Pt	Exp Pt	Unused Pt	Loc	Pwr Mode	Pin #	Pin Type	Pin Use
REFRESH_MACHINE/COUNTER<0>	1	0	2	2	FB1_1	STD	4	I/O	I
CBACK	4	0	0	1	FB1_2	STD	1	I/O	O
NOC	1	0	0	4	FB1_3	STD	6	I/O	I
NOB	1	0	0	4	FB1_4	STD	7	I/O	(b)
STERM	2	0	0	3	FB1_5	STD	2	I/O	O
ADDRESS_DECODER/DRAM_RQ	1	0	0	4	FB1_6	STD	3	I/O	I
M_A<0>	2	0	0	3	FB1_7	STD	11	I/O	O
BURST_CONTROL_STATE_MACHINE/WAIT_COUNT<3>	2	0	0	3	FB1_8	STD	5	I/O	I

ISP Downloading is Simple and Easy



- Attach cable between target and computer
- Enter JTAG download software
- Identify devices in chain
- Provide design file to software
- Press “program”

XC9500 Case Study Highlights

- High performance, lowest cost
- Easy implementation
- Flexible architecture
- Industry's best pin-locking
- 5 V ISP support - prototyping through field upgrade
- Push-button VHDL using Foundation Series