



## **Release Document**

**XACT*step* Version 5.2/6.0**  
**Viewlogic**

**October 1995**

**Read This Before Installation**



# XACT 6.0 Install for Windows

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The following information supersedes the instructions in the *Getting Started & Installation Guide* for installing XACTstep 6.0 software on PCs running Microsoft Windows. These steps minimize XACTstep 6.0 problems caused by PC resource issues and Microsoft Windows configurations that are not optimal.

**Note:** After installation is complete, the install program will present you with required environment variable settings for your autoexec.bat program. In some cases this may include multiple paths to the PROSeries tools. The duplicate entry will not prevent the software from running, and can be deleted.

For complete configuration instructions, please see the “Setting Up the Xilinx Environment” chapter of the *Getting Started & Installation Guide*.

1. Before starting the XACTstep 6.0 installation process, Xilinx recommends that you make backup copies of the win.ini and system.ini files located in your Windows directory.
2. Before starting Windows, run a batch file called rmwin32s.bat in DOS to remove any previous version of the Microsoft WIN32S driver that may be installed on your PC.

The latest version (v1.25.142.0) is necessary for use with XACTstep 6.0 and is compatible with all previous versions. If you are not sure if WIN32S is installed on your PC, you can still run this program. If the driver is not installed, rmwin32s.bat tries to delete certain files and then reports that these files could not be found.

To run `rmwin32s.bat`, first identify the CD-ROM drive letter, for example, `D:\`.

From the DOS command prompt, type the following:

```
d:\xbbs\utils\rmwin32s.bat
```

If the WIN32S driver is found, all associated files are removed from your system, and you are prompted to manually remove `winmm16.dll` and `device=...W32S.386` from your `system.ini` file.

3. Next, start Microsoft Windows.
4. In Windows, select **File** → **Run** from the Program Manager.
5. In the command line box, type the following:

```
d:\win32s\disk1\setup.exe
```

This step installs the latest version of the Microsoft WIN32S driver needed for XACTstep 6.0 applications.

6. Select **File** → **Run** from the Program Manager.
7. In the command line box, type the following:

```
d:\xbbs\utils\xinfo\xinfo.exe
```

XINFO is a Xilinx utility that analyzes your computer's system resources for compatibility with the XACTstep software. Review the "Hints" page for suggestions on changes that you should make to your PC configuration to allow XACTstep 6.0 to run more efficiently on your PC.

8. Select **File** → **Run** from the Program Manager.
9. To begin the installation of the XACTstep 6.0 toolset, type the following in the command line box:

```
d:\setup.exe
```

**Note:** Preliminary calculations of disk space requirements may be inaccurate, depending on how your hard disk is formatted. To identify required disk space accurately, the Install program must calculate disk space on the basis of the selected products list. Using Custom Install, you can correctly calculate the required disk space by turning on the Analyze Disk Space option after making your selections. Using Quick Install, simply continuing the installation process by selecting the Install button correctly calculates the available disk space.

10. After installation is complete, exit from Windows.

11. Using a text editor, load `c:\autoexec.bat`.

Certain *XACTstep* tools require that the temporary variable be set. If you do not see a line such as “`set temp=c:\temp`” in your `autoexec.bat` file, add it to this file. (The location of the temporary directory is not important; only the existence of the variable and a valid path are important.)

12. Next, reboot your PC to ensure that all environment variables have been set correctly.

Refer to the *Getting Started & Installation Guide* for information on other topics, such as environment variables and disk space requirements.



# Installing Online Documentation

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Starting with the 5.2/6.0 release, online documentation is now available on the Sun and HP workstations.

## Installing Online Documentation on a Sun Workstation

To use online documentation, you must install the Acrobat reader and the online documents on your workstation.

### Installing the Reader and Documents

Version 1.0 of the Acrobat reader is included on the XACTstep Sun 5.2 CD-ROM disk. To install the Acrobat reader, follow the instructions on page 4-4 of the *Getting Started & Installation Guide*.

Because the online documents are in tar format, you must use the XACTstep 5.2 installation program to install the online documents on your workstation. Refer to the Sun4 instructions on page 3-2 of the *Getting Started & Installation Guide*.

### Opening Documents with Acrobat Reader — Sun Workstation Installations

To access the AcroRead program from the command line, follow these instructions:

1. Include the path to the /AcroRead\_1.0/bin directory in the \$path variable of your configuration file,
2. At the command line, type the following to invoke the Acrobat reader:

```
acroread
```

The Open file dialog box of the Acrobat reader is displayed.

3. Specify the following path in the Filter box of the Open file dialog box to view Xilinx Online Documents:

```
/xact_dir/online/online/*.pdf
```

To view Xilinx Application Information, specify the following path:

```
/xact_dir/online/onlinedb/*.pdf
```

4. Select the document you want from the displayed list of .pdf files.

## Installing Online Documentation on a HP Workstation

To use online documentation, you must install the Acrobat reader and, optionally, the online documents on your workstation.

### Installing the Reader and Documents

Version 2.1 of the Acrobat reader is available on HP workstations on a separate enclosed Acrobat CD-ROM disk also provided by Xilinx. Use the instructions outlined in this section to install the Acrobat software on an HP workstation.

Installation of the Acrobat reader requires the HP-UX 9.05 operating system, the HP-VUE window manager, and 12 MB of disk space. You do not have to install the online documents to your hard disk, but if you choose to do so, you will need 52 MB of disk space.

1. Insert the CD-ROM disk into the CD-ROM drive.
2. Mount the CD-ROM drive. You need system administrator privileges to complete this step.
3. Invoke the Acrobat Installation program as follows:

```
/cdrom_dir/acrobat/unix/install
```

By default, after you have installed the desired products to your HP workstation, the installation program copies the Acrobat reader to the /usr/AcroRead directory. Xilinx recommends that you install the reader to /xact\_dir/doc/AcroRead. You must include the AcroRead/bin directory in your path.



For more information, print the “Introducing Adobe Acrobat Reader 2.1” file located in `/cdrom_dir/acrobat/unix/instguid.txt`.

**Note:** If you want to install the document files on your workstation, copy the `/cdrom_dir/onlindb` and `/cdrom_dir/online` directory trees from the XACTstep Version 5.2 CD-ROM to your disk. For example:

```
cp -Rp /cdrom_dir/onlindb /xact_dir/doc/onlindb ↵
cp -Rp /cdrom_dir/online /xact_dir/doc/online ↵
chmod -R u+w xact_dir/doc↵
```

## Opening Documents with Acrobat Reader — HP Workstation Installations

To view documents on an HP workstation, follow the instructions outlined in this section. For additional information refer to the “Viewing Documents with Acrobat Reader” section on page 4-7 of the *Getting Started & Installation Guide*.

You can either start the reader first and then decide what type of documents you want to view, or you can open the type of documents you want to view at the same time you load the reader.

To start the reader without specifying any documents, follow these instructions:

1. Ensure that the Acrobat Reader `AcroRead/bin` directory is in your path.
2. To start the reader, type the following:  
**acroread**
3. Specify one of the following paths corresponding to the type of documents you wish to view:

To view Xilinx Online Documents, open the file:

`/cdrom_dir/online/linkpage.pdf`

or

`/xact_dir/online/linkpage.pdf`

To view Xilinx Application Information, open the file:

`/cdrom_dir/onlindb/dblink.pdf`

or

`/xact_dir/onlindb/dblink.pdf`

To specify the type of documents you wish to view at the time you invoke the reader, include the path you want after the `acroread` command as follows:

To view Xilinx Online Documents, use the command:

`acroread /cdrom_dir/online/linkpage.pdf &`

or

`acroread /xact_dir/online/linkpage.pdf &`

To view Xilinx Application Information, use the command:

`acroread /cdrom_dir/onlindb/dblink.pdf &`

or

`acroread /xact_dir/onlindb/dblink.pdf &`

# Versions and Compatibility

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The following master table indicates Xilinx core software with the current version numbers.

## Software Versions

| Program             | Windows Version | DOS Version | Workstation Version |
|---------------------|-----------------|-------------|---------------------|
| APR                 | 5.2             | 5.2         | 5.2                 |
| APRLOOP             | 5.2             | 5.2         | 5.2                 |
| CstCvt              | 5.2             | 5.2         | 5.2                 |
| Design Manager      | 6.0             | N/A         | N/A                 |
| Floorplanner        | 6.0             | N/A         | 5.2                 |
| Flow Engine         | 6.0             | N/A         | N/A                 |
| Hardware Debugger   | 6.0             | N/A         | N/A                 |
| HM2RPM              | 5.2             | 5.2         | 5.2                 |
| LCA2XNF             | 5.2             | 5.2         | 5.2                 |
| MakeBits            | 5.2             | 5.2         | 5.2                 |
| MakePROM            | 5.2             | 5.2         | 5.2                 |
| MAP2LCA             | 5.2             | 5.2         | 5.2                 |
| MemGen              | 5.2             | 5.2         | 5.2                 |
| PPR                 | 5.2             | 5.2         | 5.2                 |
| PROM File Formatter | 6.0             | N/A         | N/A                 |
| Report Browser      | 6.0             | N/A         | N/A                 |
| SymGen              | 5.2             | 5.2         | 5.2                 |
| Timing Analyzer     | 6.0             | N/A         | N/A                 |

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| Program  | Windows Version | DOS Version | Workstation Version |
|----------|-----------------|-------------|---------------------|
| XACT     | 5.2             | 5.2         | 5.2                 |
| XBLOX    | 5.2             | 5.2         | 5.2                 |
| XChecker | 5.2             | 5.2         | 5.2                 |
| XCK88    | N/A             | 5.2         | N/A                 |
| XDE      | 5.2             | 5.2         | 5.2                 |
| XDelay   | 5.2             | 5.2         | 5.2                 |
| XDM      | N/A             | N/A         | 5.2                 |
| xdm      | 5.2             | 5.2         | 5.2                 |
| XEMake   | N/A             | N/A         | 5.2                 |
| XEMake6  | 6.0             | N/A         | N/A                 |
| XKey     | 5.2             | 5.2         | N/A                 |
| XMake    | 5.2             | 5.2         | 5.2                 |
| XNFBA    | 5.2             | 5.2         | 5.2                 |
| XNFCvt   | 5.2             | 5.2         | 5.2                 |
| XNFMAP   | 5.2             | 5.2         | 5.2                 |
| XNFMerge | 5.2             | 5.2         | 5.2                 |
| XNFPrep  | 5.2             | 5.2         | 5.2                 |
| XPP      | 5.2             | 5.2         | 5.2                 |
| XPrint   | 5.2             | 5.2         | 5.2                 |
| XSimMake | 5.2             | 5.2         | 5.2                 |

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## Introduction

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Welcome to the Viewlogic PRO Series Interface from Xilinx!

Xilinx software products have prefixes to designate the type of products you receive.

- DS = Development System (new system)
- DX = Development System Upgrade (upgrade to current system)
- SC = Support Contract (update to current system)
- SR = Support Reinstatement (update for non-current system)
- BU = Base Update (update to current system)

The labels on the box indicate the product you have received.

This release note supports the following products.

- PROcapture Schematic Entry, Interface, and Libraries (DS-390)
- PROsim Simulator, Interface, and Libraries (DS-290)
- Viewlogic Stand-Alone Base Development System (DS-VLS-BAS)
- Viewlogic Stand-Alone Standard Development System (DS-VLS-STD)
- Viewlogic Stand-Alone Extended Development System (DS-VLS-EXT)
- Viewlogic Base Development System (DS-VL-BAS)
- Viewlogic Standard Development System (DS-VL-STD)

## Contents

The Development System (DS) product you received contains software, documentation, and/or hardware. New DS Base, Standard, and Extended packages contain hardware, software, and documentation. Interface and Update products have software and documentation only.

### Hardware<sup>1</sup>

The hardware consists of the following items.

- XChecker Download and Readback Cable Set (included in STD, EXT, and VLS-BAS packages)
- Parallel Download Cable (included in VL-BAS package)
- Xilinx C Programmable Key (beige) for PCs (included in STD, EXT, and VLS-BAS packages )

### Software

Xilinx software for all platforms is provided on CD-ROM. It consists of the following.

- Installation Program
- FPGA Core Implementation Tools (DS-502)
- FPGA Base Implementation Tools (included in DS-VL-BAS and DS-VLS-BAS only)
- PROsynthesis, VHDL synthesizer (included in DS-VLS-EXT only)
- PROcapture Schematic Entry, Interface, and Libraries (DS-390 and VLS packages only)
- PROsim Simulator, Interface, and Libraries (DS-290 and VLS packages only<sup>2</sup>)
- XEPLD Translator Core Tools (DS-550)
- X-BLOX (DS-380) (included in STD and EXT packages only)

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1. Included in DS packages only.

2. VLS-BAS can simulate up to 5000 gates.

## Documentation

The following documentation is available in print for Viewlogic products.

- *Getting Started & Installation Guide*
- *Additional Products & Services Packet*
- *Viewlogic Interface Guide*
- *Viewlogic Tutorials*

## Online Documentation

The following online documentation is included with your Viewlogic products.

- *Libraries Guide*
- *Libraries Supplement Guide*
- *X-BLOX Reference/User Guide*
- *Viewlogic Design Analysis Guide*
- *Viewlogic Design Entry Guide*
- *Floorplanner Reference/User Guide*
- *Design Manager/Flow Engine Reference/User Guide*
- *Timing Analyzer Reference/User Guide*
- *Hardware Debugger Reference/User Guide*
- *PROM File Formatter Reference/User Guide*
- *Development System User Guide*
- *Development System Reference Guide, Vols 1-3*
- *Hardware & Peripherals User Guide*
- *XEPLD Reference Guide*
- *XEPLD Design Guide*
- *XEPLD Schematic Design Guide*
- *XEPLD Reference Guide (for Windows)*
- *XEPLD Schematic Design Guide (for Windows)*

**Note:** Xilinx Core FPGA and EPLD documentation for Sun and PC platforms is available online via CD-ROM. Some documentation for product updates and for other workstation platforms is included on the basis of product configuration.

Selected Xilinx manuals are available in printed form. See the “Documentation Order Form” in the *Additional Products & Services Packet*. Printed copies of the *Viewlogic Design Analysis Guide* and the *Viewlogic Design Entry Guide* are available from Viewlogic.

## Maintenance and Support

This product comes with free technical and product information telephone support (toll-free in the U.S. and Canada). You can also fax and e-mail your questions. See the “Xilinx Customer Support Information” chapter of this release note for offices and phone numbers.

This product comes with one year of maintenance<sup>1</sup>; you will receive all software and documentation updates automatically during that time. You will receive a notice at the end of the year giving instructions on how to renew your maintenance contract.

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1. Not included with DS-VL-BAS.

## Features in This Release

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This chapter lists the new features in this release.

### PRO Series 6.1

A new version of the Viewlogic PRO Series software, Version 6.1, is included in this release. PRO Series V6.1 offers the following features.

#### PROflow Support for XACTstep 6

PROflow has been updated to add support for the XACTstep 6 software. Selecting the XACT 6 button invokes the new Xilinx Design Manager, which provides access to all the new tools such as the Floorplanner<sup>1</sup>, the Hardware Debugger, and the Timing Analyzer.

#### Windows Printing

PRO Series supports Windows printing for easier and faster printing. All printing uses the Windows printing drivers and dialog boxes.

#### Project Archive Utility

The Project Archive Utility is a project management capability that allows you to create an archive file containing a complete collection of all schematics, symbols, and other data contained throughout the hierarchy of a specified project. It preserves completed designs and conserves disk space.

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1. Not included in the DS-VLS-BAS package.

## VSM Dialog Box

The Tools → Link to PROsim menu command opens a new GUI for the VSM program. However, it is recommended that you use PROflow for simulation. For designs that contain X-BLOX, RAMs/ROMs, or Xilinx ABEL modules, use PROflow or XSimMake to simulate your design.

## Set FPGA Library Option on Library List Editor

The Set FPGA Library button appears in the Library List Editor. When you select this button, the Xilinx libraries are automatically set in the viewdraw.ini file. This functionality is also available in PROflow by simply selecting the family when you create a project.

## New Online Documentation for PRO Series

All the Viewlogic PRO Series documentation is online and available on the Xilinx XACTstep CD. The online documentation has an easy search-and-find utility and can print any number of pages.

## Online Help in PROflow

PROflow, the design flow manager, has extensive online help to guide you through the entire design process. The online help is easy to use and covers all aspects of the design flow, including design entry, design verification, and design implementation. Look at this help first for answers to all your design flow questions.

Using PROflow to create EPLD designs is documented online. Using PROflow for FPGAs is documented in the *Viewlogic Interface Guide* and the *Viewlogic Tutorials* manual.

## Interface and Libraries

The following changes have been made to the interface and libraries for this release.

## Library Support for XC5200

New schematic and simulation libraries have been added to support the XC5200 device family. For more information on this family, see the 1994 *Programmable Logic Data Book, Third Edition*.

## XNF Version 6 Support

This version of the XNF file supports the new XC5200 Xilinx product family.

## X-BLOX Support

X-BLOX supports the XC5200 device family for all platforms.

## Increased Clock-to-Clock Performance

This section describes changed criteria for merging flip-flops into IOBs.

Platform: All

Architecture: XC4000A/D, XC3000A/L, XC3100A

The default criteria for merging registers into IOBs have changed to improve clock-to-clock performance. If you do not specify otherwise, X-BLOX pushes a flip-flop into an IOB where it improves the clock-to-out performance according to the following rules.

- X-BLOX merges a flip-flop into an OUTFF in an IOB if one or both of the following conditions apply.
  - The flip-flop D pin is sourced either directly or indirectly by non-combinational logic. Indirect sourcing occurs where one or more buffers and/or inverters, and no other logic, are found between the non-combinational source and the D pin.
  - If the flip-flop was generated from an X-BLOX symbol, the source X-BLOX symbol has a parameter that indicates it should be implemented in an IOB, for example, STYLE=IOB.
- Criteria for merging flip-flops into INFFs in an IOB have not changed.

**Note:** In a design compiled with a previous version of X-BLOX, the clock-to-clock timing might be faster if STYLE is not specified. However, in some cases the clock-to-pad speed might be slower. If clock-to-pad speed is critical in your design, use registers in the IOB. For example, use the STYLE=IOB or STYLE-=OFD definitions for DATA\_REG.

## Reduced Memory Usage

For all platforms and architectures, memory-saving enhancements made to X-BLOX lead to significant reductions in memory usage, by as much as 50 percent for certain styles of designs.

## X-BLOX Reference/User Guide Changes

The following modules have changed to support the XC5200 architecture. Modules which are not included are valid as described in the *X-BLOX Reference/User Guide*. The XC5200 attribute information in this section will be incorporated in the next revision of the *X-BLOX Reference/User Guide*.

### **ACCUM**

Attribute: STYLE can be set to ALIGNED, UNALIGNED, or RIPPLE.

### **ADD\_SUB**

Attribute: STYLE can be set to ALIGNED, UNALIGNED, or RIPPLE.

### **ANDBUS**

Attribute: STYLE is not supported.

### **BIDIR\_IO**

Attribute: NODELAY attribute can now be attached.

### **COMPARE**

Attribute: STYLE can be set to ARITH, TREE, or RIPPLE.  
STYLE=WIRED is not supported.



## **DATA\_REG**

Attribute:

STYLE=FD is added for implementation using CLB flip-flops.

STYLE=LD is added for implementation using CLB latches.

STYLE=CLB is not supported; use STYLE=FD or STYLE=LD.

STYLE=IOB is not supported.

STYLE=ILD is not supported.

STYLE=IFD is not supported.

STYLE=OFD is not supported.

**Note:** For XC3000 and 4000 designs, the NODELAY attribute can be added to the DATA\_REG symbol. For XC5200 designs, attach the NODELAY attribute to either the INPUTS or BIDIR\_IO symbols.

## **INC\_DEC**

Attribute: STYLE can be set to ALIGNED, UNALIGNED, or RIPPLE.

## **INPUTS**

Attribute: The NODELAY attribute can now be attached.

## **SHIFT**

Attributes: remain unaffected.

## **TRISTATE**

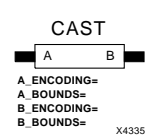
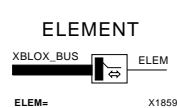
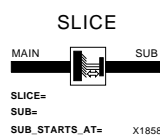
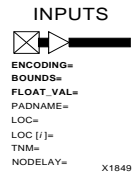
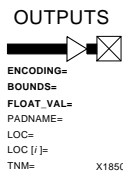
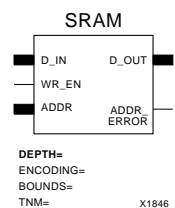
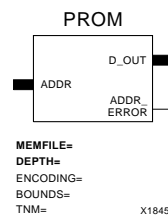
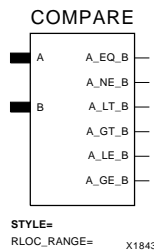
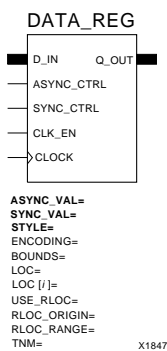
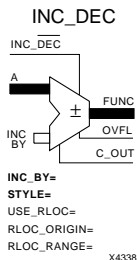
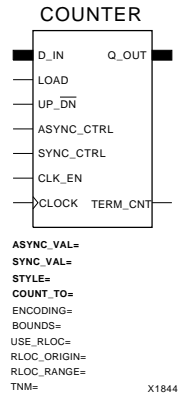
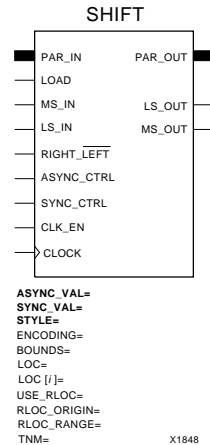
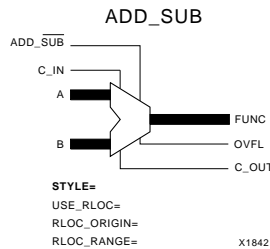
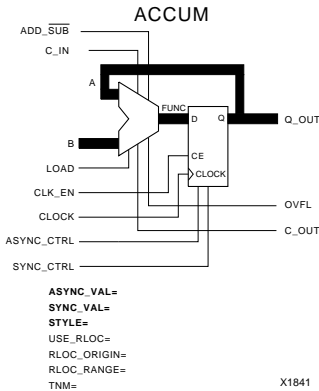
Attribute: FLOAT\_VAL is not supported.

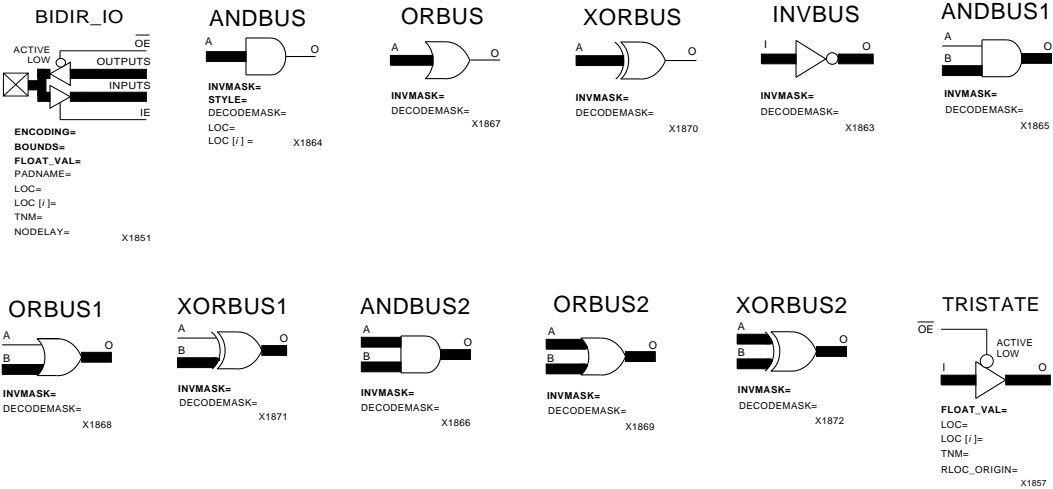
## **SRAM**

The SRAM symbol is not supported for XC5200.

# Summary of X-BLOX Symbols

Attributes that appear on schematic symbols are in bold type. Optional attributes appear in plain text. The X-BLOX symbols that are not displayed are valid as shown on the X-BLOX Symbols Reference Card.







# Chapter 3

## Device and Package Support

The following is a master table of Xilinx devices for this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*.

| Device                | Packages   | Speed Grades              |
|-----------------------|--|---------------------------|
| XC2018 <sup>a</sup>   | PC44, PC68, PC84, PG84, TQ100, VQ64                  | -33, -50, -70, -100, -130 |
| XC2064 <sup>a</sup>   | PC44, PC68, PD48, PG68                               | -33, -50, -70, -100, -130 |
| XC2018L <sup>a</sup>  | PC84, VQ64, VQ100                                    | -10                       |
| XC2064L <sup>a</sup>  | PC68, VQ64   | -10                       |
| XC3020 <sup>a</sup>   | CB100, CQ100, PC68, PC84, PG84, PQ100                | -50, -70, -100, -125      |
| XC3030 <sup>a</sup>   | PC44, PC68, PC84, PG84, PQ100, TQ100                 | -50, -70, -100, -125      |
| XC3042 <sup>a</sup>   | CB100, CQ100, PC84, PG84, PG132, PP132, PQ100, TQ100 | -50, -70, -100, -125      |
| XC3064 <sup>a b</sup> | PC84, PG132, PP132, PQ160                            | -50, -70, -100, -125      |
| XC3090 <sup>a b</sup> | CB164, CQ164, PC84, PG175, PP175, PQ160, PQ208       | -50, -70, -100, -125      |
| XC3020A               | CB100, PC68, PC84, PG84, PQ100                       | -6, -7                    |
| XC3030A               | PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100           | -6, -7                    |
| XC3042A               | CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100 | -6, -7                    |
| XC3064A <sup>b</sup>  | PC84, PG132, PP132, PQ160, TQ144                     | -6, -7                    |
| XC3090A <sup>b</sup>  | CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176       | -6, -7                    |
| XC3020L               | PC84   | -8                        |
| XC3030L               | PC84, VQ64, VQ100                                    | -8                        |
| XC3042L               | PC84, TQ144, VQ100                                   | -8                        |
| XC3064L <sup>b</sup>  | PC84, TQ144  | -8                        |

| Device                | Packages   | Speed Grades             |
|-----------------------|--|--------------------------|
| XC3090L <sup>b</sup>  | PC84, TQ176  | -8                       |
| XC3120 <sup>a</sup>   | CB100, PC68, PC84, PG84, PQ100                         | -3, -4, -5               |
| XC3130 <sup>a</sup>   | PC44, PC68, PC84, PG84, PQ100, TQ100                   | -3, -4, -5               |
| XC3142 <sup>a</sup>   | CB100, PC84, PG84, PG132, PP132, PQ100, TQ100, TQ144   | -3, -4, -5               |
| XC3164 <sup>a b</sup> | PC84, PG132, PP132, PQ160                              | -3, -4, -5               |
| XC3190 <sup>a b</sup> | CB164, PC84, PG175, PP175, PQ160, PQ208                | -3, -4, -5               |
| XC3195 <sup>a b</sup> | CB164, PC84, PG175, PG223, PP175, PQ160, PQ208         | -3, -4, -5               |
| XC3120A               | CB100, PC68, PC84, PG84, PQ100                         | -1, -2, -3, -4, -5       |
| XC3130A               | PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100             | -1, -2, -3, -4, -5       |
| XC3142A               | CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100   | -1, -2, -3, -4, -5       |
| XC3164A <sup>b</sup>  | PC84, PG132, PP132, PQ160, TQ144                       | -1, -2, -3, -4, -5       |
| XC3190A <sup>b</sup>  | CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176         | -1, -2, -3, -4, -5       |
| XC3195A <sup>b</sup>  | CB164, PC84, PG175, PG223, PP175, PQ160, PQ208         | -1, -2, -3, -4, -5       |
| XC4003                | PC84, PG120, PQ100                                     | -4, -5, -6               |
| XC4005 <sup>b</sup>   | CB164, PC84, PG156, PQ100, PQ160, PQ208                | -3, -4, -5, -6, -6B, -10 |
| XC4006 <sup>b</sup>   | PC84, PG156, PQ160, PQ208                              | -3, -4, -5, -6           |
| XC4008 <sup>b</sup>   | MQ208, PC84, PG191, PQ160, PQ208                       | -3, -4, -5, -6           |
| XC4010 <sup>b</sup>   | BG225, CB196, MQ208, PC84, PG191, PQ160, PQ208         | -3, -4, -5, -6, -10      |
| XC4013 <sup>b</sup>   | BG225, CB228, MQ208, MQ240, PG223, PQ160, PQ208, PQ240 | -3, -4, -5, -6, -10      |
| XC4002A               | PC84, PG120, PQ100, VQ100                              | -5, -6                   |
| XC4003A               | CB100, PC84, PG120, PQ100, VQ100                       | -4, -5, -6, -10          |
| XC4004A <sup>b</sup>  | PC84, PG120, PQ160, TQ144                              | -5, -6                   |
| XC4005A <sup>b</sup>  | PC84, PG156, PQ160, PQ208, TQ144                       | -4, -5, -6               |
| XC4010D <sup>b</sup>  | BG225, PC84, PQ160, PQ208                              | -5, -6                   |
| XC4013D <sup>b</sup>  | BG225, PQ160, PQ208, PQ240                             | -5, -6                   |
| XC4003H               | PG191, PQ208   | -5, -6                   |
| XC4005H <sup>b</sup>  | MQ240, PG223, PQ240                                    | -5, -6                   |
| XC5202                | PC84, PG156, PQ100, TQ144, VQ100                       | -5, -6                   |

| Device               | Packages                                       | Speed Grades           |
|----------------------|--|------------------------|
| XC5204               | PC84, PG156, PQ100, PQ160, TQ144, VQ100        | -5, -6                 |
| XC5206 <sup>b</sup>  | PC84, PG191, PQ100, PQ160, PQ208, TQ144, VQ100 | -5, -6                 |
| XC5210 <sup>b</sup>  | BG225, PC84, PG223, PQ160, PQ208, PQ240, TQ144 | -5, -6                 |
| XC5215 <sup>b</sup>  | HQ304, PG299, PQ208, PQ240                     | -5, -6                 |
| XC7236A <sup>a</sup> | PC44   | -16, -20, -25          |
| XC7318 <sup>a</sup>  | PC44, PQ44                                     | -5, -7                 |
| XC7336 <sup>a</sup>  | PC44, PQ44                                     | -5, -7, -10, -12, -15  |
| XC7354 <sup>a</sup>  | PC44, PC68                                     | -7, -10, -12, -15      |
| XC7372 <sup>a</sup>  | PC68, PC84, PQ100                              | -7, -10, -12, -15      |
| XC7336Q <sup>a</sup> | PC44, PQ44, VQ44                               | -10, -12, -15          |
| XC73108 <sup>a</sup> | BG225, PC84, PG144, PQ100, PQ160               | -7, -10, -12, -15, -20 |
| XC73144 <sup>a</sup> | BG225, PQ160                                   | -7, -10, -12, -15      |

a. Not supported in X-BLOX.

b. Not supported in Base packages.





## Known Issues

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This chapter describes the known issues in this release.

### Software

This section lists the workarounds for the software. They are presented in the order that they occur in the design process.

### Configuration

#### **Do Not Remove Xilinx Security Keys During PRO Series Sessions**

Platform: PC  
Architecture: All  
Design Step: Software Configuration  
Reference Number: 4348

Do not remove the Xilinx security key while the PRO Series software is running. The PRO Series software frequently checks for the key.

### Design Entry

#### **SymGen -v Produces an Empty Symbol File**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 22401

Using the SymGen -v option creates an empty Viewlogic symbol. Please refer to the *Viewlogic Interface Guide* for instructions on how to create a symbol manually.

## PROgen May Create a Symbol with All Inputs

Platform: All  
Architecture: All  
Design Step: Design Entry  
Reference Number: 18655

If you use PROgen with the `-makesym` option to create a symbol for a design, it may only create inputs if XNF2WIR V5.x was used to create the WIR file. XNF2WIR currently writes pin records into the translated WIR file for each EXT record in the XNF file. It does not include the directionality of the pins, so PROgen assumes a direction of in.

## X-BLOX BUS\_IF Symbols Require the X-BLOX Bus Bounds to Start at Index 0

Platform: All  
Architecture: XC3000A/L and XC4000  
Design Step: Design Entry  
Reference Number: 15033

The X-BLOX BUS\_IF components translate X-BLOX-style buses to Viewlogic buses.

An example is the BUS\_IF08 that interfaces an 8-bit X-BLOX bus and an 8-bit Viewlogic bus. The BUS\_IF component is created such that the connecting X-BLOX bus must have a BOUNDS attribute of  $n-1:0$ . If any other BOUNDS attribute is present, the following error is issued when X-BLOX is run:

```
XBLOX: ERROR 20042: ELEMENT symbol instance has ELEM= 0
is out of the bounds (8: 1) of the bus to which it is
connected.
```

Use a CAST component to cast, or transpose, the X-BLOX bus so that it starts with index 0.

## Use Correct Syntax When Using "\*" in Parameterized Attributes

Platform: All  
Architecture: All  
Design Step: Design Entry  
Reference Number: 12902

The asterisk normally means “multiply” when used in parameterized attributes in PROcapture. If it is used as a wildcard in the Xilinx tools, you may receive the following warning message from WIR2XNF:

```
WARNING 27: Attribute LOC on instance XXX has no  
parametric value. Ignored.
```

If you use the asterisk symbol for a wildcard when passing parameterized attributes, you must enclose the entire value of the variable in quotation marks. This step ensures that the attribute is passed correctly.

Following is an example of the correct syntax:

```
@LOC1="CLB_R1C*"
```

## All X-BLOX Buses Must Be Labeled

Platform: All  
Architecture: XC3000, XC4000, XC5200  
Design Step: Simulation  
Reference Number: 16613

All X-BLOX buses must be labeled.

You must give all signals connected to X-BLOX bus pins a label. The following error occurs in XSimMake on unlabeled X-BLOX buses:

```
ERROR 11: Illegal unnamed net [$1N384] connected to  
XBLOX symbol on page  
mux_ctrl1.1  
1 Errors and 0 Warnings occurred during processing.  
ERROR 7: Command [xdraw -i outmux -o soutmux -a  
soutmux outmux.xgs  
soutmux/savexnf/outmux.xgs ] failed to execute  
properly.
```

If a bus connects the bus pins, the schematic entry tool issues an error message if the bus is unlabeled. However, if these pins are connected with nets, the tool allows the bus to be processed until this XDraw error occurs.

### **Only the First Instance of Components with \$ARRAY Attribute Can Be Labeled**

Platform: All  
Architecture: All  
Design Step: Design Entry  
Reference Number: 6409

Components with the \$ARRAY attribute can be labeled, but the specified label is only applied to the first instance; the remaining components of the array are not labeled. There is no way to specify different instance names on an \$ARRAY component. If you must have individual labels, do not use the \$ARRAY attribute; use individual components instead.

### **Check Fails Because of Windows Share Utility When Workview Plus Is Also Invoked**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 14112

When you run Windows V3.1 and Workview Plus, then open a DOS window to run XSimMake, Check fails with the following message:

```
vllib: Fatal: VLLIB Error 1004: Can't open message  
file vllib.vmb
```

This error is caused by a Windows utility called Share. Since PROcapture has opened the vllib.vmb file, Share makes Check's attempts to open it fail.

Avoid using Share when using Workview Plus.

## **Deleting Project Directory Causes PROflow to Abort**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 25879

Creating a project in PROflow and then deleting the project directory with the File Manager or through DOS can cause PROflow to quit unexpectedly after issuing an error message that says "Path not found."

Be sure to exit PROflow before deleting a project directory.

## **SYSPLT Variable Is Required**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 24868

The SYSPLT variable is still required.

If the SYSPLT variable is not set, or it points to a directory that does not have a DEVDES directory, PROcapture returns this error:

```
Internal ERROR: Plotting Disabled - no DEVDES dir  
found.
```

Set the SYSPLT variable to point to your \proser\standard directory.

## **PROcapture May Crash While Saving a Toolbar**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 24836

PROcapture may crash while saving a toolbar.

PROcapture requires write permission on the tool.lst file in the \proser\standard directory. If you attempt to save the toolbar while this file is unwritable, you will receive a general protection fault error.

## **Project Directory Path Must Be Less Than 42 Characters**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 21056

PROcapture can have problems with the Windows path limitations.

In setting up a project, PROcapture creates several levels of directories in the project directory. If your path is close to the limit in Windows (around 65 characters), you may receive an “Unable to generate directory” message. Make sure your project directory path is less than 42 characters.

## **Do Not Change Project in PROcapture While PROflow Is Running**

Platform: PC  
Architecture: All  
Design Step: Design Entry  
Reference Number: 21881

When using PROflow, set the project under the Design Entry button. If you change the project in PROcapture while PROflow is running, PROflow does not recognize the change. If PROflow is not running, you can set the project in PROcapture.

## **CE Function of FJKSRE and FJKRSE Has Changed**

Platform: All  
Architecture: XC2000, XC3000, XC4000  
Design Step: Design Entry  
Reference Number: 20288

The CE function of the FJKSRE and the FJKRSE macros has changed.

There was an error in these two macros. The SET and RESET pins were dependent on CE. However, the truth table in the *Xilinx Libraries Guide* showed that they were independent. Now these two macros match the truth table.

## **Do Not Use PRO Series Executables from Viewlogic and Xilinx at the Same Time**

Platform: PC

Architecture: All

Design Step: Design Entry

Reference Number: 26338

Using PRO Series executables from both Viewlogic and Xilinx can cause licensing problems.

Viewlogic builds special versions of the PRO Series tools for use with the Xilinx programmable key. If you attempt to use executables from both Viewlogic and Xilinx at the same time, you may experience licensing problems. Using the Viewlogic key in conjunction with a Xilinx key programmed for Viewlogic could also result in licensing errors.

The following alternatives are supported by Version 6.0:

- You can use both `check.exe` and `procaptu.exe` from Viewlogic, and use the Viewlogic key with the Xilinx key programmed not for PRO Series but for *XACTstep*.
- You can use both `check.exe` and `procaptu.exe` from Xilinx, and use only the Xilinx key programmed for PRO Series and *XACTstep*.

To avoid licensing problems, follow these instructions:

- Always install the Viewlogic Stand-alone PRO Series package to a clean directory. The DS-391 package, Viewlogic Interface and Libraries, can be safely written to an existing Viewlogic installation.
- Do not attach a Viewlogic key to a Xilinx key programmed for Viewlogic.

## **XC4000D Parts Do Not Appear in PROsim's Select\_Part Menu**

Platform: PC  
Architecture: XC4000  
Design Step: Design Entry  
Reference Number: 26415

XC4000D parts do not appear in PROsim's Select\_Part menu.

When you select the PROsim → Functional Simulation → Select\_Part command in PROflow, no XC4000D parts appear. Select the equivalent part, either XC4010 or XC4013.

## **Translation to XNF**

### **WIR2XNF Fails to Update WIR Files**

Platform: PC  
Architecture: All  
Design Step: Translation to XNF  
Reference Number: 25921

WIR2XNF may incorrectly report that WIR files are out of date, which respect to either schematic or symbol files. This occurs because, in comparing the date stamps of these files, WIR2XNF does not properly consider the year number.

When this occurs, WIR2XNF will call the Viewlogic CHECK program to update the WIR file, and then erroneously report that CHECK failed:

```
CHECK - V4.09; Workview 4.1.3 062292, 3000 Series
c Copyright 1985,1992 by Viewlogic Systems, Inc.
Checking primary:JCOUNT.1 ...
0 error(s) and 0 warning(s) in project primary:JCOUNT.
Warning -Unable to update WIR file jcount.1.
(Execution of the standalone CHECK program
failed).
Warning -The schematic for jcount.1(C:\JCOUNT\
SCH\JCOUNT.1)is newer than the WIR file
C:\JCOUNT\WIR\JCOUNT.1.
Components written to file2.xnf.
0 Errors and 0 warnings occurred during processing.
```



However, as shown in the above example, CHECK completes with no warnings or errors, and the WIR file actually *does* get updated properly (the date stamp problem prevents WIR2XNF from seeing that the update has happened).

WIR2XNF will read the updated WIR file correctly, and these warnings can be safely ignored.

### **WIR2XNF Does Not Correctly Translate INIT Attribute for XC3000A/L and XC3100A Designs Using X-BLOX PROMs**

Platform: All

Architecture: XC3000A/L, XC3100A

Design Step: Translation to XNF

Reference Number: 18961

WIR2XNF fails to correctly translate the user parameter INIT=x on X-BLOX PROM symbols, so it generates an error in XNFPrep.

Instead of using the INIT attribute, use a MEM file. Set the MEMFILE attribute on the X-BLOX PROM symbol to point to your MEM file.

### **WIR2XNF May Not Be Authorized to Run with Powerview**

Platform: Workstations

Architecture: All

Design Step: Translation to XNF

Reference Number: 16768

If you are using Powerview and running WIR2XNF, you may encounter this message:

```
SCC: required license not found
For product GENERIC
Error 4
Internal initialization error....
```

Run the Check program with the -p option on the design from the system prompt. This step updates all the WIR files and ensures that they are free of errors. If errors are found, they must be fixed before running WIR2XNF again.

Check the license.wv file for PRODUCT 2. PRODUCT 2 must be authorized in order to run WIR2XNF and XNF2WIR. However, if

PRODUCT 2 is present, it may still not be authorized in the MAGIC\_NUMBER at the end of the file. PRODUCT 2 is Workview V4.1, and Viewlogic may not automatically authorize Workview for Powerview customers.

If PRODUCT 2 is present, but you still receive this error, call Viewlogic to find out if PRODUCT 2 is authorized by the MAGIC\_NUMBER in your license.wv file.

For Powerview V5.2 users, make sure the license\_server line appears and is set in both the powerview.ini and workview.ini files found in /workview/standard.

## Simulation File Creation

### Designs with Dashes in Their Names Are Not Processed

Platform: All

Architecture: All

Design Step: Simulation File Creation

Reference Number: 18661

When XSimMake creates a simulation model for a design, it creates an *sdesign* directory in which it stores all associated files. In order to access this directory, it adds a library to the viewdraw.ini file with the name *sdesign*.

If the design name contains a dash, the library also contains a dash; for example, if the design name is “de-sign,” the line in the viewdraw.ini file is the following:

```
DIR [w] .\sde-sign (sde-sign)
```

The viewdraw.ini reader cannot read any libraries that contain dashes in them and issues the following error:

```
Error - Directory specification error.  
<DIR [w] .sde-sign (sde-sign)>
```

Renaming the top-level design schematic so that dashes are not used allows the viewdraw.ini reader to read libraries with dashes in them.

This problem has been forwarded to Viewlogic.

## **XSimMake Fails When Project Is Located on a Novell Drive**

Platform: PC  
Architecture: All  
Design Step: Simulation File Creation  
Reference Number: 18674

XSimMake may fail with a file-sharing error when attempting to open the *design.xfw* file.

Moving the design directory to a local drive resolves this problem.

## **VSM Fails with Pre-Unified Libraries When XNF2WIR Inserts Startup Symbol in Translated WIR File**

Platform: All  
Architecture: XC4000  
Design Step: Simulation File Creation  
Reference Number: 18030

When XNF2WIR is run on an XC4000 design that uses the STARTUP component, it creates a reference to it in the resulting WIR file. If you created the design using libraries that pre-dated the Unified Libraries, VSM terminates with the following error:

```
ER Error - Could not find WIR file startup.1.
```

Adding a reference to the SHM4000 library in the viewdraw.ini file ensures that VSM can find the startup.1 WIR file. You can find the SHM4000 library in the \proser directory.

## **VSM Does Not Support -W Option**

Platform: Workstation  
Architecture: All  
Design Step: Simulation File Creation  
Reference Number: 19268

When creating board-level simulation files, VSM is typically run with the -w option to create a “flattened” WIR file. In its newest release, VSM does not support this option.

Run a previous version of VSM. This problem has been forwarded to Viewlogic.

## **XSimMake Appears to Hang with No Messages**

Platform: All  
Architecture: All  
Design Step: Simulation File Creation  
Reference Number: 10999

In a few instances, XSimMake may appear to stop processing and issuing any messages. This behavior occurs when XSimMake interfaces with Viewlogic routines, and occasionally one of those routines waits for some additional input. However, no messages are issued to indicate that the program is still running and is waiting for further input.

If XSimMake appears to be taking an abnormally long time to run and there is no disk access taking place, halt the program. Run XSimMake with the -v option, which writes all messages to the screen.

## **XSimMake Does Not Support Designs with CLB or IOB Primitives**

Platform: All  
Architecture: XC3100/A, XC3000/A/L, XC2000/L  
Design Step: Simulation File Creation  
Reference Number: 14713

Neither the functional flow nor the timing flow of XSimMake supports designs containing CLB or IOB primitives. For instructions on how to simulate these designs, see the *Viewlogic Interface Guide*.

## **Simulation**

### **XDraw Interprets a Design Schematic as Corrupted**

Platform: Workstation  
Architecture: All  
Design Step: Simulation  
Reference Number: 26570

XDraw issues the following error when you run XSimMake to functionally simulate a design created with Powerview V5.3.2, and when the version of the schematic is 5.1. XDraw interprets the schematic as corrupted.

```
Could not access Sheet 1 of SCHEMATIC <top>.
```

To verify this error, look at the xdraw.out file. The following is an example of what XDraw reports:

```
File <top> has been corrupted.  
=====> V 51  
Line 1 *** Error #35 ***  
primary:<top>.1 read
```

XDraw was compiled with older versions of the Viewlogic tool libraries, which do not recognize version 5.1 schematics.

Because the Powerview tools can use schematics created with previous versions, you can change the V51 line in the schematic and symbol netlist files to V51 either manually or by using a utility that is available on the Xilinx BBS and Internet FTP server. The advantage of the utility method is that once it is installed, the netlists are automatically converted as needed.

#### Utility Method

Follow these steps to use the CVT50 converter.

1. Obtain the two required files, cvt50 and xsimmake.xfw, from one of the following services:

Xilinx BBS: 408-559-9327 (SWHELP area)

or

FTP server: ftp.xilinx.com (pub/utilities/swhelp directory)

2. Copy cvt50 to ~xact/bin/sparc.
3. Copy ~xact/data/xsimmake.xfw to a backup location, for example, xsimmake.xfw.old.
4. Copy xsimmake.xfw to ~xact/data.

The simulation netlist creation utility, XSimMake, now calls the CVT50 converter automatically. The converter checks a netlist's version number and changes it, if needed, so that XDraw will work properly.

#### Manual Method

Use these instructions to modify your files manually.

1. Copy all design schematics and symbols (found in project\_dir/sch and project\_dir/sym, respectively) to a backup location.

2. Using a text editor, modify all schematic and symbol netlists — for example, mysch.1 and mysym.1 — using the following example as a guide.

Change the following:

```
V 51  
K 165102488100 mytest  
Y 0
```

to this:

```
v 50  
K 165102488100 mytest  
Y 0
```

Then, to ensure that the changes affect future processing, remove all the files located in the wir subdirectory, and run the Viewlogic Check program to create them, for example:

```
check -p mytest
```

## Startup Symbol Does Not Functionally Simulate

Platform: All

Architecture: XC4000, XC5200

Design Step: Simulation

Reference Number: 18894

The Startup symbol does not have a simulation model. If you perform a functional simulation on a design containing a net connected to the GSR pin or the GTS pin on the Startup symbol and you assert the nets connected to the pins, neither a global Set/Reset nor a global tristate occurs. To assert a GTS or GSR for functional simulation, you can force a value directly to the GSR or GTS nodes, or you can label the net connected to the Startup symbol pin as “GSR” or “GTS” accordingly, and then force a value on the net.

Timing simulation for the Startup symbol works correctly, so the workarounds just described are not necessary.

## **Simulation Takes Much Longer with the Unified Libraries**

Platform: All

Architecture: XC2000, XC3000, XC4000

Design Step: Simulation

Reference Number: 18672

The libraries pre-dating the Unified Libraries used only Viewlogic builtin primitives to model the various flip-flops and therefore did not fully model the behavior of Xilinx devices. To allow you to use the flip-flops fully, VHDL models were written to enhance the setup and hold checks.

The Viewlogic simulators take much more time to load and evaluate the VHDL models when compared to the builtin primitives, so simulation times have increased significantly.

To resolve this problem, a set of fast libraries has been created. They are similar to the libraries pre-dating the Unified Libraries and can be used in place of the libraries that use the VHDL models. These libraries speed up simulation run times significantly but do not have the added accuracy of the libraries with VHDL models. The fast libraries are XC2000f, XC3000f, and XC4000f.

## **Use VCC and GND Components to Tie Signals High and Low in Schematics**

Platform: All

Architecture: All

Design Step: Simulation

Reference Number: 11624

The FLOATVAL attribute was once used to designate a schematic net as a net tied to power or ground for simulation purposes. With current software, PROsim does not recognize a FLOATVAL attribute that you add to your schematic.

The correct way to tie a net to power or ground is to attach a component called VCC or GND. These components are part of the Xilinx libraries. Alternatively, you can explicitly force the net High or Low during simulation.

## **PROsim May Issue Erroneous Error About Multiple Conflicting FLOATVAL Attributes**

Platform: PC  
Architecture: All  
Design Step: Simulation  
Reference Number: 4788

During unit delay simulation, PROsim sometimes issues an error statement about multiple conflicting FLOATVAL attributes, although viewing the schematic shows no net with the FLOATVAL attribute.

Flip-flops in the Xilinx library may have several different control pins, such as a Clock Enable pin, Set or Reset pin, and so forth. The simulation models for these components assign FLOATVAL attributes to these control pins, so that if left unconnected, they are in a known state. Clock Enable pins are active by default (FLOATVAL=1); Set or Reset pins are inactive by default (FLOATVAL=0). If you connect the two pins to the same signal, PROsim issues the following error:

```
ERROR: Multiple conflicting FLOATVAL attributes on net  
net_name.
```

If you deliberately connected the two pins to the same net, ignore this message. If not, check your schematic for inadvertent shorts or misconnections.

## **FLOATVAL Value Does Not Return After Force and Release**

Platform: All  
Architecture: All  
Design Step: Simulation  
Reference Number: 4879

A node that has a FLOATVAL attribute does not assume its FLOATVAL value after it has been forced to a value and released.

The FLOATVAL attribute is used only to initialize values on nodes.

This issue has been forwarded to Viewlogic.



## **Tools → Link to PROsim Command Creates Invalid VSM File**

Platform: PC  
Architecture: All  
Design Step: Simulation  
Reference Number: 25424

Using the Tools → Link to PROsim in PROcapture may create an invalid VSM file.

The Link to PROsim command in PROcapture exports a VSM file, but if the design contains X-BLOX or Xilinx ABEL modules, these modules are not correctly processed. Use PROflow to perform functional and timing simulation of your designs.

## **Errors Appear in XSimMake OUT File for X-BLOX Designs**

Platform: All  
Architecture: All  
Design Step: Simulation  
Reference Number: 25038

The XSimMake functional flow always reports errors in the OUT file when simulating a design with X-BLOX modules.

In the xsimmake.out file, you might see the following errors:

```
.  
.   
.   
  
Error: Could not load schematic sheet -  
smult8:bsm38.1  
Searching for SCHEMATIC smult8:bsm55.1 ...  
Error: Could not load schematic sheet -  
smult8:bsm55.1  
Searching for SCHEMATIC smult8:xsyscaak.1 ...  
smult8:xsyscaak.1 read  
Checking smult8:xsyscaak.1 ...  
0 errors and 0 warnings on schematic  
smult8:xsyscaak.1.  
Searching for SCHEMATIC xsyscaak.2 ...  
Searching for SCHEMATIC xsyscaag.2 ...  
Searching for SCHEMATIC smult8.2 ...
```

Total # of Schematics checked - 18

Total errors - 0 and warnings - 0

These errors indicate that the Check program cannot find the schematics to match the WIR files that represent the X-BLOX modules. You can safely ignore these errors because no schematics are generated for the X-BLOX components. The schematics are not required to simulate the design correctly.

## Changing PROwave Time Units Does Not Work

Platform: PC

Architecture: All

Design Step: Simulation

Reference Number: 25542

Changing the time units in PROwave does not work correctly.

If you select Waveform → Display Params → Tunits → Size in PROwave and select milliseconds or microseconds as the time units, PROwave draws the display incorrectly. Select View → Refresh to update the screen. PROwave displays the new time units only until the screen is redrawn, then it defaults to nanoseconds again. For example, if you set the data to milliseconds, then change the actual window size, it reverts to nanoseconds.

## GEN File Created by XChecker May Cause ViewTrace to Crash

Platform: Workstations

Architecture: All

Design Step: Simulation

Reference Number: 26293, 26280

Using a GEN file created by XChecker may cause ViewTrace to crash.

If you create a GEN file from XChecker using the Export -v command, this file may cause ViewTrace 5.x to crash with this error message:

```
*** Fatal error encountered ***  
  
vtrace: Fatal 500: INTERNAL VIEWtrace ERROR -- in  
"file.c" at line 772.
```

The only known workaround is to use PROwave, which does not experience this problem.

### **Apply Stimulus to IBUF Input When X-BLOX Merges IOB Flip-Flops**

Platform: All

Architecture: XC2000, XC3000, XC4000

Design Step: Simulation

Reference Number: 20377

Incorrect timing simulation results can occur if X-BLOX has merged IOB flip-flops, and the stimulus is not applied to the input of the IBUF.

To optimize designs, X-BLOX attempts to move DFFs into IFD whenever possible. However, XSimMake does not modify the schematics to reflect the change. If the stimulus is applied to the net on the output of the IBUF, the IFD does not see this stimulus in timing simulation, and you see an X on the output of this flip-flop. Yet this procedure works well in functional simulation.

This problem arises because the timing WIR files are derived in part from the LCA file, and the modeling of this IFD implies an IBUF as part of the IFD, so the net to which you are applying the stimulus no longer exists.

In this situation, apply the stimulus to the net on the input of the IBUF.

### **Schematic Problems May Cause XDraw to Crash**

Platform: All

Architecture: All

Design Step: Functional Simulation

Reference Number: 18778, 18503

Check sometimes crashes after running XDraw. If Check crashes your PC or issues a segmentation fault on the workstation after running XDraw, there could be a problem in the original schematic that Check missed. To find this problem, look in the *sdesign/wir* directory to see at which file Check stopped. This file is usually 0 bytes. Re-examine the *sdesign.x* that corresponds to the WIR file. Usually this schematic will have a round junction in an location that is not normal. This problem generally seems to be related to nets that overlap and have

identical end points. The round junction appears where only two net leave the junction; one usually overlaps another.

Go back to the original schematic, delete all the nets, buses, and components in the vicinity of the problem, then re-enter them. This step should clear up the problem.

### **Powerview Does Not Back-Annotate Schematic During Simulation**

Platform: Workstations  
Architecture: XC7000  
Design Step: Timing Simulation  
Reference Number: 25723

If you use XSimMake to prepare the timing simulation network for an EPLD design using XACT V5.2 and you are using Powerview V5.2, ViewDraw may not display any simulation values on your schematic. This problem occurs because XSimMake uses the temporary project name "XSIMMAKE" when creating the VSM file. ViewDraw V5.2 does not display simulation values if the schematic name does not match the project name in the VSM file.

To restore visibility, save a duplicate copy of your schematic under the name "XSIMMAKE" and view this schematic during simulation.

This issue has been forwarded to Viewlogic.

### **XDM.PRO File May Cause Unrecognized Part Type Error in XSimMake**

Platform: PC  
Architecture: XC7000  
Design Step: Functional Simulation  
Reference Number: 25998

If you use PROflow to prepare the functional simulation network for an EPLD design, the XEMake program may produce a fatal error saying "unrecognized part type." You may receive this message if you have an xdm.pro file in your project directory from a prior release.

To eliminate this error, delete the xdm.pro file from your project directory.

## Unrecognized Keywords in Viewdraw.ini File Cause XDraw to Fail

Platform: All  
Architecture: All  
Design Step: Simulation  
Reference Number: 26274

XDraw does not correctly handle Viewlogic keywords in the viewdraw.ini file that it does not recognize.

For instance, the FULL\_VHDL\_CHECKS keyword enables or disables the DRC software that verifies a VHDL module so you do not have to run the Check program. However, XDraw rejects this keyword and causes XSimMake to fail even though the keyword is valid. Removing this keyword from the viewdraw.ini file prevents the error and allows XSimMake to complete successfully.

## Documentation

This section lists the corrections to the documentation.

### Viewlogic Interface Guide

This section lists the corrections to the *Viewlogic Interface Guide*.

#### Do Not Use SHM4000 Library with Unified Libraries Designs

Platform: All  
Architecture: All  
Design Step: Design Entry  
Reference Number: 10814

Do not place the SHM4000 library in the search path of designs created with the Unified Libraries.

Pages 2-13, 2-14, 2-22, and 2-23 of the *Viewlogic Interface Guide* recommend the use of the SHM4000 library in conjunction with the Unified Libraries. This recommendation is incorrect. If you use an element from the SHM4000 library while designing with the Unified Libraries, you will receive this error:

```
XNFPREP: ERROR 3516:
```

The design file contains a mixture of symbols from the new Unified Libraries (library version 2) and the older family-specific libraries.

The majority of symbols in the design are from the new Unified Libraries; however, the following symbols from the old family-specific libraries were found in the design:

```
Symbol Type = TIMESPEC ; Symbol Name = $1I468 ;  
Output Signal =
```

Symbols from the two versions of libraries cannot be combined in the same design. Please ensure that all schematic symbols are taken from the same library version. If the inconsistent symbols are generated by a synthesis program, there should be an option in that program that controls the library version used.

Remove the SHM4000 library from the search path of all designs created with the Unified Libraries.

## **SHM4000 Library Can Be Used with XC3000A/L and XC3100A Designs**

Platform: All

Architecture: XC3000A/L, XC3100A

Design Step: Design Entry

Reference Number: 10815

The SHM4000 library can be used with the XC3000A/L and XC3100A families.

Page 8-7 of the *Viewlogic Interface Guide* indicates that the SHM4000 library must be used in designs created with libraries pre-dating the Unified Libraries. But the manual then adds the following note:

**Note:** In general, add the SHM4000 library to your viewdraw.ini file for XC4000 designs. It contains symbols that prevent you from receiving warnings from XNF2WIR.

This note only applies to designs created with libraries pre-dating the Unified Libraries.

Also, the SHM4000 library contains elements, such as BIBUF, CAST, and TIMESPEC symbols, that can be used in XC3000A/L and XC3100A designs, since these families are supported by PPR and X-BLOX.

## Functional Simulation Dialog Box Illustration Is Incorrect

Platform: All  
Architecture: All  
Design Step: Functional Simulation  
Reference Number: 10816

Because of software changes that occurred after the *Viewlogic Interface Guide* went to print, the illustration of the Functional Simulation dialog box on page 4-3 is incorrect. A Select Part field has been added to this dialog box. The correct Functional Simulation dialog box is shown in Figure 4-1.

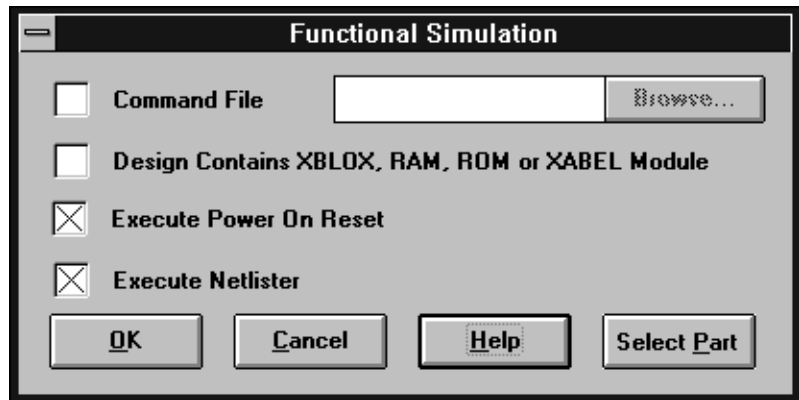


Figure 4-1 Functional Simulation Dialog Box

## Figure and Table Titles are Incorrect

Platform: All  
Architecture: All  
Design Step: Simulation  
Reference Number: 10834

The figures and tables on the following pages are numbered incorrectly: 7-25, 8-2, 8-5, 8-8, 8-15, 8-17, 8-18, 8-19, 8-21, 8-22, 8-24, 8-25, 8-30, 8-37, 8-39, 8-48, 8-49. This numbering will be corrected in the next version of the manual.

## Viewlogic Tutorials

This section lists the corrections to the *Viewlogic Tutorials* manual.

### Tutorial Solution Directories Are Outdated

Platform: All  
Architecture: All  
Design Step: Simulation  
Reference Number: 10835

Because of path length problems in the directory structure created by the Design Manager, the XC3000A and XC7000 solution directories have been moved. Pages 2-2, 3-2, and 4-2 of the *Viewlogic Tutorials* manual lists these directories as follows.

...\tutorial\vwlogic\procalc\calc3ka\soln\_3ka

The new path to the solution directories is the following:

...\tutorial\vwlogic\pcalc3ka.sol

## Viewlogic Interface Guide/Viewlogic Tutorials

This section lists the corrections that affect both the *Viewlogic Interface Guide* and the *Viewlogic Tutorials* manual.

### Design Entry Dialog Box Illustrations Are Incorrect

Platform: All  
Architecture: All  
Design Step: Design Entry  
Reference Number: 10817

Because of software changes that occurred after the documentation went to print, the illustrations of the Design Entry dialog box in the *Viewlogic Interface Guide* and the *Viewlogic Tutorials* manual are incorrect. These pictures occur on pages 2-15, 3-2, 3-3, 3-62, and 3-67 of the *Viewlogic Interface Guide* and on page 1-14 of the *Viewlogic Tutorials* manual. A Library List Editor field has been added to the dialog box. The correct Design Entry dialog box is shown in Figure 4-2.



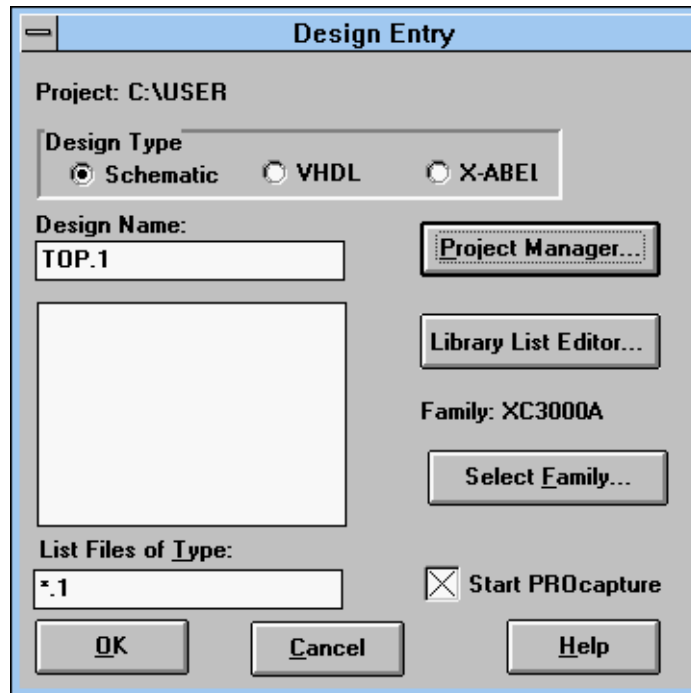


Figure 4-2 Design Entry Dialog Box



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