



Release Document

***XACTstep* Version 5.2/6.0**
Mentor Graphics

October 1995

Read This Before Installation

Installing Online Documentation

Starting with the 5.2/6.0 release, online documentation is now available on the Sun and HP workstations.

Installing Online Documentation on a Sun Workstation

To use online documentation, you must install the Acrobat reader and the online documents on your workstation.

Installing the Reader and Documents

Version 1.0 of the Acrobat reader is included on the XACTstep Sun 5.2 CD-ROM disk. To install the Acrobat reader, follow the instructions on page 4-4 of the *Getting Started & Installation Guide*.

Because the online documents are in tar format, you must use the XACTstep 5.2 installation program to install the online documents on your workstation. Refer to the Sun4 instructions on page 3-2 of the *Getting Started & Installation Guide*.

Opening Documents with Acrobat Reader — Sun Workstation Installations

To access the AcroRead program from the command line, follow these instructions:

1. Include the path to the /AcroRead_1.0/bin directory in the \$path variable of your configuration file,
2. At the command line, type the following to invoke the Acrobat reader:

```
acroread
```

The Open file dialog box of the Acrobat reader is displayed.

3. Specify the following path in the Filter box of the Open file dialog box to view Xilinx Online Documents:

```
/xact_dir/online/online/*.pdf
```

To view Xilinx Application Information, specify the following path:

```
/xact_dir/online/onlinedb/*.pdf
```

4. Select the document you want from the displayed list of .pdf files.

Installing Online Documentation on a HP Workstation

To use online documentation, you must install the Acrobat reader and, optionally, the online documents on your workstation.

Installing the Reader and Documents

Version 2.1 of the Acrobat reader is available on HP workstations on a separate enclosed Acrobat CD-ROM disk also provided by Xilinx. Use the instructions outlined in this section to install the Acrobat software on an HP workstation.

Installation of the Acrobat reader requires the HP-UX 9.05 operating system, the HP-VUE window manager, and 12 MB of disk space. You do not have to install the online documents to your hard disk, but if you choose to do so, you will need 52 MB of disk space.

1. Insert the CD-ROM disk into the CD-ROM drive.
2. Mount the CD-ROM drive. You need system administrator privileges to complete this step.
3. Invoke the Acrobat Installation program as follows:

```
/cdrom_dir/acrobat/unix/install
```

By default, after you have installed the desired products to your HP workstation, the installation program copies the Acrobat reader to the /usr/AcroRead directory. Xilinx recommends that you install the reader to /xact_dir/doc/AcroRead. You must include the AcroRead/bin directory in your path.

For more information, print the “Introducing Adobe Acrobat Reader 2.1” file located in `/cdrom_dir/acrobat/unix/instguid.txt`.

Note: If you want to install the document files on your workstation, copy the `/cdrom_dir/onlindb` and `/cdrom_dir/online` directory trees from the XACTstep Version 5.2 CD-ROM to your disk. For example:

```
cp -Rp /cdrom_dir/onlindb /xact_dir/doc/onlindb ↵
cp -Rp /cdrom_dir/online /xact_dir/doc/online ↵
chmod -R u+w xact_dir/doc↵
```

Opening Documents with Acrobat Reader — HP Workstation Installations

To view documents on an HP workstation, follow the instructions outlined in this section. For additional information refer to the “Viewing Documents with Acrobat Reader” section on page 4-7 of the *Getting Started & Installation Guide*.

You can either start the reader first and then decide what type of documents you want to view, or you can open the type of documents you want to view at the same time you load the reader.

To start the reader without specifying any documents, follow these instructions:

1. Ensure that the Acrobat Reader `AcroRead/bin` directory is in your path.
2. To start the reader, type the following:
acroread
3. Specify one of the following paths corresponding to the type of documents you wish to view:

To view Xilinx Online Documents, open the file:

```
/cdrom_dir/online/linkpage.pdf
```

or

```
/xact_dir/online/linkpage.pdf
```

To view Xilinx Application Information, open the file:

```
/cdrom_dir/onlindb/dblink.pdf
```

or

```
/xact_dir/onlindb/dblink.pdf
```

To specify the type of documents you wish to view at the time you invoke the reader, include the path you want after the `acoread` command as follows:

To view Xilinx Online Documents, use the command:

```
acoread /cdrom_dir/online/linkpage.pdf &
```

or

```
acoread /xact_dir/online/linkpage.pdf &
```

To view Xilinx Application Information, use the command:

```
acoread /cdrom_dir/onlindb/dblink.pdf &
```

or

```
acoread /xact_dir/onlindb/dblink.pdf &
```

Versions and Compatibility

The following master table indicates Xilinx core software with the current version numbers.

Software Versions

Program	Windows Version	DOS Version	Workstation Version
APR	5.2	5.2	5.2
APRLOOP	5.2	5.2	5.2
CstCvt	5.2	5.2	5.2
Design Manager	6.0	N/A	N/A
Floorplanner	6.0	N/A	5.2
Flow Engine	6.0	N/A	N/A
Hardware Debugger	6.0	N/A	N/A
HM2RPM	5.2	5.2	5.2
LCA2XNF	5.2	5.2	5.2
MakeBits	5.2	5.2	5.2
MakePROM	5.2	5.2	5.2
MAP2LCA	5.2	5.2	5.2
MemGen	5.2	5.2	5.2
PPR	5.2	5.2	5.2
PROM File Formatter	6.0	N/A	N/A
Report Browser	6.0	N/A	N/A
SymGen	5.2	5.2	5.2
Timing Analyzer	6.0	N/A	N/A

Program	Windows Version	DOS Version	Workstation Version
XACT	5.2	5.2	5.2
XBLOX	5.2	5.2	5.2
XChecker	5.2	5.2	5.2
XCK88	N/A	5.2	N/A
XDE	5.2	5.2	5.2
XDelay	5.2	5.2	5.2
XDM	N/A	N/A	5.2
xdm	5.2	5.2	5.2
XEMake	N/A	N/A	5.2
XEMake6	6.0	N/A	N/A
XKey	5.2	5.2	N/A
XMake	5.2	5.2	5.2
XNFBA	5.2	5.2	5.2
XNFCvt	5.2	5.2	5.2
XNFMAP	5.2	5.2	5.2
XNFMerge	5.2	5.2	5.2
XNFPrep	5.2	5.2	5.2
XPP	5.2	5.2	5.2
XPrint	5.2	5.2	5.2
XSimMake	5.2	5.2	5.2

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Introduction

Welcome to the Mentor Graphics Interface from Xilinx!

Xilinx software products have prefixes to designate the type of products you receive.

- DS = Development System (new system)
- DX = Development System Upgrade (upgrade to current system)
- SC = Support Contract (update for current system)
- SR = Support Reinstatement (update for non-current system)

The labels on the box indicate the product you have received.

This release note supports the following products.

- Mentor Graphics Interface (DS-344)
- Mentor Graphics Standard Development System Package (DS-MN8-STD)

Contents

The Development System (DS) product you received contains software, documentation, and/or hardware. New DS Standard package contain hardware, software, and documentation. Interface and Update products have software and documentation only.

Hardware¹

The hardware consists of the following items.

- XChecker Download and Readback Cable Set

1. Included in DS and SR packages only.

Software

Xilinx software for all platforms is provided on CD-ROM. It consists of the following.

- Installation Program
- FPGA Core Implementation Tools (DS-502)
- Mentor Graphics Interface and Libraries (DS-344)
- XEPLD Translator Core Tools (DS-550)
- X-BLOX (DS-380)

Documentation

The following documentation is available in print for Mentor Graphics products.

- *Getting Started & Installation Guide*
- *Additional Products & Services Packet*
- *Mentor Graphics Interface/Tutorial Guide*¹

Online Documentation

The following online documentation is included with your Mentor Graphics products.

- *Libraries Guide*
- *Libraries Supplement Guide*
- *X-BLOX Reference/User Guide*
- *Floorplanner Reference/User Guide*
- *Development System User Guide*
- *Development System Reference Guide, Vols 1-3*
- *Hardware & Peripherals User Guide*
- *XEPLD Reference Guide*

1. Included in DS and SR products only.

- *XEPLD Design Guide*
- *XEPLD Schematic Design Guide*

Note: Xilinx Core FPGA and EPLD documentation for Sun and PC platforms is available online via CD-ROM. Some documentation for product updates and for other workstation platforms is included on the basis of product configuration.

Selected Xilinx manuals are available in printed form. See the “Documentation Order Form” in the *Additional Products & Services Packet*.

Maintenance and Support

This product comes with free technical and product information telephone support (toll-free in the U.S. and Canada). You can also fax and e-mail your questions. See the “Xilinx Customer Support Information” chapter of this release note for offices and phone numbers.

This product comes with one year of maintenance; you will receive all software and documentation updates automatically during that time. You will receive a notice at the end of the year giving instructions on how to renew your maintenance contract.

Features in This Release

This section of the release note provides information on the new features in the current software release.

Mentor Graphics A.x-F Support

XACTstep 5.2 supports Mentor Graphics version A.x-F. It is not compatible with pre-A.x-F versions of the Mentor Graphics software. However, you can load a design created with the 8.2 version of Mentor Graphics software into the A.x-F version of Design Architect. After loading your design, check and save it before translating to an XNF file.

XC5200 Support

Library Support for XC5200

New schematic and simulation libraries are available to support the XC5200 device family. For more information on this family, see *The Programmable Logic Data Book*.

XNF Version 6 Support

This version of the XNF file supports the new XC5200 Xilinx product family.

Design Conversion To New Family

You can translate your unified library designs to a new device family. For example, you can translate an XC4000 design created with unified library components to an XC5200 design. Your schematic looks the same, however, the component references point to the

library for the new device family. Components that are specific to a particular device architecture, such as an XC4000 OSC4, are not converted and must be manually replaced with components in the new library using Design Architect.

To convert your design to a new device family, follow these steps:

1. Start Design Architect by selecting the PLD_DA icon in the Design Manager and double-clicking the left mouse button.
2. Deselect all schematic windows in Design Architect.
3. Move the cursor outside the schematic windows and use the right mouse button to display the Session popup menu.
4. Select **Convert Design** from the Session menu.

The Convert Design to New Technology dialog box appears.

5. Fill in the dialog box with the appropriate information as follows:

- Design Name or List File Name

You can either convert one component at a time or list all your design components in an ASCII list file with one design entry per line. The following is an example of a list file:

```
test
design_a
/home/rickh/projects/projA/mux
$CUSTOMERS/company_x/mike_sv16
```

The convert program searches for designs that are not specified with a full pathname (such as test and design_a in this example) in the \$MGC_WD directory or, if the \$MGC_WD variable is not set, in the directory in which you started PLD_DA.

- Verbose Mode Switch

This is the default option and can be turned off. Use this option to monitor the conversion process. If you turn this option off, the schematic window does not change during the conversion process. To increase the speed of the conversion process, turn off the Verbose option.

- Check & Save Switch

Use this option to automatically check, save, and close each design sheet after it is converted. By default, this option is turned off. If you do not select this option, you must manually check, save, and close each sheet at the end of the conversion process.

- From Technology

Use this option to specify the family of the components in your design. For example, if your design currently targets an XC3000 device, enter xc3000.

- To Technology

Use this option to specify the new device family, for example xc4000.

- Log File Name

At the end of the conversion process, a log file is created that includes information on the number of instances per sheet that were replaced as well as the number of instances that were not changed. If there are any changes in the check sheet result after each sheet conversion, this information is also included in the log file. Use this option to specify a filename for the log file. If you do not select a name, the log file is *design.log*. If you specify a group of designs in a list file, the log file is named *list_filename.log*.

- Bell Ring

This option causes the convert program to beep when a component instance is ignored and entered in the log file. You can turn this option off.

6. Select **OK** to start the conversion process.

7. A transcript of the conversion process is saved in *design.transcript*.

Enhancements/Modifications/Bug Fixes to Programs

You can now add the INIT property to flip-flops in XC7000 designs by performing the following steps:

1. Open your schematic in Design Architect.

2. Select **Setup** → **Property Owner/Type** → **Property Owner**.

The Set Property Owner dialog box appears.

3. Specify the INIT property in the Property Name field and select the Instances button.
4. Select **OK**.
5. Select the flip-flop symbol in your schematic.
6. Add the INIT property to the flip-flop.

Note: Refer to the *Mentor Graphics Interface/Tutorial Guide* for more information on adding properties.

X-BLOX Support

X-BLOX supports the XC5200 device family for all platforms.

Increased Clock-to-Clock Performance

This section describes changed criteria for merging flip-flops into IOBs.

Platform: All

Architecture: XC4000A/D, XC3000A/L, XC3100A

The default criteria for merging registers into IOBs have changed to improve CLOCK to CLOCK performance. If you do not specify otherwise, X-BLOX pushes a flip-flop into an IOB where it improves the CLOCK to OUT performance according to the following rules.

- X-BLOX merges a flip-flop into an OUTFF in an IOB if one or both of the following conditions apply.
 - The flip-flop D pin is sourced (either directly or indirectly) by *non-combinational* logic. The indirect case occurs where one or more buffers and/or inverters, and no other logic, are found between the non-combinational source and the D pin.
 - The source X-BLOX symbol (if the flip-flop was generated from an X-BLOX symbol) has a parameter that indicates it should be implemented in an IOB, for example, STYLE=IOB.
- Criteria for merging flip-flops into INFFs in an IOB have not changed.

Note: In a design compiled with a previous version of X-BLOX, the clock-to-clock timing might be faster if STYLE is not specified. However, in some cases the clock-to-pad speed might be slower. If clock-to-pad speed is critical in your design, use registers in the IOB. For example, use the STYLE=IOB or STYLE=OFD definitions for DATA_REG.

Reduced Memory Usage

For all platforms and architectures, memory saving enhancements made to the X-BLOX functional simulation mode lead to significant reductions in memory usage, by as much as 50 percent for certain styles of designs.

X-BLOX Reference/User Guide Changes

The following modules have changed to support the XC5200 architecture. Modules which are not included are valid as described in the *X-BLOX Reference/User Guide*. The XC5200 attribute information in this section will be incorporated in the next revision of the *X-BLOX Reference/User Guide*.

ACCUM

Attribute: STYLE may be set to ALIGNED, UNALIGNED, or RIPPLE.

ADD_SUB

Attribute: STYLE may be set to ALIGNED, UNALIGNED, or RIPPLE.

ANDBUS

Attribute: STYLE is not supported.

BIDIR_IO

Attribute: NODELAY attribute can now be attached.

COMPARE

Attribute: STYLE may be set to ARITH, TREE, or RIPPLE. STYLE=WIRED is not supported.

DATA_REG

Attribute:

STYLE=FD is added for implementation using CLB flip-flops.

STYLE=LD is added for implementation using CLB latches.

STYLE=CLB is not supported, use STYLE=FD or STYLE=LD.

STYLE=IOB is not supported.

STYLE=ILD is not supported.

STYLE=IFD is not supported.

STYLE=OFD is not supported.

Note: For XC3000 and 4000 designs, the NODELAY attribute can be added to the DATA_REG symbol. For XC5200 designs, attach the NODELAY attribute to either the INPUTS or BIDIR_IO symbols.

INC_DEC

Attribute: STYLE may be set to ALIGNED, UNALIGNED, or RIPPLE.

INPUTS

Attribute: The NODELAY attribute can now be attached.

SHIFT

Attributes: remain unaffected.

TRISTATE

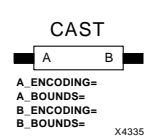
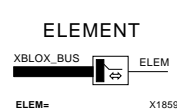
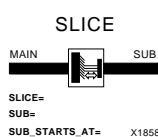
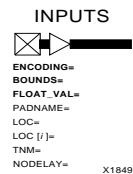
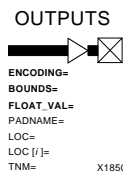
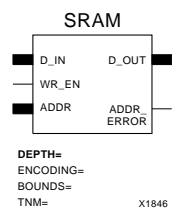
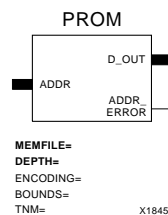
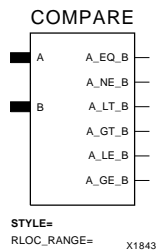
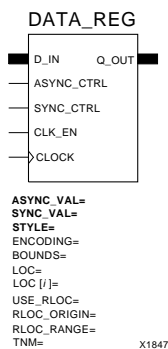
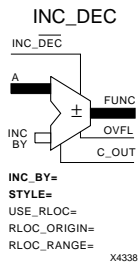
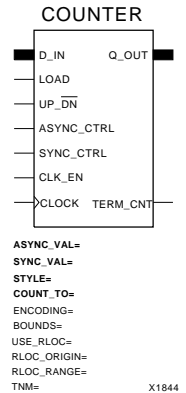
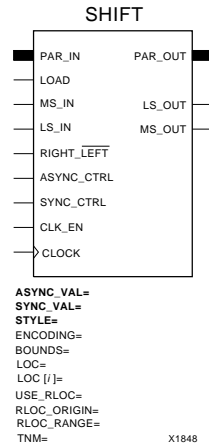
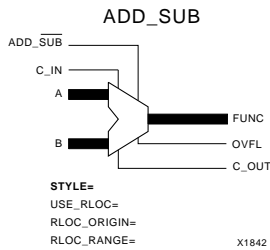
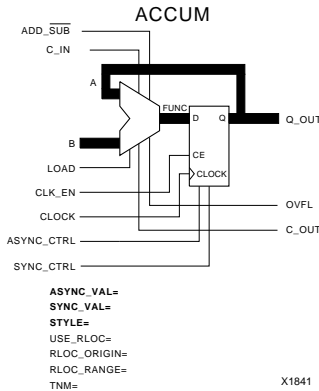
Attribute: FLOAT_VAL is not supported.

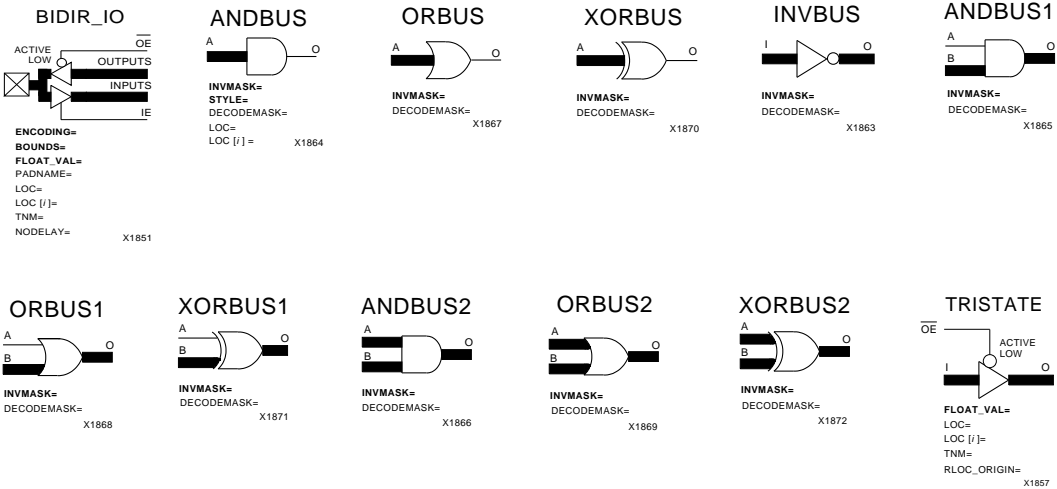
SRAM

The SRAM symbol is not supported for XC5200.

Summary of X-BLOX Symbols

Attributes that appear on schematic symbols are in bold type. Optional attributes appear in plain text. The X-BLOX symbols that are not displayed are valid as shown on the X-BLOX Symbols Reference Card.





Chapter 3

Device and Package Support

The following is a master table of Xilinx devices for this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*.

Device	Packages	Speed Grades
XC2018 ^a	PC44, PC68, PC84, PG84, TQ100, VQ64	-33, -50, -70, -100, -130
XC2064 ^a	PC44, PC68, PD48, PG68	-33, -50, -70, -100, -130
XC2018L ^a	PC84, VQ64, VQ100	-10
XC2064L ^a	PC68, VQ64	-10
XC3020 ^a	CB100, CQ100, PC68, PC84, PG84, PQ100	-50, -70, -100, -125
XC3030 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-50, -70, -100, -125
XC3042 ^a	CB100, CQ100, PC84, PG84, PG132, PP132, PQ100, TQ100	-50, -70, -100, -125
XC3064 ^{a b}	PC84, PG132, PP132, PQ160	-50, -70, -100, -125
XC3090 ^{a b}	CB164, CQ164, PC84, PG175, PP175, PQ160, PQ208	-50, -70, -100, -125
XC3020A	CB100, PC68, PC84, PG84, PQ100	-6, -7
XC3030A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-6, -7
XC3042A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-6, -7
XC3064A ^b	PC84, PG132, PP132, PQ160, TQ144	-6, -7
XC3090A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-6, -7
XC3020L	PC84	-8
XC3030L	PC84, VQ64, VQ100	-8
XC3042L	PC84, TQ144, VQ100	-8
XC3064L ^b	PC84, TQ144	-8

Device	Packages	Speed Grades
XC3090L ^b	PC84, TQ176	-8
XC3120 ^a	CB100, PC68, PC84, PG84, PQ100	-3, -4, -5
XC3130 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-3, -4, -5
XC3142 ^a	CB100, PC84, PG84, PG132, PP132, PQ100, TQ100, TQ144	-3, -4, -5
XC3164 ^{a b}	PC84, PG132, PP132, PQ160	-3, -4, -5
XC3190 ^{a b}	CB164, PC84, PG175, PP175, PQ160, PQ208	-3, -4, -5
XC3195 ^{a b}	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-3, -4, -5
XC3120A	CB100, PC68, PC84, PG84, PQ100	-1, -2, -3, -4, -5
XC3130A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-1, -2, -3, -4, -5
XC3142A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-1, -2, -3, -4, -5
XC3164A ^b	PC84, PG132, PP132, PQ160, TQ144	-1, -2, -3, -4, -5
XC3190A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-1, -2, -3, -4, -5
XC3195A ^b	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-1, -2, -3, -4, -5
XC4003	PC84, PG120, PQ100	-4, -5, -6
XC4005 ^b	CB164, PC84, PG156, PQ100, PQ160, PQ208	-3, -4, -5, -6, -6B, -10
XC4006 ^b	PC84, PG156, PQ160, PQ208	-3, -4, -5, -6
XC4008 ^b	MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6
XC4010 ^b	BG225, CB196, MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6, -10
XC4013 ^b	BG225, CB228, MQ208, MQ240, PG223, PQ160, PQ208, PQ240	-3, -4, -5, -6, -10
XC4002A	PC84, PG120, PQ100, VQ100	-5, -6
XC4003A	CB100, PC84, PG120, PQ100, VQ100	-4, -5, -6, -10
XC4004A ^b	PC84, PG120, PQ160, TQ144	-5, -6
XC4005A ^b	PC84, PG156, PQ160, PQ208, TQ144	-4, -5, -6
XC4010D ^b	BG225, PC84, PQ160, PQ208	-5, -6
XC4013D ^b	BG225, PQ160, PQ208, PQ240	-5, -6
XC4003H	PG191, PQ208	-5, -6
XC4005H ^b	MQ240, PG223, PQ240	-5, -6
XC5202	PC84, PG156, PQ100, TQ144, VQ100	-5, -6

Device	Packages	Speed Grades
XC5204	PC84, PG156, PQ100, PQ160, TQ144, VQ100	-5, -6
XC5206 ^b	PC84, PG191, PQ100, PQ160, PQ208, TQ144, VQ100	-5, -6
XC5210 ^b	BG225, PC84, PG223, PQ160, PQ208, PQ240, TQ144	-5, -6
XC5215 ^b	HQ304, PG299, PQ208, PQ240	-5, -6
XC7236A ^a	PC44	-16, -20, -25
XC7318 ^a	PC44, PQ44	-5, -7
XC7336 ^a	PC44, PQ44	-5, -7, -10, -12, -15
XC7354 ^a	PC44, PC68	-7, -10, -12, -15
XC7372 ^a	PC68, PC84, PQ100	-7, -10, -12, -15
XC7336Q ^a	PC44, PQ44, VQ44	-10, -12, -15
XC73108 ^a	BG225, PC84, PG144, PQ100, PQ160	-7, -10, -12, -15, -20
XC73144 ^a	BG225, PQ160	-7, -10, -12, -15

a. Not supported in X-BLOX.

b. Not supported in Base packages.

Known Issues

This chapter describes the known issues and workarounds for the current software release.

Software

Design Entry

EDIF2XNF Processes Port Symbols as Pads

Platform: All

Architecture: XC2000, XC3000, XC4000, XC5200

Design Step: Design Entry, Simulation

Reference Number: 19114

When EDIF2XNF is run as part of FNCSIM8 on a lower level schematic, XNFPREP may return an error similar to the following:

```
XNFPREP: ERROR 3527:
```

```
The signal '<netname>' is connected to the following  
invalid symbol pins:
```

```
<pin_list>
```

```
A pad can be connected only to the input pin of input  
symbols/clock buffers (such as, the 'I' pin of IBUF),  
and the output pin of output symbols/PULLUPS/  
PULLDOWNS (such as, the 'Q' pin of OUTFF).
```

This error occurs because EDIF2XNF inaccurately identifies PORTINs and PORTOUTs as IPADs and OPADs. XNFPREP issues the error because these “pads” are not attached to I/O buffers.

Remove all port symbols from the schematic or instantiate the schematic's symbol in an upper level sheet without ports.

Xilinx Menus Are Empty

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 6845

If the \$LCA variable is not added to mgc_location_map, you cannot select library parts from the Design Architect menus.

Be sure the \$LCA variable is added to mgc_location_map.

Autoripper Function is Not Working

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 10743

Autoripper function is not working.

Select the Set Autoripper Off command in the PLD_DA Setup menu to specify that the autoripper function is On.

Also, make sure that the \$MGC_GENLIB variable is instantiated in MGC_LOCATION_MAP.

Mentor Graphics Netcon Symbol Is Not Supported

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 7268

The Mentor Graphics gen_lib netcon symbol is not supported by the Xilinx EDIF2XNF tool. EDIF2XNF will not join two nets associated by a netcon symbol.

Do not use the netcon symbol in a Xilinx design.

Check Sheet Produces “qp_prim” Warning Message

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 7423

Design Architect can lose the value of the lca_technology parameter, causing warnings similar to the following to appear:

```
Warning:Unable to evaluate property "_qp_prim" on \  
instance.  
Unable to evaluate expression.
```

This warning can be ignored. Entering the following command in Design Architect might eliminate the warning messages:

```
$set_parameter("lca_technology", "xc3000", "string");
```

If using an XC4000 design, replace “xc3000” with “xc4000”.

I/O Pad Symbols Cannot Be Placed on Lower Level Hierarchical Sheets

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 13518

The CLASS=P property has been placed on Xilinx pad symbols in order to identify them to the Mentor Graphics tools as package pins. As a result, placing pad symbols on lower level hierarchical sheets without placing an associated pin on the hierarchical symbol causes the following error to occur:

```
Error: External net "net_name" is not connected to \  
any pin of symbol "symbol_name".
```

Move the pads to the top level of the design and add pins to the hierarchical symbol for the pads.

4-bit I/O Pad Symbols in the DS-344 Library Do Not Match the XACT Libraries Guide

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 16586

The ipad4, opad4, and iopad4 symbols in the new Unified Libraries have a single bus pin attached to them. This is in contrast to the description in the Libraries Guide, which shows four distinct pins. This change was necessary in order to add the CLASS=P property to the I/O symbols to identify them as package pins to the Mentor Graphics tools. This might cause difficulty when trying to interface to the ibuf4, obuf4, and other 4-bit I/O symbols, which have four individual pins on them.

If using the ibuf4, obuf4, or other 4-bit I/O symbols, which must be attached to pads, it might be easier to attach four one-bit pad symbols to them. Otherwise, the bused 4-bit pad symbols can be attached using a bus with bus rippers to individual signals.

Multiple LOC Values Cannot Be Added to Symbol

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 16243

You cannot add more than one LOC property to the same symbol in Design Architect.

Although you cannot add more than one LOC property to a symbol, you can specify multiple values for the same LOC property. You can add multiple LOC values to a LOC property by separating the values with a semi-colon(;), as shown in the examples in the following table.

Property Value	Description
T; L (XC4000 only)	Place decoder on the top or left edge.
CLB_R1C1; CLB_R5C5; LOC <>CLB_R5C5 (XC40000 only)	Place CLB logic in the top left corner in a 5x5 area, but not in the CLB in row 5, column 5.

If multiple LOC values specify different locations or areas, the software selects only one value. If multiple prohibit values are specified, the software attempts to meet all the values. If the LOC values prohibit certain areas and specify other areas, the software attempts to meet all the prohibit values and selects only one value that specifies an area.

Obsolete Symbol Message Appears When Instantiation of Obsolete Symbol Is Attempted

Platform: All

Architecture: XC2000, XC3000, XC4000

Design Step: Design Entry

Reference Number: Not Available

If you attempt to instantiate one of the obsolete symbols, a message appears informing you that the symbol is now obsolete.

Obsolete symbols are included in the Unified Library for the XC2000, XC3000, and XC4000 families. The obsolete symbols are in the same directories as the new unified symbols, but they are not included in the menus. If you attempt to instantiate one of the obsolete symbols, a message appears informing you that the symbol is now obsolete. In some cases, an alternative unified symbol is recommended. Refer to the “Selection Guide” chapter of the *Libraries Guide* for tables showing the names of equivalent elements for obsolete components.

Unified Libraries BUFE Elements Might Require Logic Level for Inversion

Platform: All

Architecture: XC3000, XC3100, XC4000

Design Step: Design Entry

Reference Number: 14336

For convenience, the Unified Libraries include 3-state buffer elements with both active-Low enable (the BUFT elements) and active-High enable (the BUFE elements). The actual 3-state buffers in the XC4000- and XC3000-based architectures have active-Low enables that are not directly invertible. If a BUFE element is sourced by a gate, the inversion of the enable signal is performed at the source and no extra delay is incurred. However, if a BUFE element is sourced by a flip-flop, or by another element without a dedicated output inversion, the inver-

sion of the enable signal is implemented in an additional function generator, adding an extra level of delay to the path.

When an inverter cannot be absorbed at the source or load pins, XNFFPrep issues a message similar to the following:

```
XNFFPREP: WARNING 4037
```

```
These inverters could not be absorbed and each will be  
implemented in a single function generator. This will  
introduce additional delay and use resources  
inefficiently. (Note that some of the symbols listed  
below might have been reduced to inverters by earlier  
trimming.)
```

```
Inverter Name = <inverter_name>
```

```
Output Signal = <signal_name>/T
```

The presence of “/T” at the end of the output signal name indicates that the inverter might be part of a BUFE component.

If the delay on a 3-state enable path is important, and the enable signal is sourced by a non-invertible output, avoid using a BUFE component if possible.

When Changing Library References, the Existing Viewpoint is Not Automatically Overwritten

Platform: All

Architecture: All

Design Step: Design Entry

Reference Number: 16345

When you migrate to a different architecture, for example, from an XC3000 device to an XC4000 device, the `lca_technology` variable in the existing XNF viewpoint file is set to the original architecture. This viewpoint is not overwritten when you migrate to a different architecture.

Men2XNF8 may return a warning similar to the following:

```
Note: Building cell construct "ibuf". (from:  
Synthesis/EDIF Interface/Design Data Port 82)
```

```
Warning: Instance: '/I$628'
```

```
Could not find a registered simulation model with  
label: 'xc3000'
```

NULL model will be inserted. (from Analysis/Digital Simulation Utility /DSIM 85)

Delete existing XNF viewpoint.

Incorrect Pintypes on Pad Symbols

Platform: All

Architecture: All

Design Step: Design Entry

Reference Number: 19146

The IPAD, OPAD, and IOPAD symbols in the Unified Libraries do not have pintype properties. Therefore, the Mentor Graphics program that creates symbols interprets the pins on the pads as inputs only.

If a pintype error occurs, perform the following steps:

1. Select the pad symbol in the Design Architect window.
2. Select **File** → **Open Down** from the menu bar using the left mouse button.

The Open Down dialog box appears.

3. Select the pad symbol and select **OK**.
4. Select **File** → **Save Symbol As**.

The Save Symbol As dialog box appears.

5. Enter a new name and a local directory for the symbol.
6. Select **OK** to save the new symbol.
7. Select the pad symbol in the Symbol window.
8. Select **Properties** → **Add** using the right mouse button.
9. Scroll through the list of existing property names and click with the left mouse button on the Pintype property.
10. In the Property Value box, enter out for OPADs or ixo for IOPADs.
11. Click the **OK** button. The **ADD PR** prompt bar appears.
12. Move the cursor to where you want to place the property text and click the left mouse button to place it.

13. Save the symbol.
14. Instantiate your local symbol instead of the library symbol.

Retargeting Designs to Different Device Families Does Not Update Design Viewpoint

Platform: All

Architecture: All

Design Step: Design Entry, Translation to XNF

Reference Number: 16363

When retargeting a design to a different device family, the design viewpoint might contain a reference to the old device family.

Manually delete the old viewpoint (it will not be automatically regenerated by Men2XNF8) using the following UNIX shell commands:

```
delete_object design_name/xnf  
delete_object design_name/default
```

XNFMerge Produces Error When Symbol Names Are Not Unique

Platform: All

Architecture: All

Design Step: Design Entry, Translation to XNF

Reference Number: 18219

The following XNFMerge error message is displayed:

```
Error 221: Filename symbol_name.xnf called  
recursively.  
Can't accept recursive designs.
```

Do not give symbols the same names as primitives or other symbols in a lower-level schematic.

Translation to XNF

EDIF2XNF Does Support Net Name Aliasing

Platform: All

Architecture: XC2000, XC3000, XC4000, XC5200

Design Step: Translation to XNF

Reference Number: 18643

EDIF2XNF processes a net with multiple net names as two or more separate, unconnected nets and does not issue an error message in this situation. As a result, XNFPrep may trim what appears to be connected logic. Net name aliasing usually occurs when a bus-ripped net is given a name that differs from that of the bus. In Xilinx designs, you must give bus-ripped nets the same name as the bus. For example, if bit three is ripped off the BUNDLE(7:0) bus, the net should be named BUNDLE(3).

Change net names by passing the nets through BUF symbols.

ENWRITE Does Not Report Error Messages if the \$LCA Environment Variable is Not Set Correctly

Platform: All

Architecture: All

Design Step: Translation to XNF

Reference Number: 4497

If the \$LCA variable is not set correctly, ENWRITE will not accurately write the lower level primitives in the EDIF file.

Make sure the \$LCA environment variable is set correctly.

ENWRITE Does Not Overwrite Existing EDIF Files

Platform: All

Architecture: All

Design Step: Translation to XNF

Reference Number: 4505

Remove the “old” EDIF files before running ENWRITE, or use the Men2XNF8 script, which deletes them automatically.

I/O Pad Symbol Properties Do Not Appear in EDIF, XNF Netlists

Platform: All
Architecture: All
Design Step: Translation to XNF
Reference Number: 12892

In DS-344 V5.x, the CLASS=P property has been placed on all I/O pad symbols in the Unified Libraries in order to identify them to the Mentor Graphics tools as package pins. Because of the addition of this property, no other properties placed on the pads are translated to the EDIF file; the Pxx pin location property that is on the pin of the pad becomes part of the net attached to the pad.

All properties that previously could be placed on the pad symbols should now be placed on the net associated with the pad.

EDIF2XNF Incorrectly Recognizes OPAD16 as a Primitive Instead of a Macro

Platform: All
Architecture: XC4000
Design Step: Translation to XNF
Reference Number: 24520

EDIF2XNF produces an error similar to the following:

```
Error: 6 EDIF data "opad16.eds" not found in directory
"/home/xact/520/ds344/data/unified/edif4000"
Cell OPAD16 is not a recognized Xilinx primitive
component;
This means that there is no CONTENTS record found in
this cell.
```

Consult the EDIF2XNF documentation to find out how to map foreign primitives to Xilinx components or fix the EDIF input file.

Make sure the EDIF data files are installed in the XACT directory.

This error message occurs if your design was created with pre-8.2_5 Mentor Graphics tools. To solve this problem, load, check, and save your design using 8.2_5 Design Architect or later.

Implementation

PLD_XMake Without -x Option Does Not Work on Designs with ABL Modules on Machines That Do Not Support ABL2XNF (HP and RS6000 Machines)

Platform: HPPA

Architecture: All

Design Step: Implementation

Reference Number: 16711

To run PLD_XMake on a design with ABL modules, manually translate the design on a machine that supports ABL2XNF; transfer the XNF file to the machine running Mentor Graphics Design Manager; and run XMake with the -x option at the command line.

Simulation

XNFBA Produces Error When LCA File from MakeBits V4.x Is Used As Input

Platform: All

Architecture: XC2000, XC3000, XC4000, XC5200

Design Step: Simulation File Creation

Reference Number: 16848

Prior to XACT 5.0, MakeBits -w was the processing step that incorporated routing delays into a routed LCA file. Beginning with the XACT 5.x release, XDelay -w performs this function. If MakeBits V4.x was used to incorporate routing delays, XNFBA V5.x might issue one or more error messages similar to the following:

```
ERROR 301: Delay 1.5 on PIN 0 of <symbol_type>
          <symbol_name> is not annotated.
The pin is connected to the signal <signal_name>.
```

To process LCA files annotated by MakeBits V4.x, run XDelay -w V5.x before you run XNFBA.

F/F, Input Latches, and RAM Models Go to Unknown State (x) During Simulation

Platform: All
Architecture: All
Design Step: Simulation
Reference Number: Not Available

If the timing requirements of the flip-flop, latch, or RAM primitives are violated, the output of the symbol is driven to an unknown state. This emulates the behavior in the actual devices.

QuickSim II provides the flexibility to turn the violation checking on or off, via the `-consm` option. If this option is set to “messages”, violation checking occurs. If QuickSim is started with the “`-consm off`” option, it ignores all setup, hold, and pulsewidth parameters.

QuickSim II Cannot Force ‘X’ on a Bus or Net of Type Decimal

Platform: All
Architecture: All
Design Step: Simulation
Reference Number: 4581

Mentor Graphics does not support the forcing of an unknown value (“X”) on a bus or a net that is defined in simulation with a decimal radix.

Use a hex or binary radix for the bus.

QuickSim II Gives “Binding Not Present” Error

Platform: All
Architecture: All
Design Step: Simulation
Reference Number: 4745

If a design viewpoint does not exist, QuickSim II issues an error message similar to the following:

```
/// Error: Binding not present for lca_technology \  
    (from: Uims/Mule/Scope 02)  
// Error: lca_technology undefined at line 1 \  
    (from: Uims/Ample/Ample_eval 0A)  
// Note: Suspended at line 1 (from: Uims/Ample\
```



```
/Ample_eval 0B)
// Error: Instance: `I$21/DFF'
// MODEL property expected but not found on \
primitive instance.
// NULL model will be inserted. (from: Analysis\
/Digital Simulation Utilities/Dsim 1D)
```

Run PLD_DVE_SIM to create a design viewpoint and run QuickSim II again.

QuickSim II, Globalsetreset Does Not Model FFs or Latches Correctly if Inputs Are Unknown

Platform: All
Architecture: XC3000, XC4000, XC5200
Design Step: Simulation
Reference Number: 7206

Flip-flops do not remain reset automatically when “globalreset” (XC5200), “globalsetreset” (XC4000), or “globalresetb” (XC3000), is deasserted. If any of the inputs to the flip-flop are unknown when the global reset signal is deasserted, the flip-flop output might become unknown.

Be sure all the flip-flop inputs are driven to a known value before releasing the global reset signal, or place INIT properties on the nets to define their initial value.

QuickSim II Might Crash and Produce Errors in PLD_DMGR

Platform: All
Architecture: All
Design Step: Simulation
Reference Number: 8324

Occasionally, QuickSim II might encounter a memory fault or other problem while exiting, causing it to crash. If QuickSim II was started from within PLD_DMGR, PLD_DMGR will report a return code error 139 and indicate that QuickSim failed.

Save all vital information before exiting QuickSim II. Otherwise, the error can be ignored.

FNCSIM8 with -o Option Cannot Be Run on Designs that Contain Symbols with the FILE Property That Are Not Located in the Same Directory as the Top Level of Your Design

Platform: All

Architecture: XC2000, XC3000, XC4000, XC5200

Design Step: Simulation

Reference Number: 15728

You can include an XNF file from another source in your design by creating a symbol to represent the file, and then placing a FILE property on the symbol. The property value is the name of the netlist you want to include. If this symbol is not instantiated in the top level of the design hierarchy, FNCSIM8 will not run correctly with the -o option.

Place the XNF files in the same directory as the top-level component of the design hierarchy, or run FNCSIM8 with the -g option.

Symbol with FILE Property Must Exist in the Same Directory as the Top Level of Your Design

Platform: All

Architecture: XC2000, XC3000, XC4000, XC5200

Design Step: Simulation

Reference Number: 15245

Quicksim II issues an error similar to the following:

```
Instance: /I$13
MODEL property expected but not found on primitive
instance
NULL model will be inserted.
```

This error message occurs if you use the FILE Property on user-created symbols that are not in the same directory as the top level design.

To solve this problem, perform one of the following:

- Save the symbol and the file in the same directory as the top level design and make sure that the file has the same name as the symbol.

or

- Run FNCSIM8 and TIMSIM8 with the Auto Generate option. This option is not recommended because computer-generated schematics are used during simulation instead of your original schematics.

Note: Refer to the “FPGA Design Issues” chapter in the *Mentor Graphics Interface/Tutorial Guide* for more information on the File property.

X-BLOX Functional Simulation Requires That All X-BLOX Nets, Buses, and Instances Be Named

Platform: All

Architecture: XC3000A, XC4000, XC5200

Design Step: Simulation

Reference Number: 16608

The XBLXGS program, which draws X-BLOX functional simulation schematics, might fail if X-BLOX nets, buses, and instances do not have names attached to them.

Be sure all the X-BLOX nets, buses, and instances have names attached to them. Nets and buses are given names by attaching a NET property, while symbols are given names by attaching an INST property.

EPLD Setup Time Violations

Platform: All

Architecture: XC7000

Design Step: Simulation

Reference Number: Not Available

If your EPLD design uses input-pad registers or latches, timing simulation issues setup time violations if you change the data input at the same time as the clock edge. EPLD device specifications allow zero hold time for input-pad registers/latches.

You can safely ignore the violation.

Gen_Sch8 -w Overwrites User-Generated Schematics

Platform: All
Architecture: All
Design Step: Simulation
Reference Number: 17026

The following command overwrites schematics generated by you with schematics generated by the computer:

```
gen_sch8 -w design.xnf
```

No warning messages are displayed.

Use the -w option with Gen_Sch8 only when you want to overwrite simulation schematics. Be sure to specify the simulation XNF file as the input file as shown in the following examples:

```
gen_sch8 -w design_fnc.xnf
```

or

```
gen_sch8 -w design_tim.xnf
```

Gen_Sch8 Does Not Preserve Net Names

Platform: All
Architecture: XC2000, XC3000, XC4000, XC5200
Design Step: Simulation
Reference Number: 19375

The signals on X-BLOX Inputs and Outputs symbols have different names during simulation.

The signals connected to Input symbols are loads for the input buffers and the signals connected to Output symbols are sources for the output buffers.

If your original schematic is used, the signal between the pad and the buffer is named:

input or output instance/PAD(n)

Note: n = bit number.

If you add the PADNAME property to the Inputs or Outputs symbol, the name becomes:

input or output instance/ value of PADNAME property(n)

If you use an auto-generated schematic, the schematic is flattened and the “/” is replaced by “_”. The new names are:

input or output instance_PAD(0)

or

input or output instance_value of PADNAME property(n)

You can use original schematics for designs that contain X-BLOX components only for functional simulation.

Gen_Sch8 Does Not Run Under the Solaris Operating System

Platform: All

Architecture: All

Design Step: Simulation

Reference Number: Not Available.

The Solaris operating system is not officially supported. However, based on limited testing of this operating system, the XACT core tools and the Mentor Graphics interface tools, with the exception of Gen_Sch8, do run under Solaris.

Hold Violations

Platform: All

Architecture: XC2000, XC3000, XC4000, XC5200

Design Step: Simulation

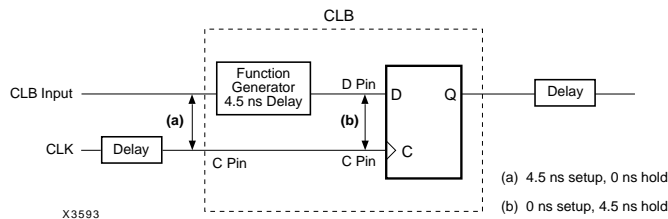
Reference Number: 10626

During simulation, you may encounter hold violations on flip-flops used in your design. According to *The Programmable Logic Data Book*, there is no hold time for the flip-flops in a CLB unless the DIN pin is used. The absence of hold-time requirements is reflected in the modeling in the routed XNF file similar to the following.

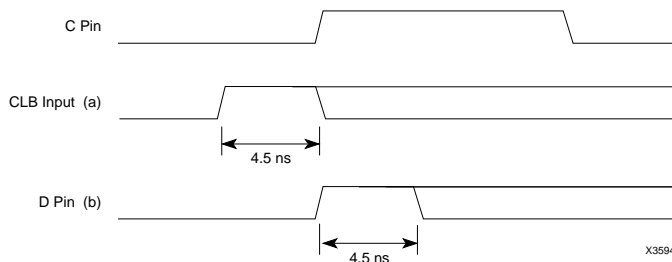
```
SYM, Q1.QX, DFF, INIT=R
  PIN, Q, 0, Q1.QX, 5.0
  PIN, D, I, Q1.F
  PIN, C, I, CAB, 6.1
  PIN, CE, I, BCE, 0
  PULSE, C, +, 4.0
  SETUP, D, C, +, 0.0, 4.5
END
```

The Setup line indicates that the input pin D is clocked by C, which is positive-edge-triggered, and has a setup time of 0 ns and a hold time of 4.5 ns. This XNF file is for an XC4000 device with a speed grade of 5. If you look up the setup time for a CLB flip-flop in *The Programmable Logic Data Book*, the setup time is 4.5 ns, and the hold time is 0 ns.

The setup and hold-time specifications in the Xilinx data sheets are based on a comparison of the CLB input signal and the CLB clock input, which is also the clock input of the flip-flop. This comparison is illustrated as (a) in the figure below. Before QuickSim reads your netlist, the CLB is broken down into gates and flip-flops. QuickSim checks the setup and hold time by comparing the D input of the flip-flop and the clock input, shown as comparison (b) in the figure below.



Consequently, QuickSim may report what appears to be a setup violation from the viewpoint of the CLB specification as a hold violation. A hold violation waveform is shown in the figure below. Since the sum of the setup and hold-time requirements is the same in either case, whether the violation is reported as a setup or hold-time violation is immaterial.



Documentation

Mentor Graphics Interface/Tutorial Guide

Path Variable is Incorrectly Set

Platform: All

Architecture: All

Design Step: Not Available

Reference Number: 10737

Path variable is incorrectly set. Do not use uppercase letters for the path variable.

Correct:

```
set path=( $PATH
```

Incorrect:

```
set PATH=( $PATH
```


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