

# Addendum to LogiCore Release Document

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## LogiCore PCI Interface

The following schematic pages have been modified to incorporate new features and to update known problems. This is an incremental pre-release. The same and additional modifications and features will be included in the Version 1.10 release (planned release date July 96).

*Download the latest files from our Technical Bulletin Board, FTP site, or Xilinx Home Page.* The files are compressed in two versions:

1. pcimay96.zip with pkzip (DOS) or zip (UNIX)
2. pcimay96.tar with tar (UNIX)

## Installation

1. Downloading from the BBS -- see instructions in *The Xilinx Programmable Logic Data Book*, page 6-2.
2. Downloading from the Xilinx FTP site --  
`ftp://ftp.xilinx.com/pub/products/logicore`
3. Downloading from the Xilinx Home Page -- type the following address and file name in your web browser.  
`http://www.xilinx.com/pcimay96.zip` or  
`http://www.xilinx.com/pcimay96.tar`
4. To unpack the files, type:  
`pkunzip -d pcimay96.zip` (DOS)  
`unzip -d pcimay96.zip` (UNIX) or  
`tar -xvf pcimay96.tar` (UNIX).

## Updating Your Design

1. *Important!!* Make a back-up copy of your existing design!
2. Copy the appropriate schematic files into your project's /sch directory.
3. Copy the appropriate symbol files into your project's /sym directory.
4. Re-run 'check -p' on your top-level design.
5. Re-run 'vsm -h' on the top-level design for functional simulation.
6. Re-run PPR to place and route the design.

## Known Issues

### Output Enable Signals out of Sync

Platform: All

Architecture: XC4013E-3PQ208C

Design Step: Simulation

Reference Number: NA

The output enable signals for TRDY-, STOP-, and DEVSEL- turn on one cycle too late and turn off one cycle too late. The output enable signal is common to TRDY-, STOP-, and DEVSEL-.

To avoid the problem of mis-timed output enable signals, you should update these files in your design.

/sch Directory

pci\_lc.3 - add TRDY- and M\_DATA signals to symbol 'pci-cntl'

pci-cntl.3 - add TRDY- and M\_DATA signals to symbol 'pci-ofcn'

pci-ofcn.1 - various fixes to output enables and STOP- logic

pci-xoe.1 - fixes internal contention problem, output enable on TRDY-, STOP-, and DEVSEL-

pci-xoe.2 - improves performance on output enable timing for the Address/Data bus

pci-xoe.3 - new page containing mapping information

pci\_lc.4 - adds new output enable for PAR based on the output

enable for AD

/sym Directory

pci-cntl.1 - add TRDY- and M\_DATA signals to symbol

pci-ofcn.1 - add TRDY- and M\_DATA signals to symbol

pci-xoe.1 - add various signals to symbol

## **Internal Contention on the ADIO Bus**

Platform: All

Architecture: XC4013E-3PQ208C

Design Step: Simulation

Reference Number: NA

There is internal contention on the ADIO bus following a Target Write.

To avoid the problem of contention on the ADIO Bus, you should update these files in your design.

/sch Directory

pci\_lc.3 - add TRDY- and M\_DATA signals to symbol 'pci-cntl'

pci-cntl.3 - add TRDY- and M\_DATA signals to symbol 'pci-ofcn'

pci-ofcn.1 - various fixes to output enables and STOP- logic

pci-xoe.1 - fixes internal contention problem, output enable on TRDY-, STOP-, and DEVSEL-

pci-xoe.2 - improves performance on output enable timing for the Address/Data bus

pci-xoe.3 - new page containing mapping information

pci\_lc.4 - adds new output enable for PAR based on the output enable for AD

/sym Directory

pci-cntl.1 - add TRDY- and M\_DATA signals to symbol

pci-ofcn.1 - add TRDY- and M\_DATA signals to symbol

pci-xoe.1 - add various signals to symbol

## **TERM Macro Does Not Support Target Abort (T\_ABORT)**

Platform: All  
Architecture: XC4013E-3PQ208C  
Design Step: Simulation  
Reference Number: NA

TERM must be asserted carefully during S\_DATA phase to cause either Target Retry or Target Disconnect conditions. The TERM signal must be asserted during a specific window for the macro to correctly assert STOP-.

To avoid the problem of this unsupported macro, you should update these files in your design.

/sch Directory

pci-stop.1 - adds Target Abort support, TERM can be asserted at any time.

pci-dsel.1 - allows macro to claim cycle when T\_ABORT is asserted by the user application.

pci-dsel.2 - updates mapping information to reflect changes in 'pci-dsel.1'.

## **Not All Outputs Are Tri-stated When RST Is Asserted**

Platform: All  
Architecture: XC4013E-3PQ208C  
Design Step: Simulation  
Reference Number: NA

See PCI bus specification, revision 2.1, section 4.3.2 for a full description.

To address this issue, update the following files in your design.

/sch Directory

pci\_lc.5 - connects RST- signal to Global Tri-State signal on the STARTUP symbol.

## **Some Features May Be Unsupported**

Platform: All  
Architecture: XC4013E-3PQ208C  
Design Step: Simulation  
Reference Number: NA

All of the bits in the Command/Status register are implemented using flip-flops, include the reserved bits. Some features, such as fast back-to-back, are not supported.

To address this issue, update the following files in your design.

/sch Directory

cmdreg.1

statreg.1

## **Some Bits in the Status Register Are Not Set**

Platform: All  
Architecture: XC4013E-3PQ208C  
Design Step: Simulation  
Reference Number: NA

The SERR- pin did not have an enable from the Command Register. As a result, various bits in the status register may not be set automatically.

To address this issue, update the following files in your design.

/sch Directory

pci\_lc.4

Status bits are automatically asserted for

1. Detected Parity Error, Status bit 15
2. Signalled System Error, Status bit 14, tied Low (SERR- not supported)
3. Received Master-Abort, Status bit 13, tied Low (Initiator function)
4. Received Target-Abort, Status bit 12, tied Low (Initiator function)
5. Signalled Target-Abort, Status bit 11
6. DEVSEL- Timing, Status 10-9, tied to '10'b (SLOW decode)

7. Data Parity Reported, Status 8, tied Low (Initiator function)
8. Fast Back-to-Back Capable, Status bit 7, tied Low (not supported)

### **Problem with the FIFO in the Example Application**

Platform: All

Architecture: XC4013E-3PQ208C

Design Step: Simulation

Reference Number: NA

There is a problem with the FIFO in the example application because it asserts STOP- when the FIFO is about to be over- or under-run. The current implementation asserts TERM at the wrong time and consequently, the LogiCore macro asserts STOP- at the wrong time.

To address this issue, update the following files in your design.

/sch Directory

ctl\_f\_t.1



The Programmable Logic Company<sup>SM</sup>



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