



Release Document

XACT^{step} Version 5.2/6.0
Xilinx ABEL

October 1995

Read This Before Installation

Versions and Compatibility

The following master table indicates Xilinx core software with the current version numbers.

Software Versions

Program	Windows Version	DOS Version	Workstation Version
APR	5.2	5.2	5.2
APRLOOP	5.2	5.2	5.2
CstCvt	5.2	5.2	5.2
Design Manager	6.0	N/A	N/A
Floorplanner	6.0	N/A	5.2
Flow Engine	6.0	N/A	N/A
Hardware Debugger	6.0	N/A	N/A
HM2RPM	5.2	5.2	5.2
LCA2XNF	5.2	5.2	5.2
MakeBits	5.2	5.2	5.2
MakePROM	5.2	5.2	5.2
MAP2LCA	5.2	5.2	5.2
MemGen	5.2	5.2	5.2
PPR	5.2	5.2	5.2
PROM File Formatter	6.0	N/A	N/A
Report Browser	6.0	N/A	N/A
SymGen	5.2	5.2	5.2
Timing Analyzer	6.0	N/A	N/A

Program	Windows Version	DOS Version	Workstation Version
XACT	5.2	5.2	5.2
XBLOX	5.2	5.2	5.2
XChecker	5.2	5.2	5.2
XCK88	N/A	5.2	N/A
XDE	5.2	5.2	5.2
XDelay	5.2	5.2	5.2
XDM	N/A	N/A	5.2
xdm	5.2	5.2	5.2
XEMake	N/A	N/A	5.2
XEMake6	6.0	N/A	N/A
XKey	5.2	5.2	N/A
XMake	5.2	5.2	5.2
XNFBA	5.2	5.2	5.2
XNFCvt	5.2	5.2	5.2
XNFMAP	5.2	5.2	5.2
XNFMerge	5.2	5.2	5.2
XNFPrep	5.2	5.2	5.2
XPP	5.2	5.2	5.2
XPrint	5.2	5.2	5.2
XSimMake	5.2	5.2	5.2

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Chapter 1

Introduction

Welcome to the Xilinx ABEL (XABEL) Interface from Xilinx!

Xilinx software products have prefixes to designate the type of products you receive.

- DS = Development System (new system)
- DX = Development System Upgrade (upgrade to current system)
- SC = Support Contract (update to current system)
- SR = Support Reinstatement (update to non-current system)

This release note supports the following products.

- Xilinx ABEL Interface and Package (DS-371)

Contents

The Development System (DS) product you received contains software and documentation. Update products also have software and documentation.

Hardware

Xilinx ABEL requires a programmable key for operation. This key is supplied with Xilinx PC (Standard, Extended, and DS-VLS-BAS) packages or Core FPGA (DS-502) software. If you have purchased Xilinx ABEL and do not already have a key, contact Xilinx Customer Service.

Software

Xilinx software for all platforms is provided on CD-ROM. It consists of the following.

- Installation Program
- Xilinx ABEL (DS-371)

Documentation

The following documentation is available in print for Xilinx ABEL products.

- *Getting Started & Installation Guide*
- *Additional Products & Services Packet*
- *Xilinx ABEL User Guide*
- *Xilinx-ABEL Software Design Reference Manual*¹

Online Documentation

All documentation supporting Xilinx Core FPGA and EPLD software products is available online.

Selected Xilinx manuals are available in printed form. See the “Documentation Order Form” in the *Additional Products & Services Packet*.

Maintenance and Support

This product comes with free technical and product information telephone support (toll-free in the U.S. and Canada). You can also fax and e-mail your questions. See the “Xilinx Customer Support Information” chapter of this release note for offices and phone numbers.

This product comes with one year of maintenance; you will receive all software and documentation updates automatically during that time. You will receive a notice at the end of the year giving instructions on how to renew your maintenance contract.

1. Included in DS and SR products only.

Chapter 2

Features in This Release

This chapter lists the new features in this release.

XC5000 Support

This release adds XC5000 family support to Xilinx ABEL.

Map Property Limit for XC5000 Family

The maximum number of inputs for the XC5000 CLB is 5.

HP700 Platform Support

Xilinx ABEL is now supported on the HP700 platform. The Xilinx ABEL graphical user interface is not supported in this release. Instead, the ABL2XNF program is provided to run Xilinx ABEL on the command line. Refer to the *Xilinx ABEL User Guide* for instructions on invoking Xilinx ABEL from the command line.

Block Property for TIMESPEC Attributes

A new Xilinx Block property statement has been added to allow you to assign timing specifications to a register. The syntax of this statement is the following:

```
Xilinx Property 'BLOCK register_name TNM=name_list' ;
```

For more information on TNM and name lists, refer to the “XACT-Performance” chapter of the *Development System Reference Guide*.

Map Property for Registered Signals

You can now use Xilinx Map property statement for registered signals as well as for combinatorial signals.

ABL2XNF Addpins Command Line Option

A new ABL2XNF command-line option, Addpins, adds IOBs to the external pin records in the XNF file generated by Xilinx ABEL. Only input pins and output pins can be added to the XNF file. Bidirectional pins or output pins with tristate control are not supported. This XNF file can be processed with the Xilinx placing and routing software for simple stand-alone designs without an upper-level schematic. The syntax of the Addpins option is the following:

```
abl2xnf addpins={true|false}
```

The default value is False.

Create_Mapped_XNF Option Added to GUI

The Create_Mapped_XNF option has been added to the graphical user interface. It allows SynthX, rather than the placing and routing software, to map the logic. In the *Xilinx ABEL User Guide*, this option is called the Mapped_XNF option.

OE Extension Support for XC2000 Family

The .OE dot extension is now supported for XC2000 FPGA designs in addition to XC7000 CPLD designs. This dot extension is not supported for other FPGA families.

Chapter 3

Device and Package Support

The following is a master table of Xilinx devices for this release. For more information on architectural families and specific device parameters, see *The Programmable Logic Data Book*.

Device	Packages	Speed Grades
XC2018 ^a	PC44, PC68, PC84, PG84, TQ100, VQ64	-33, -50, -70, -100, -130
XC2064 ^a	PC44, PC68, PD48, PG68	-33, -50, -70, -100, -130
XC2018L ^a	PC84, VQ64, VQ100	-10
XC2064L ^a	PC68, VQ64	-10
XC3020 ^a	CB100, CQ100, PC68, PC84, PG84, PQ100	-50, -70, -100, -125
XC3030 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-50, -70, -100, -125
XC3042 ^a	CB100, CQ100, PC84, PG84, PG132, PP132, PQ100, TQ100	-50, -70, -100, -125
XC3064 ^{a b}	PC84, PG132, PP132, PQ160	-50, -70, -100, -125
XC3090 ^{a b}	CB164, CQ164, PC84, PG175, PP175, PQ160, PQ208	-50, -70, -100, -125
XC3020A	CB100, PC68, PC84, PG84, PQ100	-6, -7
XC3030A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-6, -7
XC3042A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-6, -7
XC3064A ^b	PC84, PG132, PP132, PQ160, TQ144	-6, -7
XC3090A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-6, -7
XC3020L	PC84	-8
XC3030L	PC84, VQ64, VQ100	-8
XC3042L	PC84, TQ144, VQ100	-8
XC3064L ^b	PC84, TQ144	-8

Device	Packages	Speed Grades
XC3090L ^b	PC84, TQ176	-8
XC3120 ^a	CB100, PC68, PC84, PG84, PQ100	-3, -4, -5
XC3130 ^a	PC44, PC68, PC84, PG84, PQ100, TQ100	-3, -4, -5
XC3142 ^a	CB100, PC84, PG84, PG132, PP132, PQ100, TQ100, TQ144	-3, -4, -5
XC3164 ^{a b}	PC84, PG132, PP132, PQ160	-3, -4, -5
XC3190 ^{a b}	CB164, PC84, PG175, PP175, PQ160, PQ208	-3, -4, -5
XC3195 ^{a b}	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-3, -4, -5
XC3120A	CB100, PC68, PC84, PG84, PQ100	-1, -2, -3, -4, -5
XC3130A	PC44, PC68, PC84, PG84, PQ100, VQ64, VQ100	-1, -2, -3, -4, -5
XC3142A	CB100, PC84, PG84, PG132, PP132, PQ100, TQ144, VQ100	-1, -2, -3, -4, -5
XC3164A ^b	PC84, PG132, PP132, PQ160, TQ144	-1, -2, -3, -4, -5
XC3190A ^b	CB164, PC84, PG175, PP175, PQ160, PQ208, TQ176	-1, -2, -3, -4, -5
XC3195A ^b	CB164, PC84, PG175, PG223, PP175, PQ160, PQ208	-1, -2, -3, -4, -5
XC4003	PC84, PG120, PQ100	-4, -5, -6
XC4005 ^b	CB164, PC84, PG156, PQ100, PQ160, PQ208	-3, -4, -5, -6, -6B, -10
XC4006 ^b	PC84, PG156, PQ160, PQ208	-3, -4, -5, -6
XC4008 ^b	MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6
XC4010 ^b	BG225, CB196, MQ208, PC84, PG191, PQ160, PQ208	-3, -4, -5, -6, -10
XC4013 ^b	BG225, CB228, MQ208, MQ240, PG223, PQ160, PQ208, PQ240	-3, -4, -5, -6, -10
XC4002A	PC84, PG120, PQ100, VQ100	-5, -6
XC4003A	CB100, PC84, PG120, PQ100, VQ100	-4, -5, -6, -10
XC4004A ^b	PC84, PG120, PQ160, TQ144	-5, -6
XC4005A ^b	PC84, PG156, PQ160, PQ208, TQ144	-4, -5, -6
XC4010D ^b	BG225, PC84, PQ160, PQ208	-5, -6
XC4013D ^b	BG225, PQ160, PQ208, PQ240	-5, -6
XC4003H	PG191, PQ208	-5, -6
XC4005H ^b	MQ240, PG223, PQ240	-5, -6
XC5202	PC84, PG156, PQ100, TQ144, VQ100	-5, -6

Device	Packages	Speed Grades
XC5204	PC84, PG156, PQ100, PQ160, TQ144, VQ100	-5, -6
XC5206 ^b	PC84, PG191, PQ100, PQ160, PQ208, TQ144, VQ100	-5, -6
XC5210 ^b	BG225, PC84, PG223, PQ160, PQ208, PQ240, TQ144	-5, -6
XC5215 ^b	HQ304, PG299, PQ208, PQ240	-5, -6
XC7236A ^a	PC44	-16, -20, -25
XC7318 ^a	PC44, PQ44	-5, -7
XC7336 ^a	PC44, PQ44	-5, -7, -10, -12, -15
XC7354 ^a	PC44, PC68	-7, -10, -12, -15
XC7372 ^a	PC68, PC84, PQ100	-7, -10, -12, -15
XC7336Q ^a	PC44, PQ44, VQ44	-10, -12, -15
XC73108 ^a	BG225, PC84, PG144, PQ100, PQ160	-7, -10, -12, -15, -20
XC73144 ^a	BG225, PQ160	-7, -10, -12, -15

a. Not supported in X-BLOX.

b. Not supported in Base packages.

Known Issues

This chapter describes the known issues in this release.

Software

This section lists the workarounds for the software. They are presented in the order that they occur in the design process.

Installation

Include Environment Variables in Setup File

Platform: Workstations

Architecture: All

Design Step: Installation

Reference Number: 10564

Set the following environment variables in your setup file.

```
setenv XABELDEV $XACT/data/lib5
setenv XAPPLRESDIR $XABELDEV
setenv UIDPATH $XACT/bin/sparc/%U
```

Software Configuration

Xilinx ABEL Needs 300 KB Disk Space for Intermediate Files

Platform: All

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

If there is less than 300 KB available on the hard disk when you invoke Xilinx ABEL, it may hang while processing a design. Xilinx ABEL requires 300 KB of disk space for temporary files. This amount does not include space for design files created while running Xilinx ABEL.

Make sure there is at least 300 KB of disk space available before invoking Xilinx ABEL.

NNANSI.SYS Conflicts with Graphic Display

Platform: PC

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

The nnansi.sys driver may conflict with the Xilinx ABEL graphics display.

Use ansi.sys, not nnansi.sys, in your config.sys file.

Correct Installation of XKeysymDB File

Platform: Workstation

Architecture: All

Design Step: Software Configuration

Reference Number: 8097

If you are using the OpenLook 3 graphical user interface, installing the \$XACT/data/lib5/XKeysymDB file into /usr/lib/X11 may overwrite an existing XKeysymDB file.

If there is a /usr/lib/X11/XKeysymDB file on a machine where you intend to run Xilinx ABEL, append \$XACT/data/lib5/XKeysymDB

to that file. If it does not exist, copy from \$XACT/data/lib5/XKey-symDB to that file.

ABEL Files in \$XACT/examples/xabel/dataio Are Not Supported by Xilinx

Platform: All

Architecture: All

Design Step: Software Configuration

Reference Number: Not Available

The files located in \$XACT/examples/xabel/dataio are examples referred to in the *Xilinx ABEL Software Design Reference Manual* from Data I/O. These examples may contain certain features or devices not supported by Xilinx ABEL.

Use the designs in \$XACT/examples/xabel/designs for FPGAs or \$XACT/examples/xabel/bjxepld for EPLDs if you want to learn XABEL using example designs.

Design Entry

Use Unique State Names When Defining Multiple State Machines

Platform: All

Architecture: All

Design Step: Design Entry

Reference Number: 18866

If you are defining multiple state machines, do not use the state name from one machine as part of the next state logic of another. This usage causes ambiguities during SynthX that result in the following error:

```
Output X is multiply defined.
```

X is the name of the state. To avoid this error, declare a “dummy” node equal to the state name and use the node in the next state logic of the second state machine.

Printing to Bad Plotter Port May Cause Loss of File Edits

Platform: PC
Architecture: All
Design Step: Design Entry
Reference Number: Not Available

When you print from Xilinx ABEL, the following message appears:

```
Write fault error writing to device XXX.
```

Xilinx ABEL then exits to DOS, losing any file changes that were made.

This error may occur if the specified plotter port is not set up properly. Always save file changes before printing from Xilinx ABEL.

Not All Device Types Are Supported

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: Not Available

Xilinx ABEL does not support all of the PLDs supported by Data I/O's ABEL.

If the device type that you wish to use is not supported, alter the design to be device-independent. Refer to the "Supported Device Types" appendix of the *Xilinx ABEL User Guide* for more information.

Schematic-Based Modules Cannot Be Embedded in Behavioral Designs

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: Not Available

You cannot embed a schematic module in a behavioral design.

Rewrite the schematic modules as behavioral modules or rewrite the entire design so that the only schematic is the top level of the design.

FITEQN May Process Incorrect Pin Types If Using INCLUDE_EQN Property

Platform: All
Architecture: EPLD
Design Step: Design Entry
Reference Number: Not Available

If an included file in a multi-module design references an I/O pin signal with a .PIN extension and the top-level file does not, the signal is interpreted as an output-only pin, and the XEPLD fitter issues the following message:

```
'signal.pin' is not declared with an IOPIN statement.
```

Declare the signal as an IOPIN in a PLUSASM Property statement in the top-level file. Alternatively, you can describe the entire design in one file.

SynthX Can Sometimes Take a Long Time to Process a Xilinx Design

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: Not Available

SynthX takes a long time to process a Xilinx ABEL design.

Add a @DCSET (don't-care set) directive to the ABEL source file. This step speeds up the compilation time by allowing AHDL2X to arbitrarily assign values to don't-care terms, making it easier to minimize the logic. If the design contains a symbolic state machine, try adding the @DCSTATE (don't-care state) directive in addition to a @DCSET directive.

Pin with Invert Attribute Is Not Inverted If Used As a Feedback Signal

Platform: PC
Architecture: All
Design Step: Design Entry
Reference Number: Not Available

The Invert attribute explained in Table 4-1 and Figure 4-2 of the *Xilinx ABEL User Guide* does not function as specified. It fails to invert the signal if it is used as a feedback signal elsewhere in the design.

Do not use the Invert attribute for feedback signals. If the device already has a pin of that type, make the design device-independent.

ImproveX Takes a Long Time to Run or Runs Out of Memory

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 14773

ImproveX can take a long time to run if the ABL file contains wide arithmetic, compare functions, or combinatorial functions. These functions can also cause increased memory usage.

For wide functions (> 8 bits), try the following:

1. Insert the @carry4 directive into the ABL file. This directive instructs ImproveX to break arithmetic functions into smaller, more manageable pieces.
2. Break up large functions into smaller functions using temporary nodes.

Instead of this:

```
X = [a7..a0] == [b7..b0];
```

use the following:

```
temp = [a7..a4] == [b7..b4]; (declare "temp" as node)  
X = temp & ([a3..a0] == [b3..b0]);
```

Also, try using the Xilinx Property Savesig statement on the temporary nodes. It prevents them from being collapsed. If run time is still a problem, turn the Use All Available Memory switch off in XABEL.

Note: Synthesized combinational logic functions may not be practical for some large arithmetic functions. Consider designing specialized logic, especially for adders, multiplexers, and comparators.

Xilinx Property Statements Cannot Span More Than One Line

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: Not Available

Unpredictable results occur if the Xilinx Property statement is not completely specified on one line.

Do not use multiple lines when using Xilinx Property statements. Here is an example that uses this statement correctly:

```
xilinx property 'initialstate state_0';
```

Registered Outputs Must Be Declared As Type 'Reg'

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 12296, 13410, 15113

Due to better syntax checking, Xilinx ABEL now requires explicit pin declarations. Previously, if an output was simply declared to be of type pin, and the design description contained a *pin.FB* reference or *pin.clk* assignment, Xilinx ABEL would synthesize the output using a register.

Declare registered outputs with the following syntax:

```
signal pin istype 'reg';
```

or

```
signal pin istype 'reg, invert';
```

ABL2XNF's Unspecified_state Option Only Applies to Symbolic State Machines

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 9787, 10704

You can use the `Unspecified_state` option to tell ABL2XNF how to implement non-specified state transitions. This option does not apply to encoded state machines. Neither does the Xilinx Property Initial-state statement.

Fully specify encoded state machines by adding Else clauses, specifying all possible input conditions, and making sure that the machine goes to the correct initial state upon powerup.

PLASimX does not recognize the `Unspecified_state` option, so if you use this option to complete an incompletely specified state machine automatically, PLASimX still treats it as an incompletely specified state machine, even though the XNF file generated by XABEL is a completely specified machine. Therefore, generate your PLASimX test vectors as if the machine were incompletely specified.

Pin Number Assignment Does Not Work for PGA and BGA Packages

Platform: All
Architecture: EPLD
Design Step: Design Entry
Reference Number: 13754

Xilinx ABEL only takes numerical pin numbers and does not accept the alphanumeric pin names needed on PGA and BGA packages when you create a stand-alone design with EPLDs and you assign pin numbers to signals in the ABL file.

Use PLUSASM Property statements to declare the pin types and pin numbers.

XABEL Cannot Write to the Root Directory with an Absolute Path Name

Platform: PC
Architecture: ALL
Design step: Design Entry
Reference Number: 2405

If you specify "c:\design.abl" when using the File → Save As option, XABEL issues the following message:

```
Directory "c:\" not found
```

Either specify a relative path name when using the File → Save As option, or do not write files to the root directory.

AHDL2X Does Not FFlag Syntax Error for If-Then Construct with No Else

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 4189

If you specify an If-Then clause and do not terminate it with an Else statement or a semicolon, AHDL2X does not flag an error, and SynthX may not generate the logic that you intended, for example:

```
state_one : if input_a then state_two <-- add either
              a ";", or an "ELSE"

              if input_b then state_three
              else state_one;
```

Add either an Else clause, or use a semicolon to terminate the If-Then statement.

Always use an Else clause in such statements to ensure that only one state is active at a time; otherwise, two If clauses may happen to be "true" at the same time, causing indeterminate behavior.

SymGen Does Not Pass DEF=XABEL, FILE=, or PLD= Parameters to OrCAD Symbols

Platform: All
Architecture: All
Design Step: Design Entry
Reference number: 13188, 15992

The current release of OrCAD cannot support the DEF=XABEL or FILE= parameters on the symbol itself.

After placing the SymGen symbols on your schematic, add the appropriate attributes to each instance.

SymGen Produces an Incorrect SMR File for Symbols with Bused Pins

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 15450

If the input XSF file has PIN records with buses, SymGen produces an SMR file with single-bit pins instead of bused pins. This only happens with user-created XSF files, because the "<>" bus pin characters are illegal in Xilinx ABEL. Xilinx ABEL does not output an XSF file with bused pin records. The symbol that is output for schematic entry, however, is accurate.

When Run Under XDM, SymGen Can Hang If an Error Is Encountered

Platform: Workstation
Architecture: All
Design Step: Design Entry
Reference Number: 14656

When you run SymGen from XDM on a workstation with the -v option, it may appear to hang if it encounters an error and enters interactive mode, requiring your input. The message from SymGen is not printed in the display window, yet SymGen is waiting for a response.

Terminate SymGen's execution by using Ctrl-C, then run SymGen from the command line outside of XDM.

Do Not Use Upper-Case File or Module Names for EPLD Designs on Non-PC Platforms

Platform: All
Architecture: EPLD
Design Step: Design Entry
Reference Number: Not Available

AHDL2X converts all output file names to lower case. Since ABL2PLD is case-sensitive, it cannot find the expected upper-case output files for AHDL2X. This problem does not apply to FPGAs, since ABL2XNF is not case-sensitive.

Use only lower-case file names for EPLD designs.

Translation to XNF

External Inputs Should Source Logic

Platform: All
Architecture: All
Design Step: Translation to XNF
Reference Number: 19715

Declaring logic using nodes and not associating it with an input signal may cause a memory or segmentation fault when SynthX is run. Make sure all of your logic is sourced by external inputs.

Part List Does Not Contain All Valid Part Types

Platform: All
Architecture: XC7000, XC4000, XC2000
Design Step: Translation to XNF
Reference Number: 11325, 14414, 16117

The following part types are missing from the part list in the Xilinx FPGA Options and Xilinx EPLD Options dialog boxes:

2018XX-33
4005HXX-X
7318PC44

If your specific part type is missing from the list, simply type it into the Part Type field manually instead of selecting the part type with the mouse.

No Help for Error Numbers 00XX

Platform: All
Architecture: All
Design Step: Translation to XNF
Reference Number: 11043

Error numbers 00XX are system errors and are not included in the on-line help for errors. In particular, error 0034 signifies an unsupported device type.

Comment out the device in the ABL source file. Enable the Auto-Make option and re-compile the design. The Compiler Listing is then up to date with the ABL source file.

Possible Binding Mismatch Using Mentor Symbols with Buses

Platform: All
Architecture: All
Design Step: Translation to XNF
Reference Number: 12616

When you use Mentor to generate a symbol with a bus, Mentor uses the <> characters in the bus name. These characters are illegal in Xilinx ABEL and cannot be used as part of a signal name. Using them can cause a binding mismatch error from XNFMerge.

Edit the XNF file after running Xilinx ABEL to add the <> characters to the bus pins, or do not create Mentor symbols with buses.

BLIFOPTX Can Take Very Long Run Times

Platform: All
Architecture: All
Design Step: Translation to XNF
Reference Number: 11662

BLIFOPTX reduces logic such that each signal has the minimum number of terms possible. This reduction can cause extremely long run times for some designs.

For EPLD designs, turn off the logic reduction in the Xilinx EPLD Options menu.

For FPGA designs, turn off the Pre-Synthesis Logic Reduction option in the Xilinx FPGA Options menu. These steps keep BLIFOPTX from reducing the design.

BLIFOPTX May Crash on a Single Fully Specified Truth Table

Platform: All
Architecture: All
Design Step: Translation to XNF
Reference Number: Not available

If a design is written with a single fully specified truth table and no equations or state machines, BLIFOPTX may crash. BLIFOPTX, an optimization tool, will find nothing to optimize in a truth table without don't-cares. It may become confused and crash. If this occurs, copy the BL0 file to a file of the same name with a .bl1 extension. Continue the process by running SynthX on the BL1 file.

Documentation

This section lists the corrections to the documentation.

Xilinx ABEL User Guide

SymGen in Windows Is Undocumented

Platform: All
Architecture: All
Design Step: Design Entry
Reference Number: 10818

The *Xilinx ABEL User Guide* does not document how to use SymGen in Windows to create a symbol for Xilinx ABEL modules. This documentation follows.

The SymWin (SymGen for Windows) program automates the creation of symbols for Xilinx ABEL modules. It uses as input an XSF file created by ABL2XNF. The XSF file contains the pinout for the symbol. SymWin uses this file to generate an appropriate symbol.

1. Invoke the Symbol Generation Utility by clicking on the Symbol Generation Utility icon in the Program Manager XACTstep program group. (The program name is symwin.exe.)

The Symbol Generator dialog box appears, as shown in Figure 4-1.

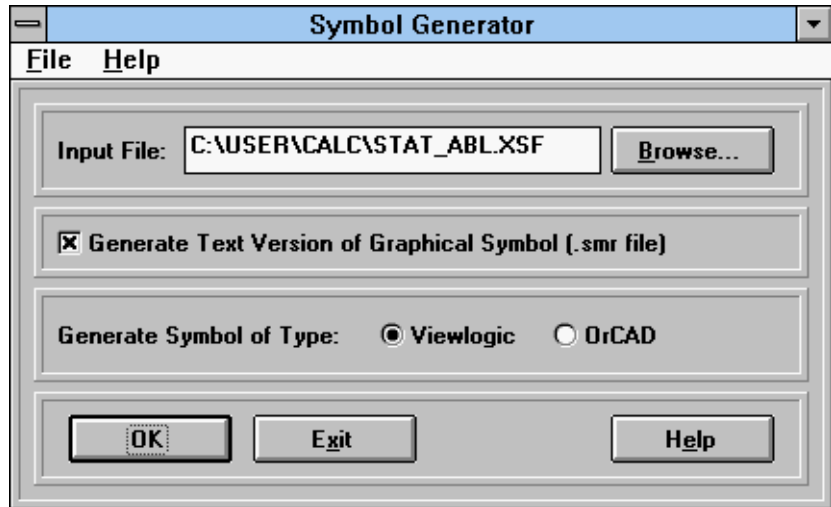


Figure 4-1 Symbol Generator Dialog Box

2. Using the Browse button, go to the design directory, select the STAT_ABL.xsf file, and press OK.
3. Select **Viewlogic** or **OrCAD**, as appropriate, in the Generate Symbol of Type field. Viewlogic is the default.
4. Press the OK button.
5. After SymWin finishes creating the symbol, a report is displayed in the SymGen Results window.
6. After viewing the report, press any key to close the SymGen Results window.
7. Click on **Exit** to close the Symbol Generator dialog box.

SymWin creates a Viewlogic symbol file called stat_abl.1 and places it in the sym directory.

SynthX Mapped_XNF Option Is Now Create_Mapped_XNF

Platform: All

Architecture: All

Design Step: Design Entry

Reference Number: 10819

The Mapped_XNF option in SynthX, documented on page 6-42, is now called the Create_Mapped_XNF option.

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