

TMS320C6201

Test and Evaluation Board

Technical Reference

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About This Manual

This manual describes the operation of the TMS320C6201 ('C6201) test and evaluation board (TEB). The 'C6201 TEB is a low-cost desktop card that helps you evaluate certain characteristics of the 'C6201 digital signal processor (DSP) to determine if the DSP meets your application requirements. You can create your software to run on the board and expand the system using the prototype area.

This manual tells you how to install and operate the 'C6201 TEB with your system. It also describes key features of the TEB and helps you understand the TEB's key components.

How to Use This Manual

This book contains the following types of information:

- ☐ **Introductory material**, consisting of Chapters 1 and 2. Chapter 1 provides an overview of the 'C6201 TEB and its components. Chapter 2 tells you how to install the TEB.
- ☐ **Topical material**, consisting of Chapter 3, provides descriptions of hardware functions.
- ☐ **Reference material**, consisting of Appendixes A and B, provides PAL[®] code and schematics.

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This document uses the following conventions.

- ☐ Program listings, program examples, and interactive displays are shown in a special typeface.
- ☐ Device names are abbreviated with a C, followed by the last two to four alphanumeric characters in the name. For example, TMS320C6x is written as 'C6x and TMS320C6201 is written as 'C6201.

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This is an example of a caution statement.
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Related Documentation

You can use the following book to supplement this user's guide:

Programming Atmel's AT29 Flash Family, Flash Application Note (AN-3)
(Atmel literature number 0518B)

Related Documentation From Texas Instruments

The following books describe the 'C6x devices and related support tools. To obtain a copy of any of these TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924. When ordering, please identify the book by its title and literature number.

XDS51x Emulator Installation Guide (literature number SPNU070) describes the installation of the XDS510™, XDS510PP™, and XDS510WS™ emulator controllers. The installation of the XDS511™ emulator is also described.

JTAG/MPSD Emulation Technical Reference (literature number SPDU079) provides the design requirements of the XDS510™ emulator controller, discusses JTAG designs (based on the IEEE 1149.1 standard), and modular port scan device (MPSD) designs.

TMS320C6x C Source Debugger User's Guide (literature number SPRU188) tells you how to invoke the 'C6x simulator and emulator versions of the C source debugger interface. This book discusses various aspects of the debugger, including command entry, code execution, data management, breakpoints, profiling, and analysis.

TMS320C6x C Source Debugger User's Guide (for SPARCstations)

(literature number SPRU224) tells you how to invoke the 'C6x simulator and emulator versions of the C source debugger interface for SPARCstations. This book discusses various aspects of the debugger, including command entry, code execution, data management, breakpoints, profiling, and analysis.

TMS320C62xx Technical Brief (literature number SPRU197) gives an introduction to the 'C62xx digital signal processor, development tools, and third-party support.

TMS320C6201 Digital Signal Processor Data Sheet (literature number SPRS051) describes the features of the TMS320C6xx and provides pinouts, electrical specifications, and timings for the device.

TMS320C62xx Peripherals Reference Guide (literature number SPRU190) describes common peripherals available on the TMS320C62xx digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.

TMS320C62xx CPU and Instruction Set Reference Guide (literature number SPRU189) describes the 'C62xx CPU architecture, instruction set, pipeline, and interrupts for the TMS320C62xx digital signal processors.

TMS320C62xx Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code and includes application program examples.

TMS320C6x Optimizing C Compiler User's Guide (literature number SPRU187) describes the 'C6x C compiler. This C compiler accepts ANSI standard C source code and produces assembly language source code for the 'C6x generation of devices. This book also describes the assembly optimizer, which helps you optimize your assembly code.

TMS320C6x Assembly Language Tools User's Guide (literature number SPRU186) describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the 'C6x generation of devices.

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Overview of the TMS320C6201 Test and Evaluation Board

The TMS320C6201 test and evaluation board (TEB) helps you evaluate certain characteristics of the TMS320C6201 ('C6201) fixed-point digital signal processor (DSP) to ensure that it meets your application requirements. The TEB is self-contained, only requiring connections to an AC power supply and to your own emulation hardware and software. The TEB is platform independent and uses either an XDS510™ emulator controller for a PC™ or an XDS510WS™ emulator controller for a UNIX™ workstation.

The 'C6201 TEB carries a 'C6201 DSP on board to allow full-speed verification of 'C6201 code. You can also use the TEB to design your own prototype systems. The 'C6201 DSP has 128 Kbyte on-chip SRAM that consists of 64 Kbyte internal program/cache and 64 Kbyte internal data memory. The TEB uses the 'C6201's 32-bit external memory interface to facilitate accesses to on-board synchronous and asynchronous memories. A PC or UNIX windows-oriented debugger simplifies code development and debugging. For more information about the debugger, see the *TMS320C6201 C Source Debugger User's Guide* or the *TMS320C6x C Source Debugger User's Guide for SPARCStation*.

The TEB also has a 'C6201 16-bit host access port, a serial and timer access port, an IEEE Standard 1149.1-compliant JTAG connector for accessing the 'C6201's scan-based emulation features, and a through-hole area for design prototyping. You can also use the TEB as a reference when designing your own systems.

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1.2 Functional Overview of the TMS320C6201 TEB	1-3

1.1 Key Features of the TMS320C6201 TEB

The 'C6201 TEB has the following features:

- ☐ 'C6201 capable of executing 1600 million instructions per second (MIPS)
- ☐ Varied instruction cycle times of the 'C6201:
 - 5-ns instruction cycle time when using the DSP's internal memories
 - 6-ns instruction cycle time when using synchronous dynamic RAM (SDRAM) and one-half rate external synchronous burst static RAM (SBSRAM)
 - 6.7-ns instruction cycle time when using the TEB's external SBSRAM, regardless of which other TEB memories are used
- ☐ 512K bytes 6.7-ns SBSRAM
- ☐ 8M bytes 12-ns SDRAM
- ☐ 256K bytes 12-ns asynchronous static RAM (ASRAM)
- ☐ 128K bytes 200-ns flash programmable erasable ROM (PEROM)
- ☐ 16-bit host port header
- ☐ Access to the 'C6201's serial ports and timers via a header
- ☐ Emulator connector
- ☐ Prototyping area

1.2 Functional Overview of the TMS320C6201 TEB

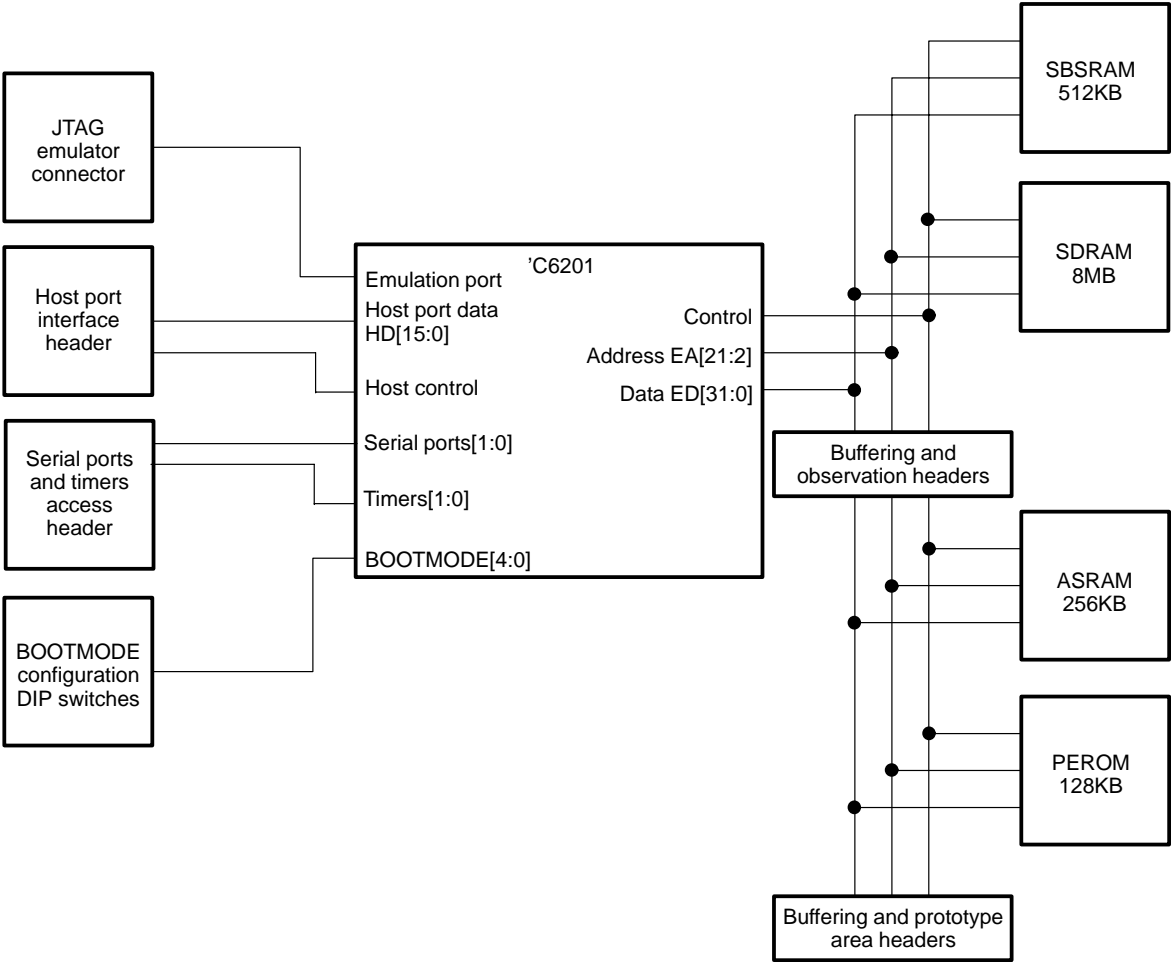
Figure 1–1 shows the basic block diagram and interconnects of the 'C6201 TEB. The interconnects include the external memory, host port, emulation interfaces, and serial ports and timers.

The 'C6201 DSP interfaces to the memories through a 32-bit data bus. Headers are situated between the synchronous and asynchronous memories to allow easy examination of the external memory interface's address, data, and control signals. The TEB's control signals are also available at these headers. Additional headers between the asynchronous memories and the prototyping area allow for access to asynchronous control signals and the data bus, which may be used in the prototyping area.

Use the host port header to connect your host processor to the 'C6201's host port interface. This allows your host processor to access the 'C6201's internal memory. The serial ports and timers header allows access to the 'C6201's serial ports and timers.

An emulation connector provides access to the IEEE Standard 1149.1 (JTAG) scan-based emulation port of the 'C6201. This port is a superset of the IEEE 1149.1 standard and is used by either an XDS510 or an XDS510WS emulator.

Figure 1–1. TMS320C6201 TEB Connectivity



Installing the TMS320C6201 Test and Evaluation Board

This chapter provides installation instructions for the 'C6201 TEB.

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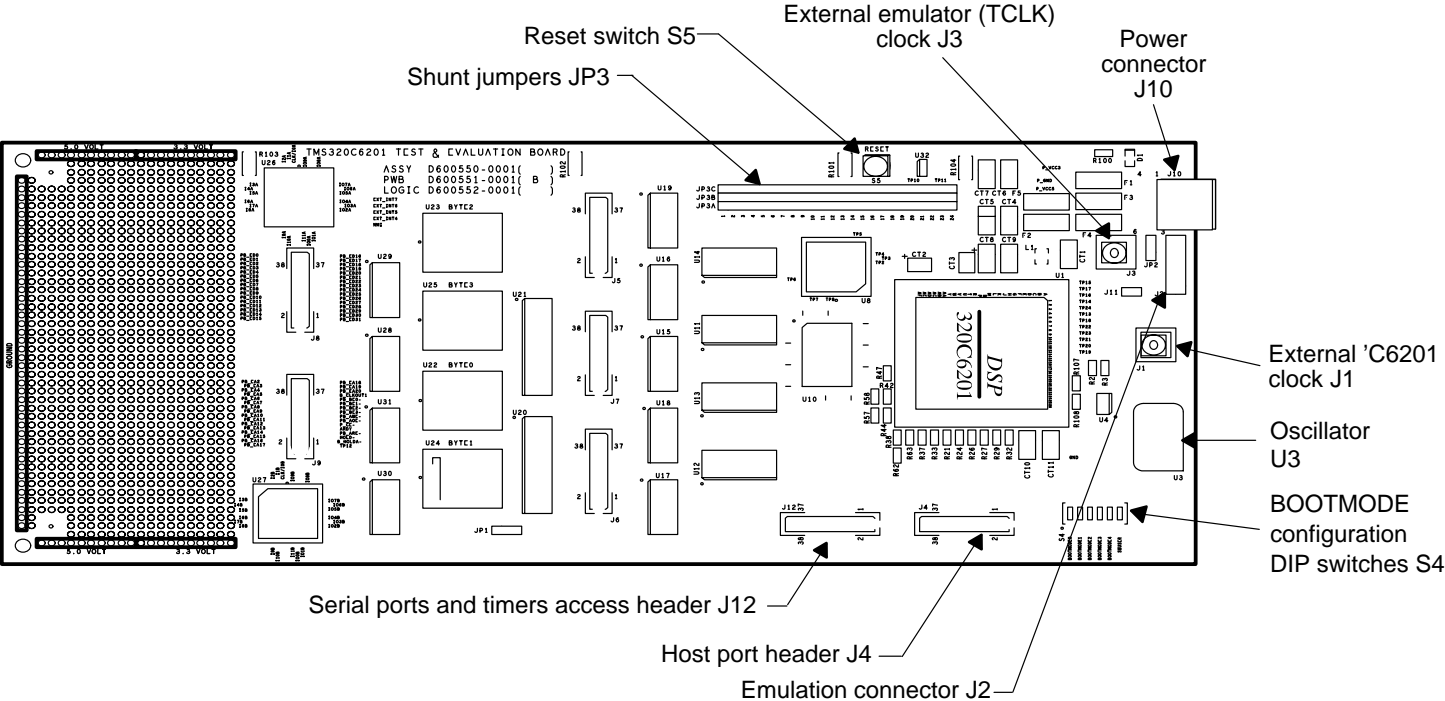
2.1 The TMS320C6201 TEB

The 'C6201 TEB is 5 inches x 12 inches and is intended for desktop use. It meets the following specifications:

- ☐ Instruction cycles of 7.5 ns (frequency equal to 133 MHz). This is accomplished using a 33.25-MHz oscillator and operating the 'C6201's phase-locked loop (PLL) clock in multiply-by-four mode.
- ☐ Configuration of the 'C6201 boot process using the TEB's on-board DIP switches. These switches are set for the following:
 - Use of the 'C6201's memory map 1
 - Memory at address 0 is 'C6201 internal RAM
 - Boot-load startup process using 8-bit PEROM with default timing in CE1 external address space
- ☐ Use of the emulator's TCLK signal

Figure 2–1 shows the layout of the 'C6201 TEB.

Figure 2–1. TMS320C6201 TEB



2.2 Host Requirements

The TEB is platform independent and can be used with an XDS510 emulator controller for a PC or an XDS510WS emulator controller for a UNIX workstation. The *XDS51x Emulator Installation Guide* lists the minimum hardware requirements for your emulator. The installation instructions included with your emulator software lists the minimum software requirements for your emulator.

2.3 TMS320C6201 TEB Kit Components

The kit contains the following items:

- ☐ 'C6201 TEB
- ☐ Custom power supply
- ☐ *TMS320C6201 Test and Evaluation Board Technical Reference* (this document)
- ☐ Diskette containing TEB-related files

2.4 TMS320C6201 TEB Connection

Before you apply power to the TEB or connect the TEB to your emulator, see Table 2–1 and Table 2–2 to ensure that all shunt jumpers and DIP switches are set to their default positions. Table 3–3 and Table 3–4 contain complete descriptions of all shunt jumpers and DIP switches used on the TEB. See these tables before you change any default settings.

Table 2–1. Default TEB Shunt Jumper Settings*A–B indicates HIGH (1), B–C indicates LOW (0)*

Name	Position	Setting	Description
ROM protect	JP1	1–2	Flash PEROM write disabled
TCLK select	JP2	2–3	Use XDS51x emulator's TCLK signal
NMI	JP3.1	B–C	Nonmaskable interrupt inactive
EXT_INT4	JP3.2	B–C	Interrupts EXT_INT4—EXT_INT7 inactive
EXT_INT5	JP3.3	B–C	
EXT_INT6	JP3.4	B–C	
EXT_INT7	JP3.5	B–C	
PLLFREQ1	JP3.6	B–C	25 MHz < CLKOUT1 ≤ 135 MHz
PLLFREQ2	JP3.7	B–C	
PLLFREQ3	JP3.8	B–C	
CLKMODE0	JP3.9	A–B	PLL multiply-by-four mode
CLKMODE1	JP3.10	A–B	
RSV0	JP3.11	A–B	Reserved
RSV1	JP3.12	A–B	
RSV2	JP3.13	A–B	
RSV3	JP3.14	A–B	
RSV4	JP3.15	B–C	
EMU0	JP3.16	A–B	TI emulation support
EMU1	JP3.17	A–B	
LENDIAN	JP3.18	A–B	Little-endian mode addressing
ARDY	JP3.19	A–B	External controller ready (to avoid stalling)
HOLD–	JP3.20	A–B	Connects 'C6201 to the system
Unused	JP3.21	No Shunt	
Unused	JP3.22	No Shunt	
TINP0	JP3.23	A–B	Timer inputs
TINP1	JP3.24	A–B	

*Table 2–2. Default TEB DIP Switch Settings**OFF indicates HIGH (1), ON indicates LOW (0)*

Name	Position	Setting	Description
BOOTMODE0	S4.1	OFF	Boot configuration settings for memory map 1 with internal RAM at address 0 and 8-bit PEROM boot process
BOOTMODE1	S4.2	ON	
BOOTMODE2	S4.3	OFF	
BOOTMODE3	S4.4	OFF	
BOOTMODE4	S4.5	ON	
SWUSER	S4.6	OFF	User-defined input to U8 PAL [®]

2.5 TMS320C6201 TEB Installation

The 'C6201 TEB is connected to a power supply and an emulator. The following steps show how to connect the TEB to both.

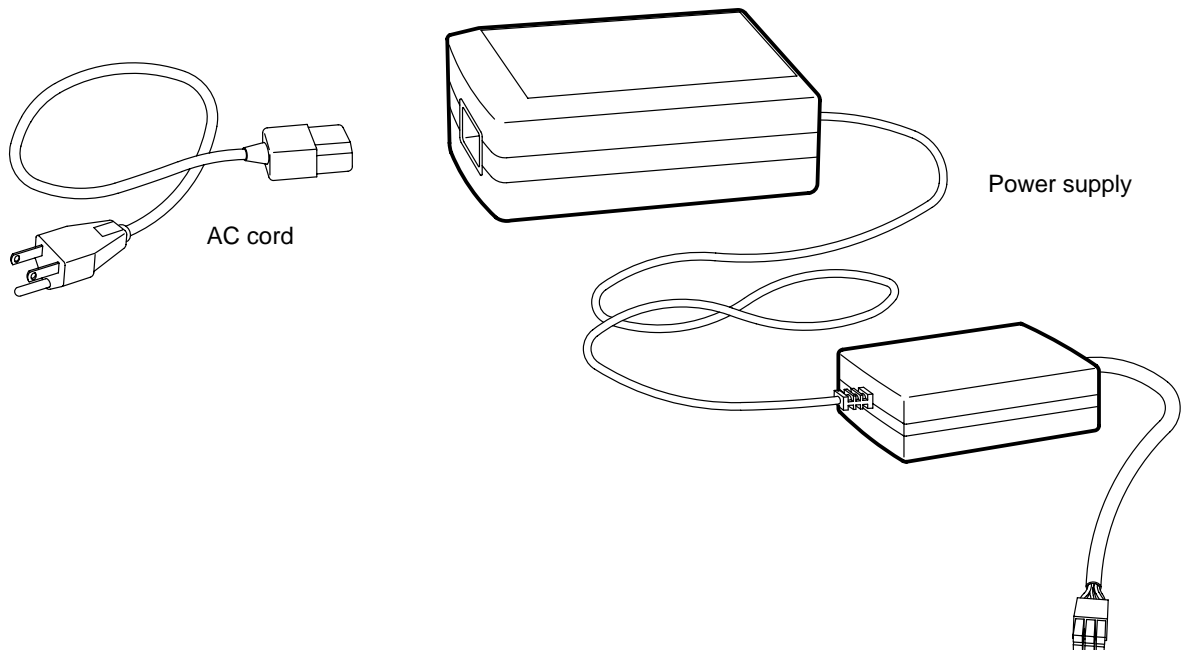
Never disconnect or reconnect any cables or other hardware devices while power is applied to the emulator or TEB. Doing so can cause damage to your emulator and/or TEB.

Step 1: Install your emulation hardware and software.

Step 2: Ensure the emulator power is off. If you have an XDS510WS emulator controller (for a UNIX workstation), switch off the power. If you have an XDS510 emulator controller (for a PC), power down the emulator by shutting down Windows and turning off your PC.

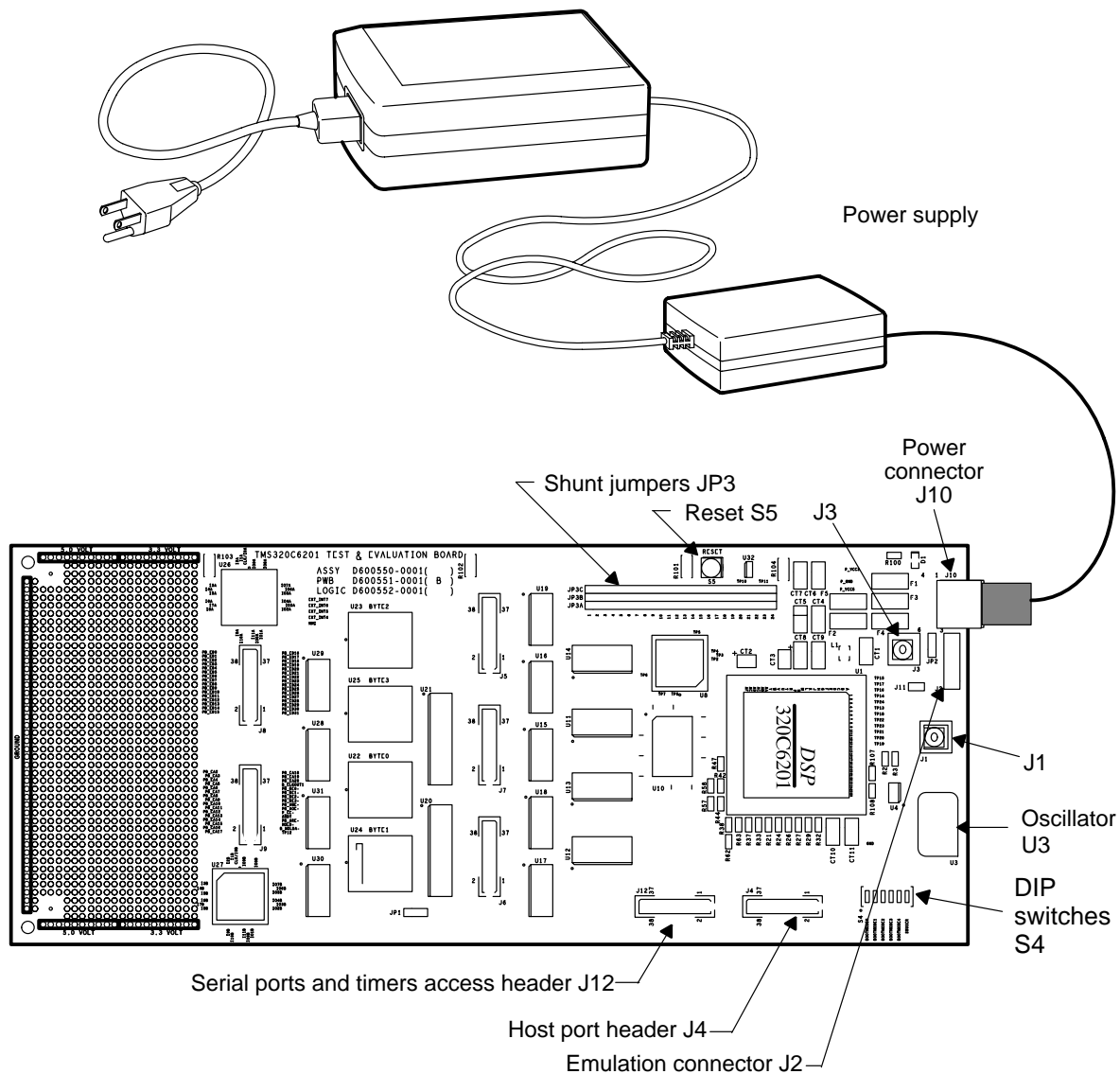
Step 3: Insert the female end of the AC line cord into the power supply.

Figure 2–2. Attaching AC Cord Into Power Supply



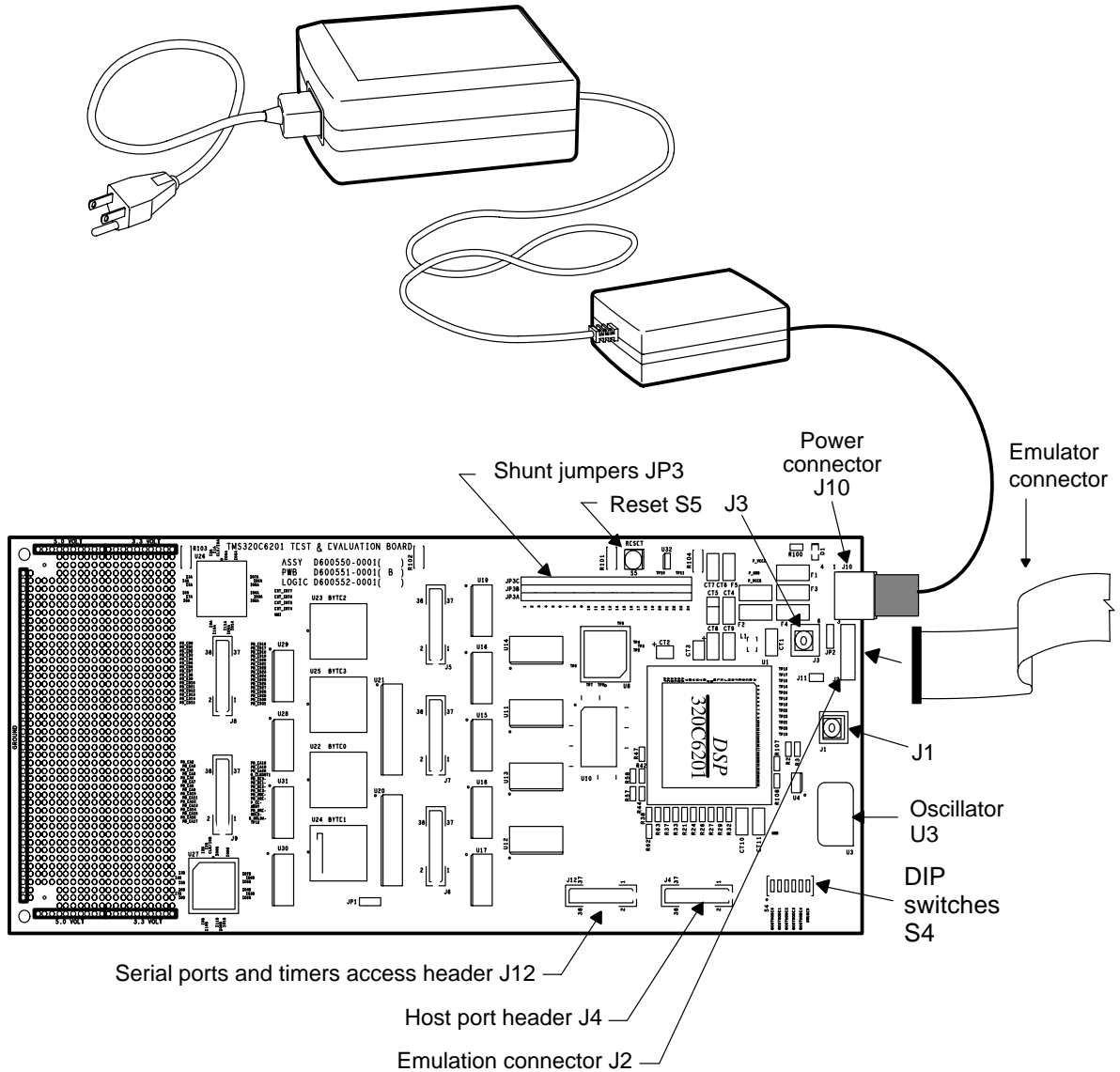
Step 4: Connect the power supply's male 6-pin connector into J10 of the TEB.

Figure 2–3. Connecting the Power Supply to the TEB



Step 5: With moderate downward pressure, connect the 14-pin keyed connector from your emulator to J2 on the TEB.

Figure 2–4. Connecting the Emulator to the TEB



Step 6: Turn on power to the emulator. If you have an XDS510WS emulator controller (for a UNIX workstation), switch on the power. If you have an XDS510 emulator controller (for a PC), turn on your PC.

Step 7: Plug the male end of the power supply's AC line cord into an AC outlet. This applies power to the TEB. An LED on the power supply and one on the TEB indicates that power is applied.

If you need to disconnect the TEB, unplug the TEB, then turn off power to the emulator (using the power switch if you have an XDS510WS or by shutting down Windows and turning off your PC if you have an XDS510).

TMS320C6201 Test and Evaluation Board Operation

This chapter describes the 'C6201 TEB, its key components, and how they operate. It also provides additional information on the TEB's various interfaces.

The 'C6201 TEB consists of the following components:

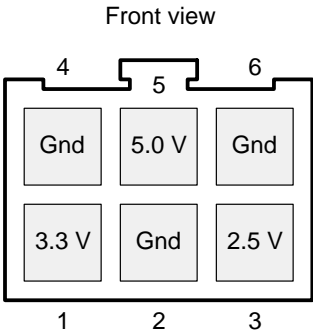
- ☐ Custom power supply
- ☐ TMS320C6201 TEB
 - Memory control
 - Power
 - Reset generation
 - Clock generation
 - Interrupt generation
 - 'C6201 external memory interface
 - 'C6201 host port interface
 - Serial ports and timers interface
 - Emulation interface
 - Prototyping area
 - Shunt jumpers and DIP switches
- ☐ 3.5-in floppy diskette

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3.1 Custom Power Supply

A custom power supply provides 2.5-, 3.3-, and 5.0- V_{DC} regulated supply voltages to the TEB when connected to an AC wall outlet. An LED on top of the power supply illuminates when it has been properly connected to AC power. The LED blinks when the power supply is connected to a wall outlet where the DC outlet is not connected to the TEB. The TEB's power supply must be loaded to regulate the voltages measured at its DC outlet. Voltages at the DC outlet without the load of the TEB appear unstable.

Figure 3–1. Power Supply DC Connector



3.2 Power Requirements

LED D1 (located next to the power jack on the TEB) illuminates when power is applied to the 6-pin DC power jack J10. See Figure 2–4 for details about applying power to the TEB. Table 3–1 lists the appropriate fuse current ratings to protect the TEB components.

Table 3–1. TEB Fuse Ratings

Voltage	Label	Schematic reference designation	Rating	Purpose of Supply Voltage
2.5	V _{CC2}	F2	7.0 A	'C6201 internals
3.3	V _{CC3}	F1	4.0 A	'C6201 I/Os and TEB 3.3-V components
3.3	P_V _{CC3}	F5	0.75 A	Prototype area 3.3-V components
5.0	V _{CC5}	F3	0.25 A	TEB 5.0-V components
5.0	P_V _{CC5}	F4	1.5 A	Prototype area 5.0-V components

Use only fuses with ratings listed in Table 3–1 to avoid damage to the TEB.

Do not draw more current than allowed by the fuses. This can damage the power supply and the TEB.

3.3 Reset Generation

At power up, power down, and during brownout conditions, a supply voltage supervisory circuit forces the 'C6201 DSP into a reset condition. Pressing the push-button switch S5 also forces a reset. In either case, the 'C6201's reset line is active (low) for a period of at least 200 ms.

3.4 Clock Generation

The 'C6201 DSP operates at frequencies up to 200 MHz. Two options for generation of the clock signal CLKIN are provided on the TEB.

- ☐ A 68- Ω resistor installed in location R2 selects oscillator U3.
- ☐ Removing R2 and installing it as R3 selects the SMA connector J1 as the source for the CLKIN signal.

These options, combined with the 'C6201's internal phase-locked loop (PLL), allow you to experiment with different clock frequencies. Use of the PLL in the multiply-by-four mode for a CLKOUT1 frequency other than 133 MHz requires the replacement of components R1, C2, and C3. See the *TMS320C6201 Digital Signal Processor Data Sheet* for more information.

The factory default configuration of the TEB uses a 33.25-MHz oscillator to provide input to the 'C6201's PLL, which is set to operate in multiply-by-four mode. R2 is installed to select U3 as the source for the 'C6201's PLL. Shunt jumpers JP3.10 (CLKMODE1) and JP3.9 (CLKMODE0) select the clock multiply-by-four mode. Shunt jumpers JP3.8 (PLLREQ3)–JP3.6 (PLLREQ1) select a CLKOUT1 frequency range of 25–135 MHz. The oscillator and the PLL provide a CLKOUT1 signal that has a period of approximately 7.5 ns, a frequency of 133 MHz, and a duty cycle of approximately 50%.

You can operate the 'C6201 internally at frequencies up to 200 MHz by reconfiguring shunt jumpers JP3.10–JP3.6 and replacing the CLKIN source. You must also replace oscillator U3 with a different frequency 5.0-V oscillator. You can use SMA connector J1 by removing and installing the 68 Ω resistor R2 in the location of R3. When changing frequencies, see the *TMS320C6201 Digital Signal Processor Data Sheet* to achieve optimal performance for your desired configuration of the TEB.

3.5 Interrupt Generation

Pressing the push-button switch S5 generates a manual reset of the 'C6201. Shunt jumpers JP3.1 (NMI) and JP3.2 (EXT_INT4)–JP3.5 (EXT_INT7) pull the 'C6201's external interrupts up or down. The factory default shunt jumper settings must be pulled low because these interrupts are rising-edge sensitive.

Figure 2–1, page 2-3, shows solder connections for the interrupts at the upper right of the prototype area, to the right of U26. You must remove the appropriate interrupt shunt jumper(s) to control these interrupts with non-TEB circuitry (for example, prototype circuitry).

3.6 External Memories

The TEB provides four different types of memory for program execution and data storage. The TEB's memory types, their speeds and organizations, and the selected 'C6201 chip enable signal are listed in Table 3–2:

Table 3–2. TEB Memories

Memory Type	Designation	Timing (ns)	Organization	Total	'C6201 CE
SBSRAM	U10	6.7	128KB x 32 bits	512KB	CE2
SDRAM	U11–U14	12	2MB x 8 bits	8MB	CE0
ASRAM	U20–U21	12	64KB x 16 bits	256KB	CE3
ROM	U22–U25	200	32KB x 8 bits	128KB	CE1

See the *TMS320C6201 Digital Signal Processor Data Sheet* for a description of the chip enable signals and the processor memory map.

3.7 Host Port Connection

Header J4 connects to the TEB and an off-board (user supplied and programmed) host. The header is an AMP 2–767004–2 and the mating connector part number is AMP 767003–9.

3.8 Serial Ports and Timers Connection

Header J12 allows access to the 'C6201's serial ports and timers. The header is an AMP 2–767004–2 and the mating connector part number is AMP 767003–9.

Note:

Timer input 0 (TINP0) and timer input 1 (TINP1) are pulled high by the factory default configuration of shunt jumpers JP3.23 and JP3.24, respectively.

3.9 Emulation Port Connection

Emulation connector J2 connects the 'C6201's emulation port and either the XDS510 or XDS510WS emulator. Shunt jumpers JP3.16 and JP3.17 pull the EMU0 and EMU1 signal up or down. The factory default configuration causes these signals to be pulled up. For more information about emulation signals, see the *JTAG/MPSD Emulation Technical Reference*.

SMA connector J3 allows you to provide an alternative TCK signal. To use the alternative TCK signal, shunt jumper JP2 must be moved from its factory default position to connect pins 1 and 2.

3.10 Prototyping Area

Figure 2–1 shows the through-hole area for prototyping located at the left end of the TEB. This area includes two sockets for user-programmable 3.3- V_{dc} 22V10 PAL[®] devices (U26 and U27). Fused 3.3- V_{dc} (P_{VCC3}) and 5.0- V_{dc} (P_{VCC5}) supply connections are provided at both the top and bottom edges of the prototyping area. Fuses protect against attempts to draw more current than is allowed by the power supply's design. Ground connections are provided at the extreme left end of the prototyping area.

Connectors J8 and J9 provide connectivity to the 'C6201's external memory interface's data, address, and control busses. These 32-bit connectors provide a direct connection with the modern test equipment cables. (The header part number is AMP 2–767004–2 and the mating connector part number is AMP 767003–9.) All 32 bits of data are available at J8. Only 19 bits of address are available at J9 because the TEB's prototyping area shares the 'C6201's external address space CE1 with the on-board PEROM. Consequently, only asynchronous devices may be interfaced to J8 and J9. PAL[®] U8 logic equations (Appendix A) control buffers between the asynchronous memory portion of the TEB and the TEB's prototyping area.

The 'C6201's external interrupts are available as test points NMI and EXT_INT4–EXT_INT7. See section 3.5, *Interrupt Generation*, for details about the use of these test points.

Use only fuses with ratings given in Table 3–1 to avoid damage to the TEB.

Do not draw more current than allowed by the fuses. This can damage the power supply and the TEB.

3.11 Shunt Jumpers and DIP Switches

You can configure the on-board 'C6201 and TEB devices by changing the settings of shunt jumpers and DIP switches described in Table 3–3 and Table 3–4.

Table 3–3. TEB Shunt Jumpers

Name	Position	Description																
ROM protect	JP1	Write protects Flash PEROM 1–2 Writes disabled 2–3 Writes enabled																
TCLK select	JP2	Selects JTAG clock 1–2 SMA connector (J3) 2–3 Emulation connector (J2)																
NMI	JP3.1	Nonmaskable interrupt A–B Active B–C Inactive NONE Controlled by other logic (prototyping area)																
EXT_INT4	JP3.2	External interrupts: edge-driven (rising edge) A–B Active B–C Inactive NONE Controlled by other logic (prototyping area)																
EXT_INT5	JP3.3																	
EXT_INT6	JP3.4																	
EXT_INT7	JP3.5																	
PLLFREQ1	JP3.6	Selects one of three frequency ranges for the 'C6201 CLKOUT1 signal																
PLLFREQ2	JP3.7																	
PLLFREQ3	JP3.8																	
		<table><tr><th>JP3.8</th><th>JP3.7</th><th>JP3.6</th><th>Frequency Range</th></tr><tr><td>B–C</td><td>B–C</td><td>B–C</td><td>25–135 MHz</td></tr><tr><td>B–C</td><td>B–C</td><td>A–B</td><td>35–160 MHz</td></tr><tr><td>B–C</td><td>A–B</td><td>B–C</td><td>40–200 MHz</td></tr></table>	JP3.8	JP3.7	JP3.6	Frequency Range	B–C	B–C	B–C	25–135 MHz	B–C	B–C	A–B	35–160 MHz	B–C	A–B	B–C	40–200 MHz
JP3.8	JP3.7	JP3.6	Frequency Range															
B–C	B–C	B–C	25–135 MHz															
B–C	B–C	A–B	35–160 MHz															
B–C	A–B	B–C	40–200 MHz															
CLKMODE0	JP3.9	Clock mode select. Selects the multiplication factor of the input clock frequency. CLKOUT1 is 1x or 4x CLKIN:																
CLKMODE1	JP3.10																	
		<table><tr><th>JP3.10</th><th>JP3.9</th><th>Clock Mode</th></tr><tr><td>B–C</td><td>B–C</td><td>PLL multiply-by-one mode</td></tr><tr><td>B–C</td><td>A–B</td><td>Reserved</td></tr><tr><td>A–B</td><td>B–C</td><td>Reserved</td></tr><tr><td>A–B</td><td>A–B</td><td>PLL multiply-by-four mode</td></tr></table>	JP3.10	JP3.9	Clock Mode	B–C	B–C	PLL multiply-by-one mode	B–C	A–B	Reserved	A–B	B–C	Reserved	A–B	A–B	PLL multiply-by-four mode	
JP3.10	JP3.9	Clock Mode																
B–C	B–C	PLL multiply-by-one mode																
B–C	A–B	Reserved																
A–B	B–C	Reserved																
A–B	A–B	PLL multiply-by-four mode																

Table 3–3. TEB Shunt Jumpers (Continued)

Name	Position	Description
RSV0	JP3.11	Reserved
RSV1	JP3.12	
RSV2	JP3.13	
RSV3	JP3.14	
RSV4	JP3.15	
EMU0	JP3.16	TI emulation support
EMU1	JP3.17	
LENDIAN	JP3.18	Selects endianness of addressing B–C Big endian A–B Little endian
ARDY	JP3.19	Asynchronous memory ready signal
HOLD–	JP3.20	Hold request from host (external memory interface bus arbitration)
UNUSED	JP3.21	Unused
UNUSED	JP3.22	Unused
TINP0	JP3.23	Timer input 0
TINP1	JP3.24	Timer input 1

Note: A–B indicates HIGH (1)
B–C indicates LOW (0)

Table 3–4. TEB DIP Switches

Name	Position	Description
BOOTMODE0	S4.1	Boot mode configuration. See the <i>TMS320C62xx Peripherals Reference Guide</i> for a complete description.
BOOTMODE1	S4.2	
BOOTMODE2	S4.3	
BOOTMODE3	S4.4	
BOOTMODE4	S4.5	
SWUSER	S4.6	User-defined input to U8 PAL [®]

TMS320C6201 TEB PAL[®] Equations

This appendix contains the programmable logic source for the TMS320C6201 test and evaluation board PAL[®] equations. These were compiled with DATA I/O ABEL[™] version 4.0.


```
module U8_MLA
Title '
PAL NAME      Memory Logic Block A (PAL MLA)
PAL #         U8, D600555-1741*
DWG NAME      TMS320C6201 Test & Evaluation Board
ASSY #        D600550-0001B
COMPANY       Texas Instruments, Incorporated

SYNTHESIS TOOL: ABEL-4 Design Environment v1.0'

U8 device 'P22V10C'; "The PALLV22V10 is a 28-pin PLCC

"NC                pin 1; NO CONNECT
clkout1            pin 2; "Clock out 1 from C6201
ce1_               pin 3; "Chip enable 1 from C6201
awe_              pin 4; "Asynchronous write enable from C6201
aoe_              pin 5; "Asynchronous output enable from C6201
ea21              pin 6; "EMIF address bit 21 from C6201
ce3_              pin 7; "Chip enable 3 from C6201
"NC               pin 8; NO CONNECT
tp2               pin 9; "Test point(2) input - undefined
tp3               pin 10; "Test point(3) input - undefined
tp4               pin 11; "Test point(4) input - undefined
tp5               pin 12; "Test point(5) input - undefined
swuser            pin 13; "Switch input - user defined
GND               pin 14; "Ground
"NC               pin 15; NO CONNECT
reset_            pin 16; "Reset
a_dir             pin 17; "Asynchronous direction
a_oe_             pin 18; "Asynchronous buffer output enable
romce_            pin 19; "ROM Chip Enable
p_ce_             pin 20; "Prototype chip enable
p_dir            pin 21; "Prototype buffer direction
"NC               pin 22; NO CONNECT
p_dboe_           pin 23; "Prototype data buffer output enable
p_aboe_           pin 24; "Prototype addr buffer output enable
tp6               pin 25; "Test point(6) output - undefined
tp7               pin 26; "Test point(7) output - undefined
tp8               pin 27; "Test point(8) output - undefined
VCC               pin 28; "Power
```

Equations

"Because the TMS320C6201 may be in part of a write cycle (i.e., setup or hold "time) when awe_ is inactive, the aoe_ signal should be used to determine the "direction of the access.

axoez	axwez	Access
0	0	Invalid combination with the DSP Should not happen so disable the buffers
0	1	Read from asynchronous type to the DSP Should cause buffers to output towards the DSP
1	0	Write (strobe) to asynchronous type from the DSP Should cause buffers to output towards async type
1	1	Could be part of a write cycle (i.e., write setup or hold time) Should cause buffers to output towards async type


```

a_dir   = aoe_;                                "A->B (i.e., DSP to external memories) when 1,
                                              "B->A (i.e., external memories to DSP) when 0
a_oe_   = (cel_ & ce3_ & awe_ & aoe_) # (!awe_ & !aoe_);

romce_  = cel_ # ea21;                        "Select flash ROM when ea21 = 0
p_ce_   = cel_ # !ea21;                       "Select Prototype area when ea21 = 1
p_dir   = (!(cel_ & ea21) # aoe_);
p_dboe_ = (awe_ & aoe_) # (!awe_ & !aoe_) # cel_ # !ea21;
p_aboe_ = 0;

```

Test_Vectors

```

([ cel_, ce3_,aoe_, awe_] -> [a_dir, a_oe_])
[ 1 , 1 , 0 , 0 ] -> [ 0 , 1 ];
[ 1 , 1 , 0 , 1 ] -> [ 0 , 0 ];
[ 1 , 1 , 1 , 0 ] -> [ 1 , 0 ];
[ 1 , 0 , 1 , 1 ] -> [ 1 , 0 ];
[ 0 , 1 , 1 , 1 ] -> [ 1 , 0 ];
[ 1 , 1 , 1 , 1 ] -> [ 1 , 1 ];

```

```
Test_Vectors
([cel_, ea21, aoe_, awe_] -> [romce_, p_ce_, p_dir, p_dboe_, p_aboe_])
[ 0 , 0 , 0 , 0 ] -> [ 0 , 1 , 1 , 1 , 0 ];
[ 0 , 0 , 0 , 1 ] -> [ 0 , 1 , 1 , 1 , 0 ];
[ 0 , 0 , 1 , 0 ] -> [ 0 , 1 , 1 , 1 , 0 ];
[ 0 , 0 , 1 , 1 ] -> [ 0 , 1 , 1 , 1 , 0 ];
[ 0 , 1 , 0 , 0 ] -> [ 1 , 0 , 0 , 1 , 0 ];
[ 0 , 1 , 0 , 1 ] -> [ 1 , 0 , 0 , 0 , 0 ];
[ 0 , 1 , 1 , 0 ] -> [ 1 , 0 , 1 , 0 , 0 ];
[ 0 , 1 , 1 , 1 ] -> [ 1 , 0 , 1 , 1 , 0 ];

[ 1 , 0 , 0 , 0 ] -> [ 1 , 1 , 1 , 1 , 0 ];
[ 1 , 0 , 0 , 1 ] -> [ 1 , 1 , 1 , 1 , 0 ];
[ 1 , 0 , 1 , 0 ] -> [ 1 , 1 , 1 , 1 , 0 ];
[ 1 , 0 , 1 , 1 ] -> [ 1 , 1 , 1 , 1 , 0 ];
[ 1 , 1 , 0 , 0 ] -> [ 1 , 1 , 1 , 1 , 0 ];
[ 1 , 1 , 0 , 1 ] -> [ 1 , 1 , 1 , 1 , 0 ];
[ 1 , 1 , 1 , 0 ] -> [ 1 , 1 , 1 , 1 , 0 ];
[ 1 , 1 , 1 , 1 ] -> [ 1 , 1 , 1 , 1 , 0 ];

end
```

TMS320C6201 TEB Schematics

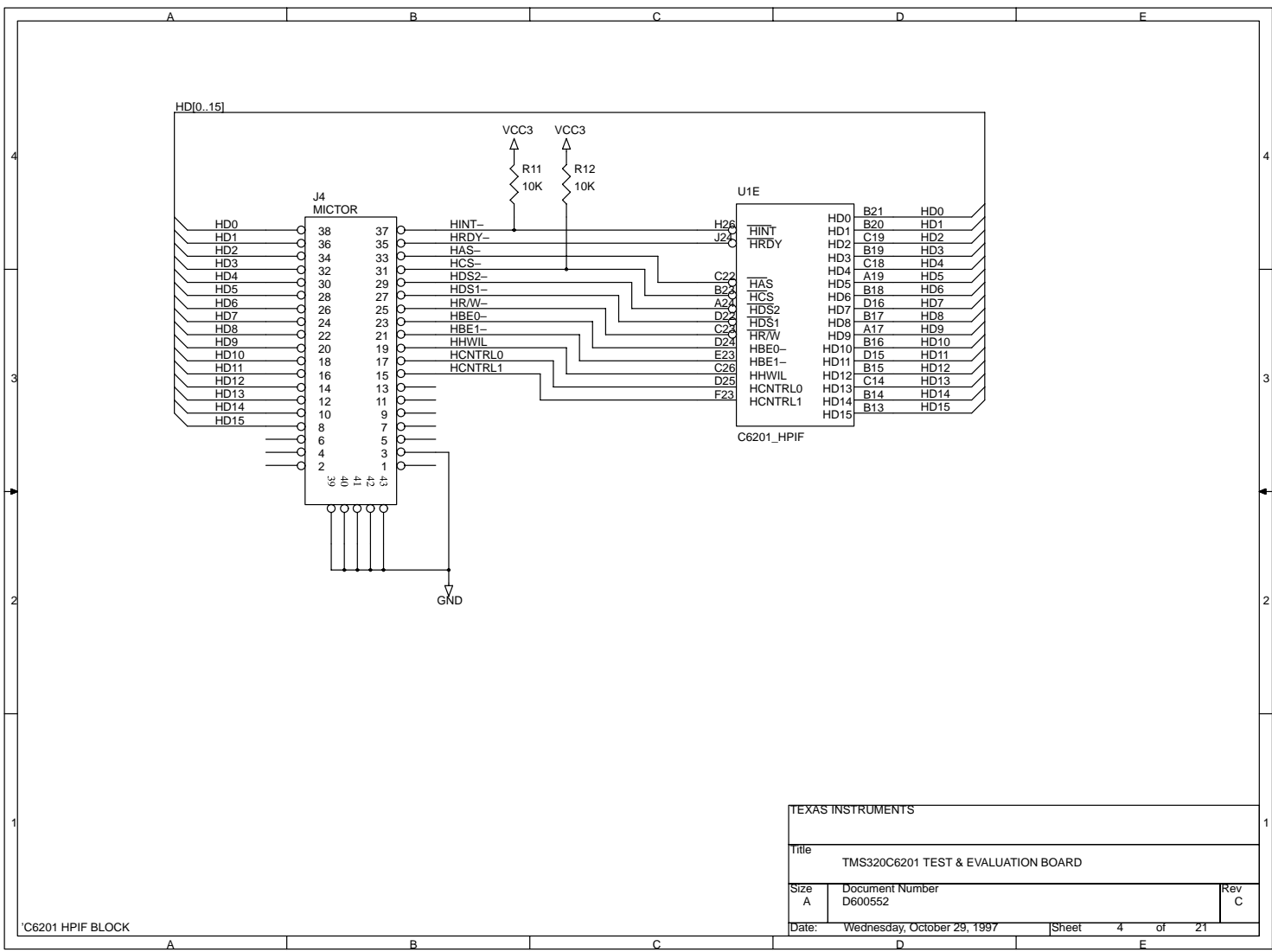
This appendix contains the schematics for the TMS320C6201 TEB.

A		B		C		D		E	
NOTES, UNLESS OTHERWISE SPECIFIED: 1. RESISTANCE VALUES ARE IN OHMS. 2. CAPACITANCE VALUES ARE IN MICROFARADS. 3. HIGHEST REFERENCE DESIGNATOR USED: A. CERAMIC CAPS C71 B. TANTALUM CAPS CT11 C. DIODES D1 D. FUSES F5 E. CONNECTORS/HEADERS J12 F. SHUNTS JP3 G. FILTER L1 H. RESISTORS R108 I. SWITCHES S5 J. TEST POINTS TP24 K. IC'S U32 4. UNUSED REFERENCE DESIGNATORS: A. RESISTORS R4,R97 B. SWITCHES S1,S2,S3 C. TEST POINTS TP1 D. IC'S U2,U5,U6,U7,U9 5. U1A-U1I COMPRISE A SINGLE TMS320C6201. THIS IS A 352-CONTACT BGA DEVICE THAT IS TOO LARGE TO SHOW ON A SINGLE SHEET. THIS REVISION OF THE BOARD IS COMPATIBLE WITH REV 2.X OF THE C6201 SILICON 6. ALL FOUR SHIELD CONNECTIONS OF J1 AND J3 MUST CONNECT TO THE GROUND PLANE. 7. SHUNTS FOR NMI AND EXT_INT4-EXT_INT7, AS APPROPRIATE, MUST NOT BE PULLED UP(VCC3) OR DOWN(GND) FOR CONTROL OF THESE SIGNALS. 8. PAGE ORDER AND NUMBERING MAY CHANGE BETWEEN REVISIONS OF THE SCHEMATICS				REVISIONS					
				REV	DESCRIPTION			DATE	APPROVED
				A	ECN970401(E) M. DAWKINS 4-3-97			6-6-97	J. CLARK
					FORMAL RELEASE				
				B	ECN10289(B) M. DAWKINS 9-8-97			9-11-97	J. CLARK
C	ECNxxxxx(E) M. DAWKINS								

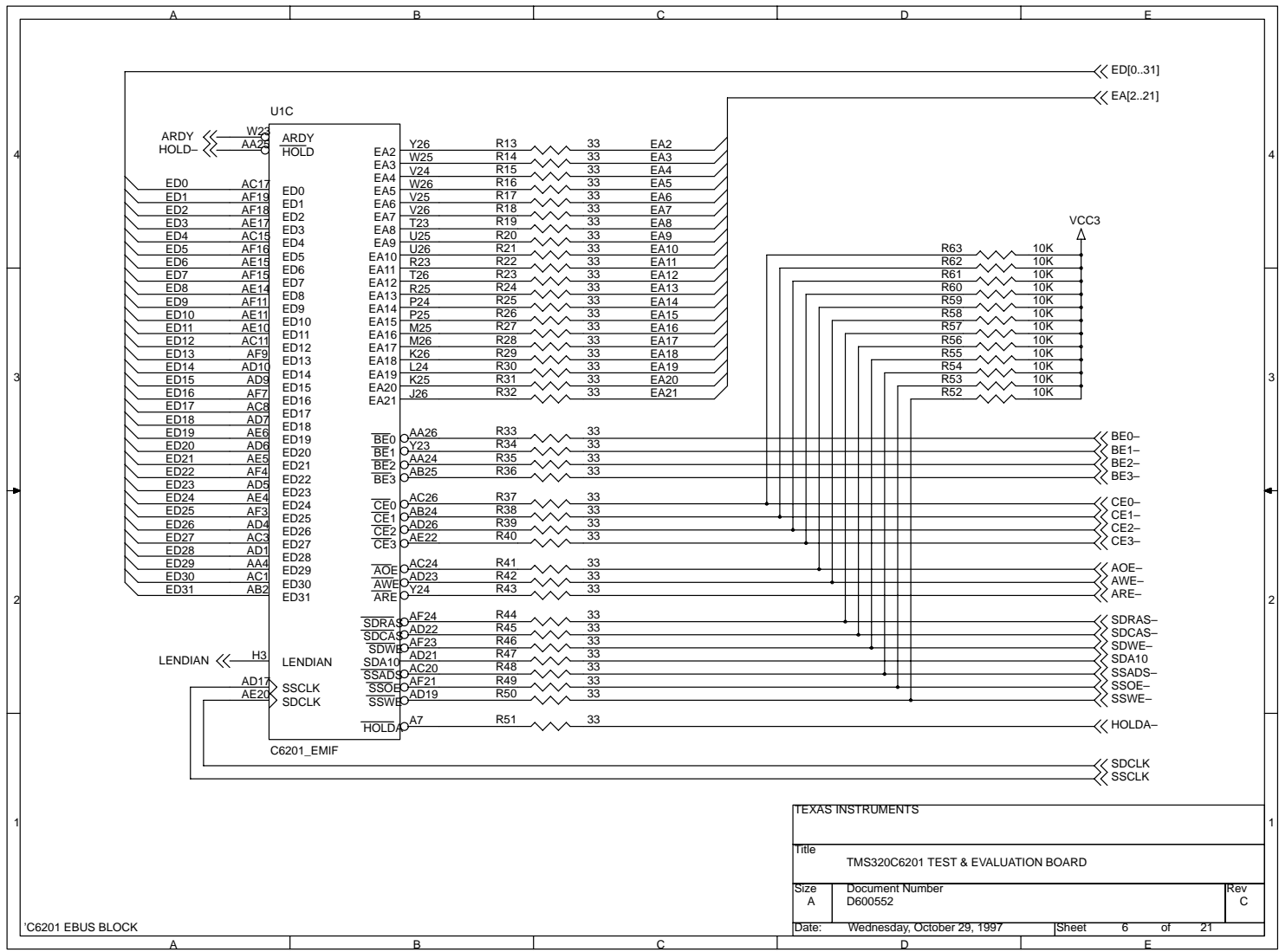
REVISION STATUS OF SHEETS								DWN		DATE		TEXAS INSTRUMENTS SOFTWARE DEVELOPMENT SYSTEMS SEMICONDUCTOR GROUP HOUSTON, TEXAS Title TMS320C6201 TEST & EVALUATION BOARD Size A Document Number D600552 Date: Wednesday, October 29, 1997 Sheet 1 of 21	
REV	C	C	C	C	C	C	C	CHK	G. CONNELLY	1-20-97			
SH	15	16	17	18	19	20	21	ENGR	M. DAVIS	6-6-97			
REV	C	C	C	C	C	C	C	ENGR-MGR	G. CONNELLY	6-6-97			
SH	8	9	10	11	12	13	14	QA	R. LERNER	6-6-97			
REV	C	C	C	C	C	C	C	J.A	J. WHISONANT	6-6-97	Rev C		
SH	1	2	3	4	5	6	7	MFG	M. JACKSON	6-6-97			
REV	C	C	C	C	C	C	C	RLSE	J. CLARK	6-6-97			
SH	1	2	3	4	5	6	7	APPLICATION					

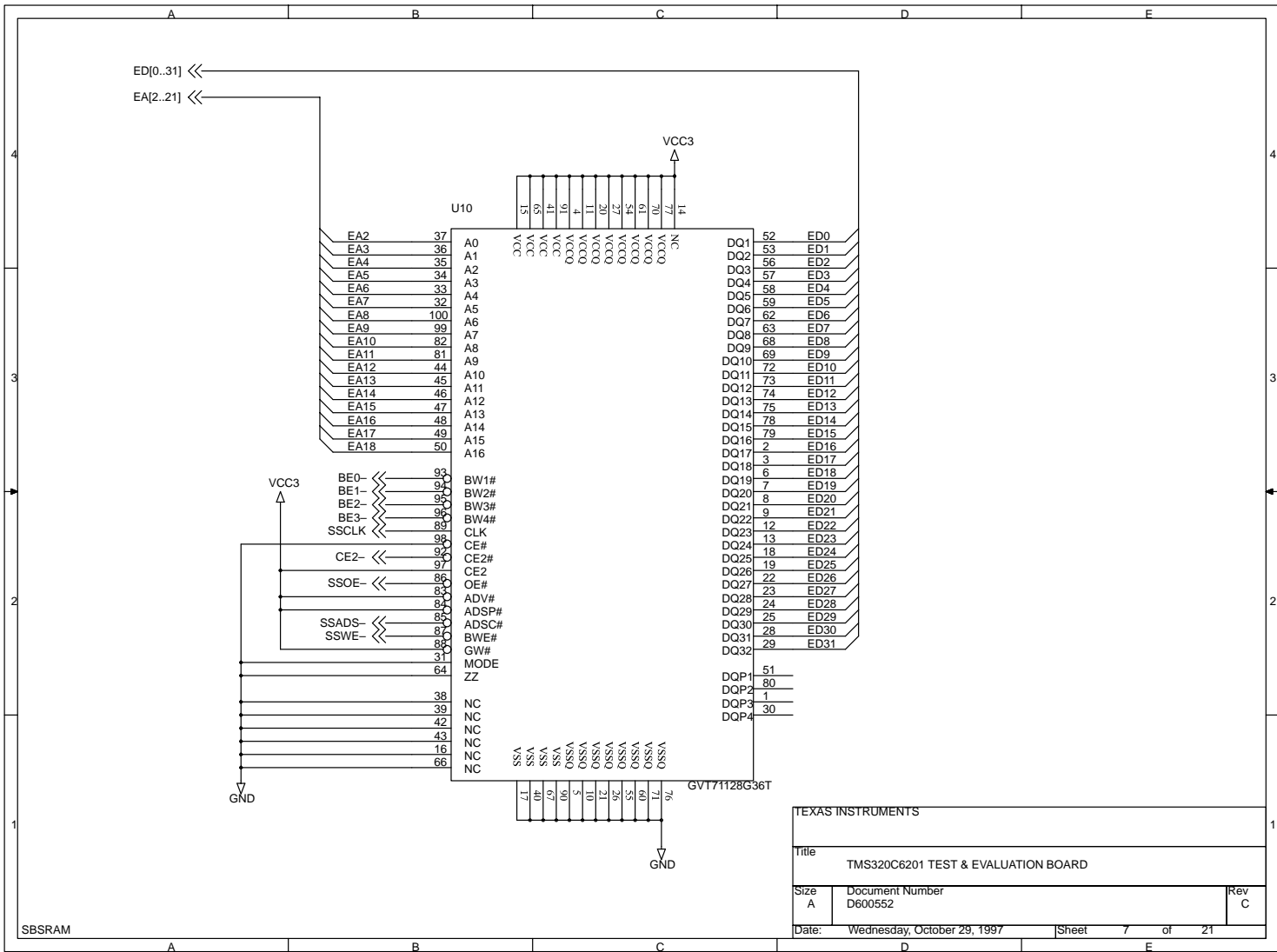


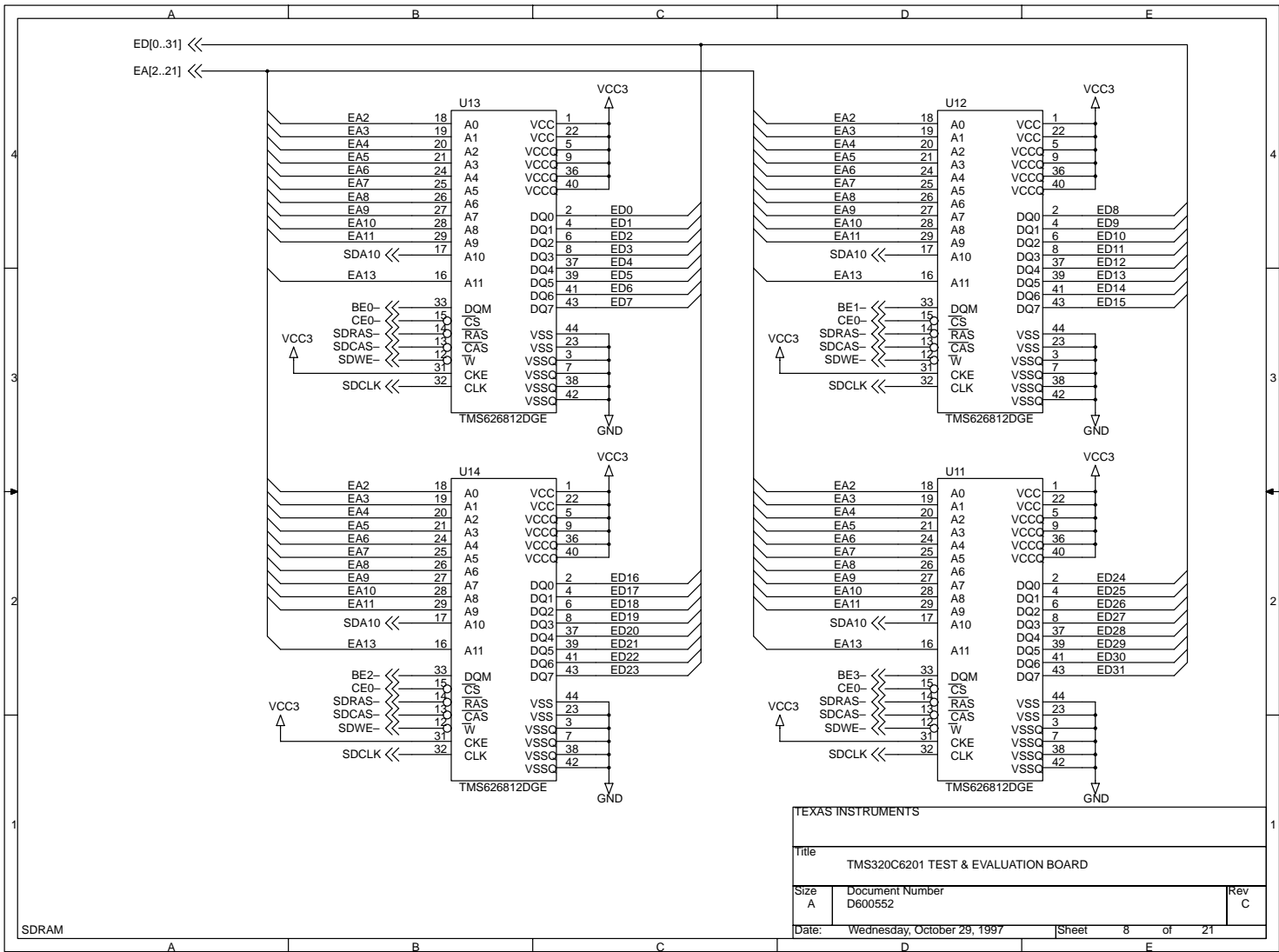




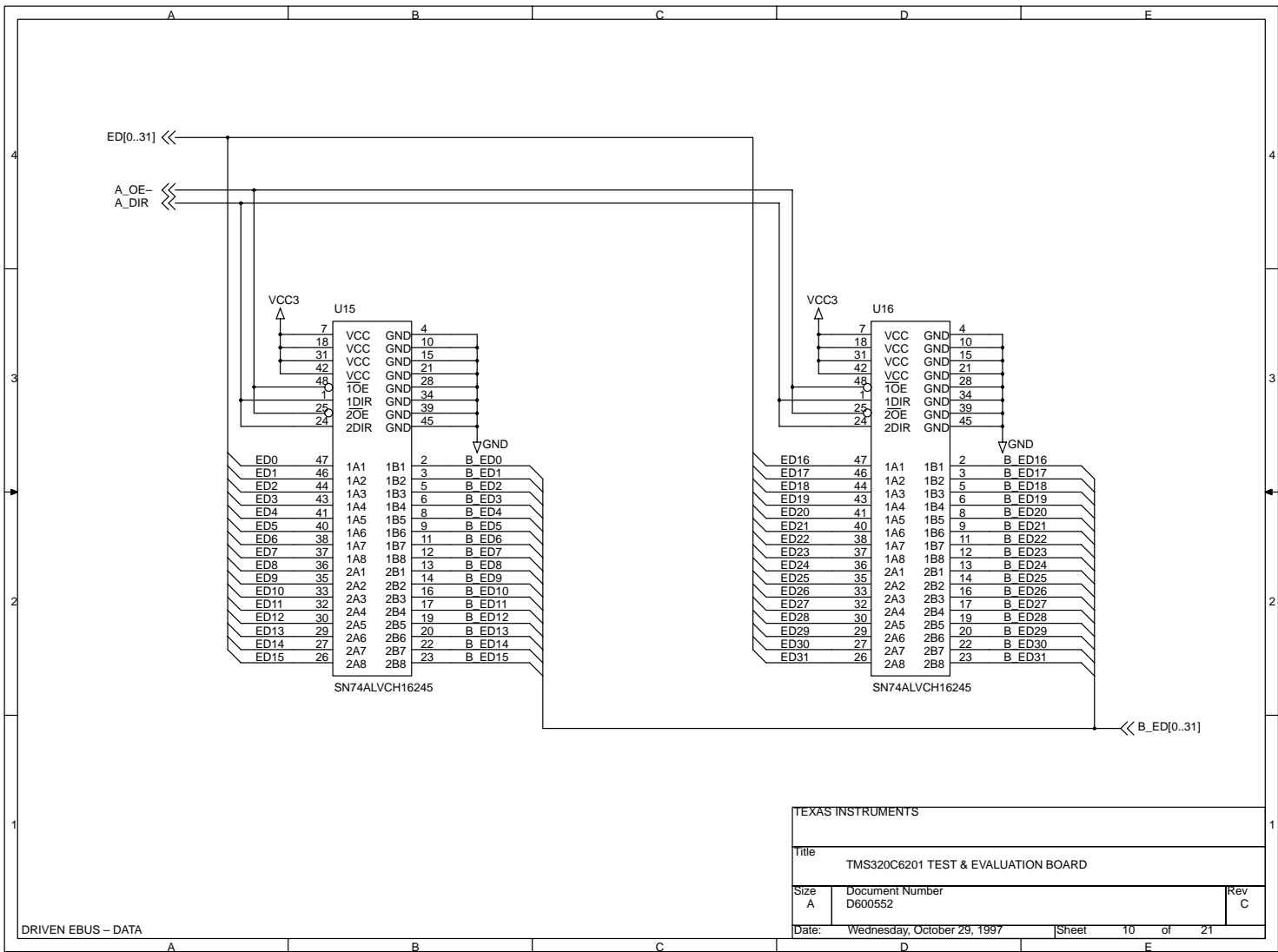


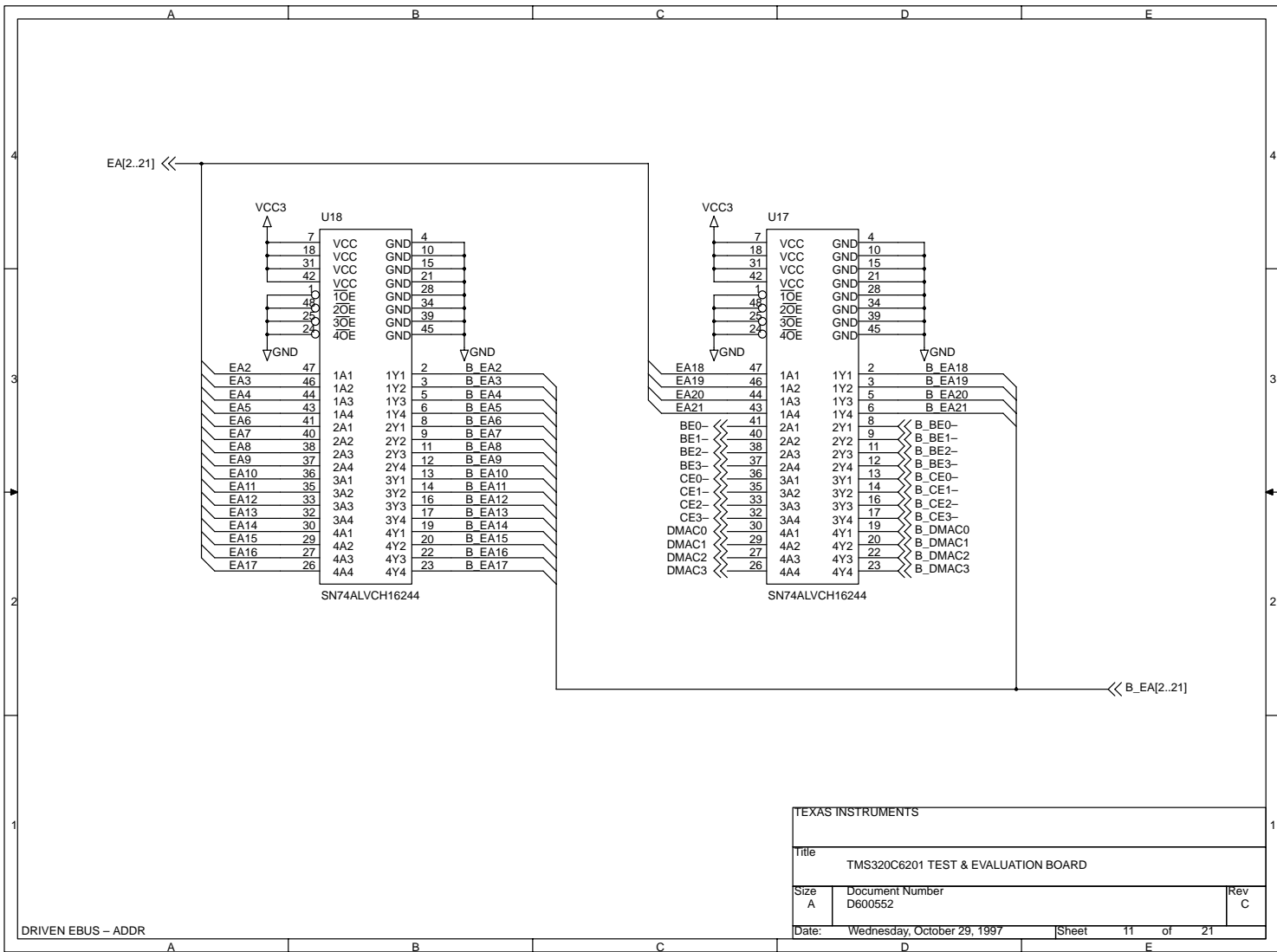


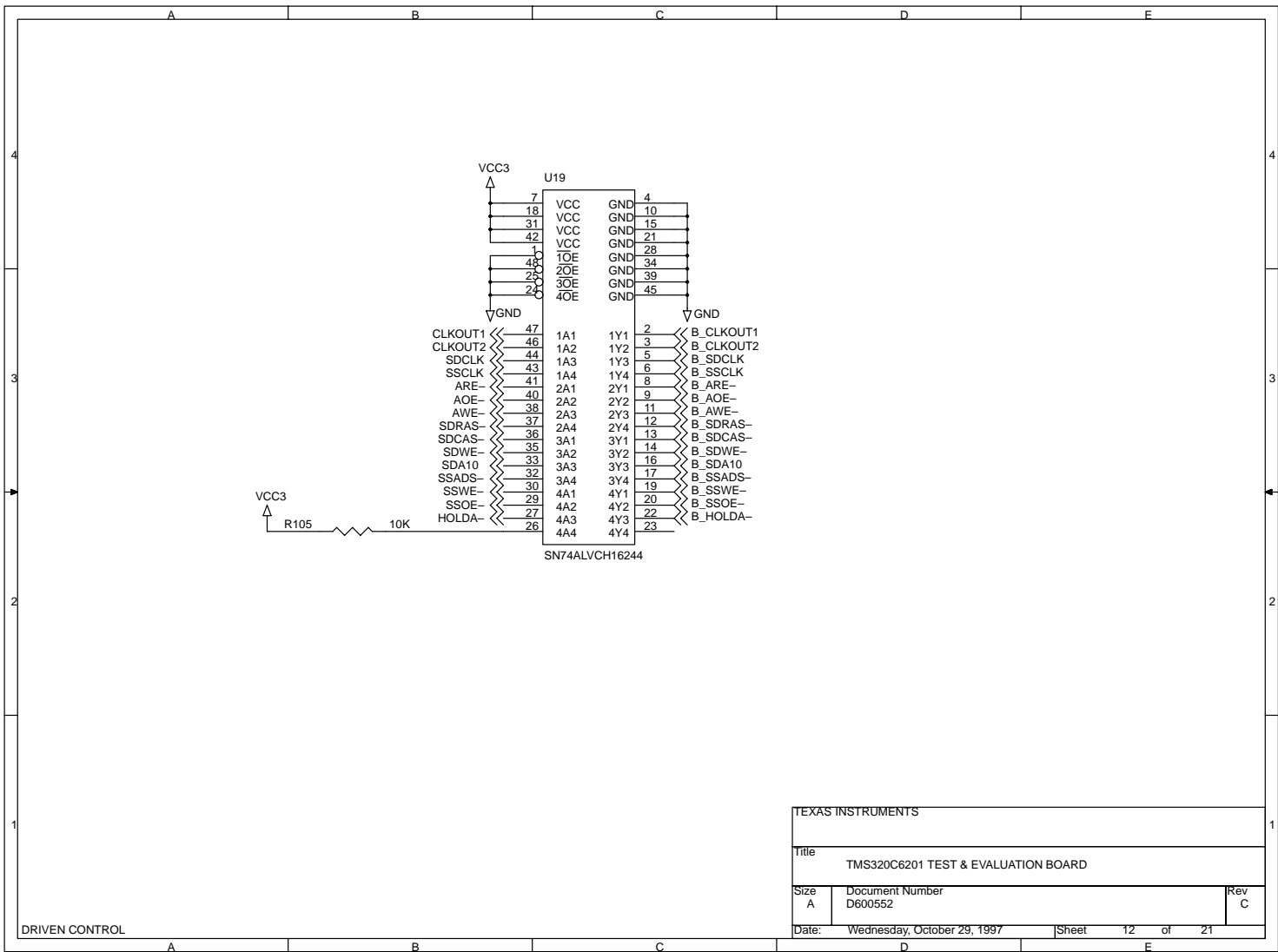


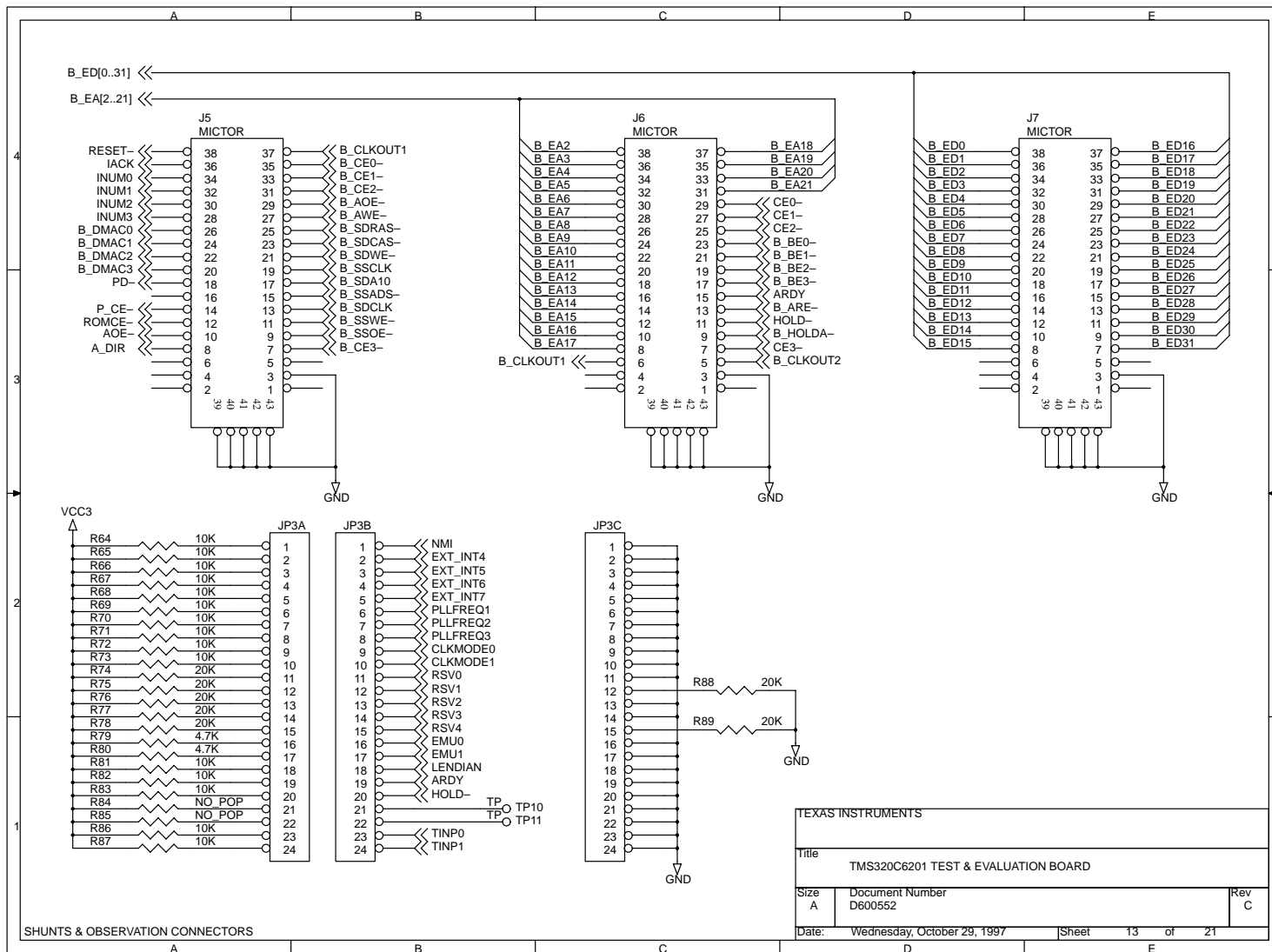


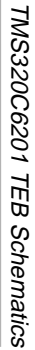


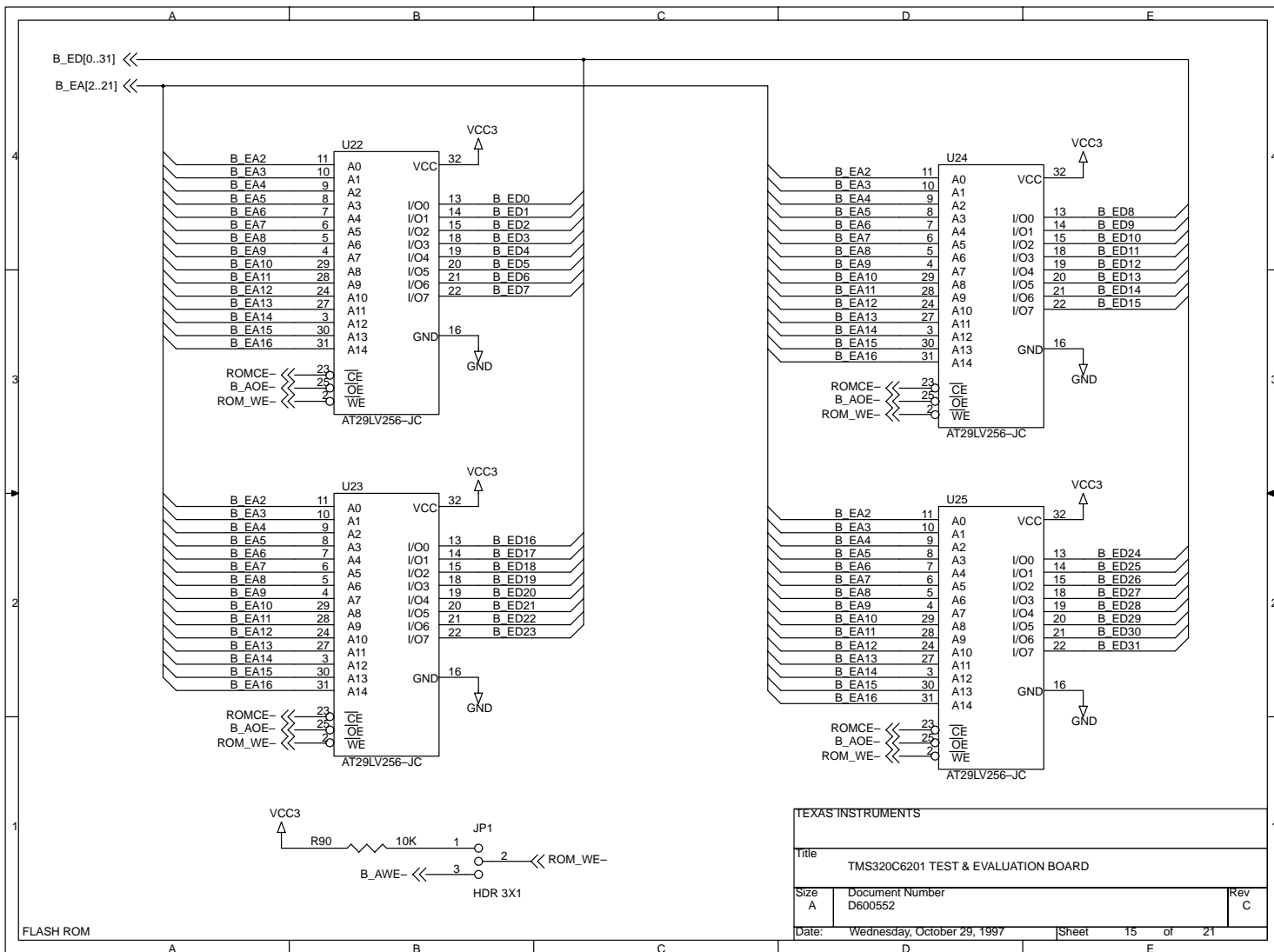


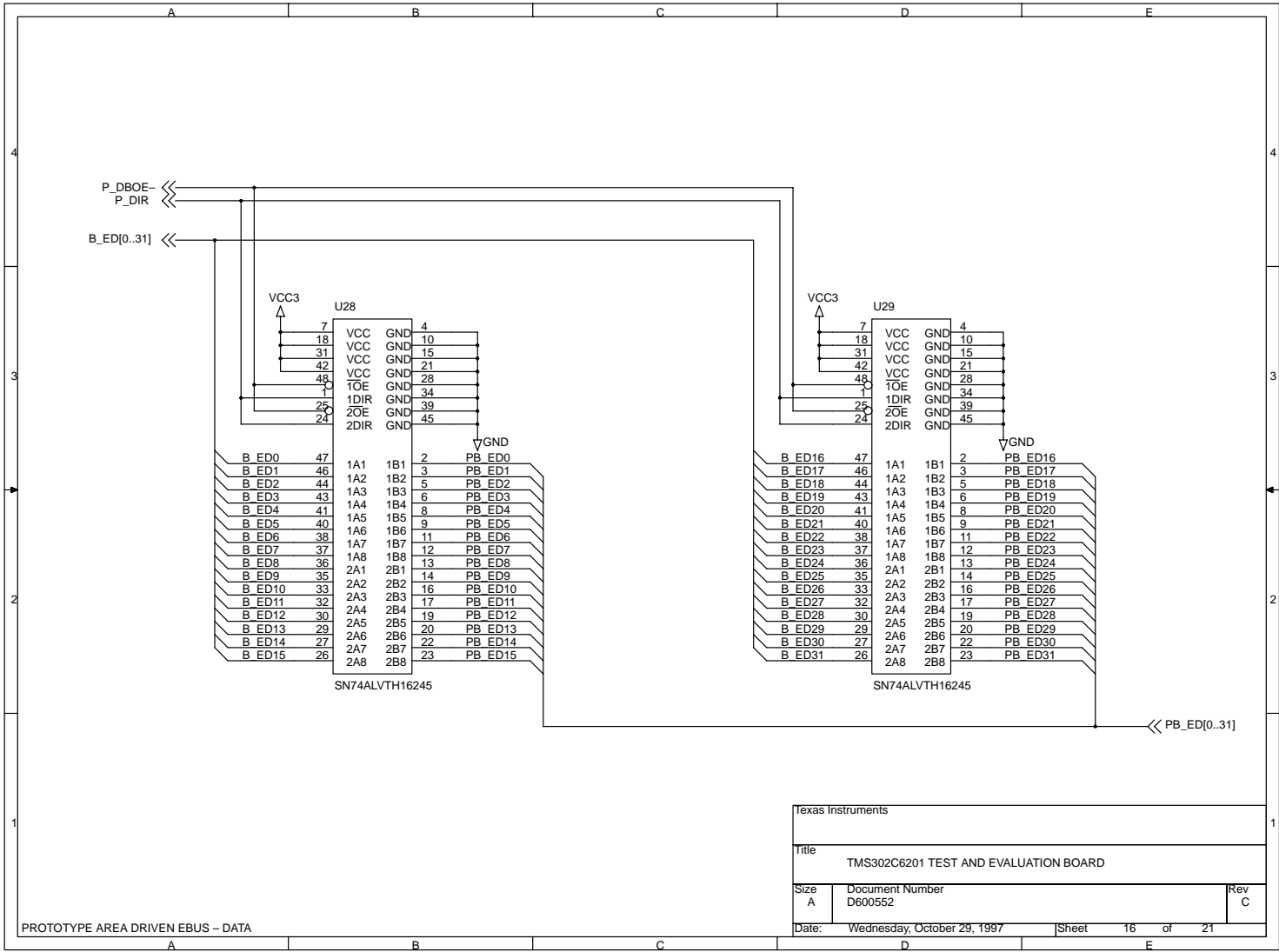


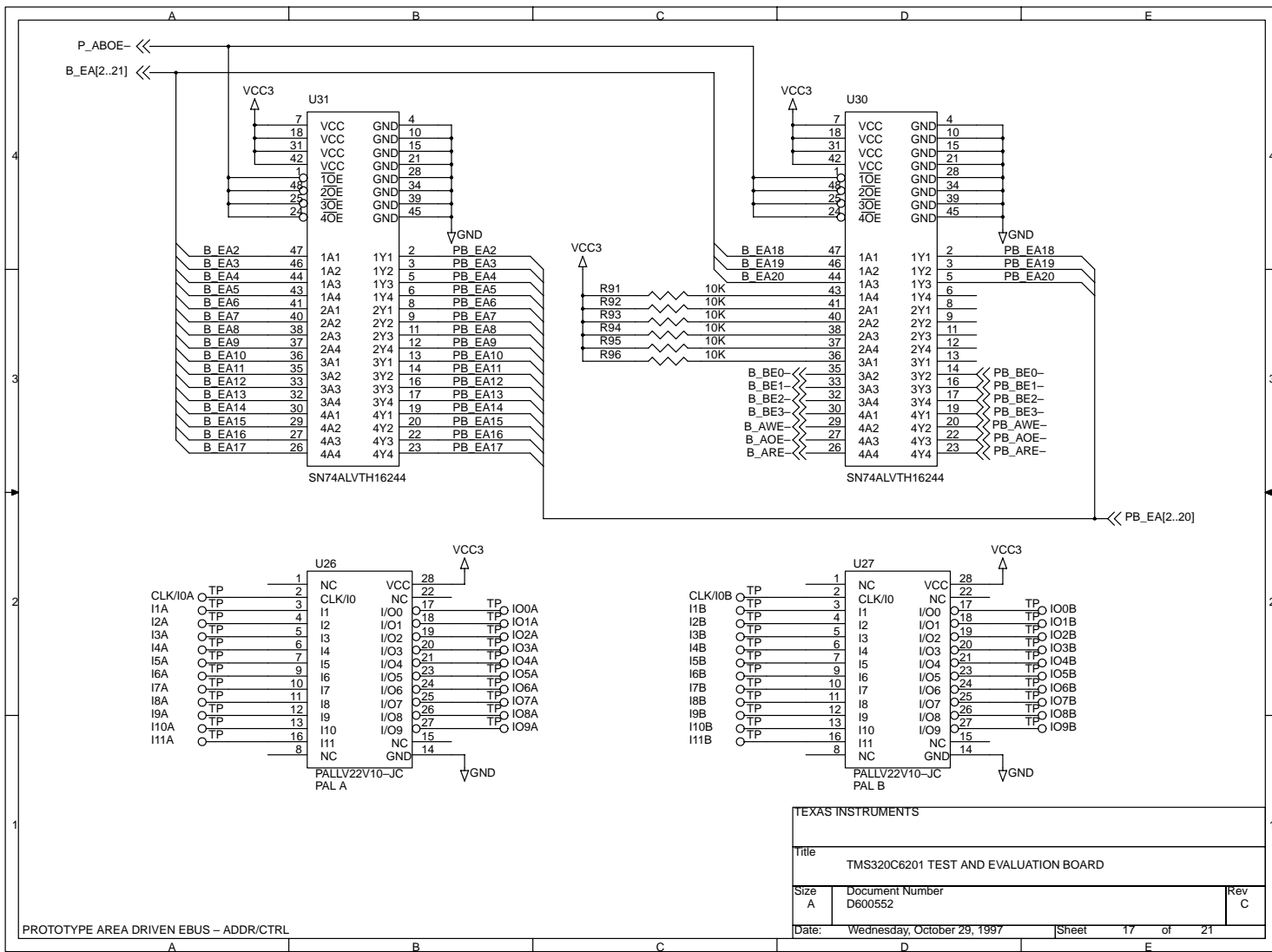


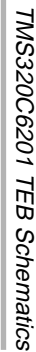


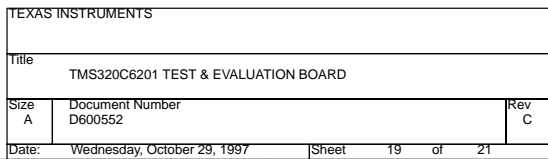


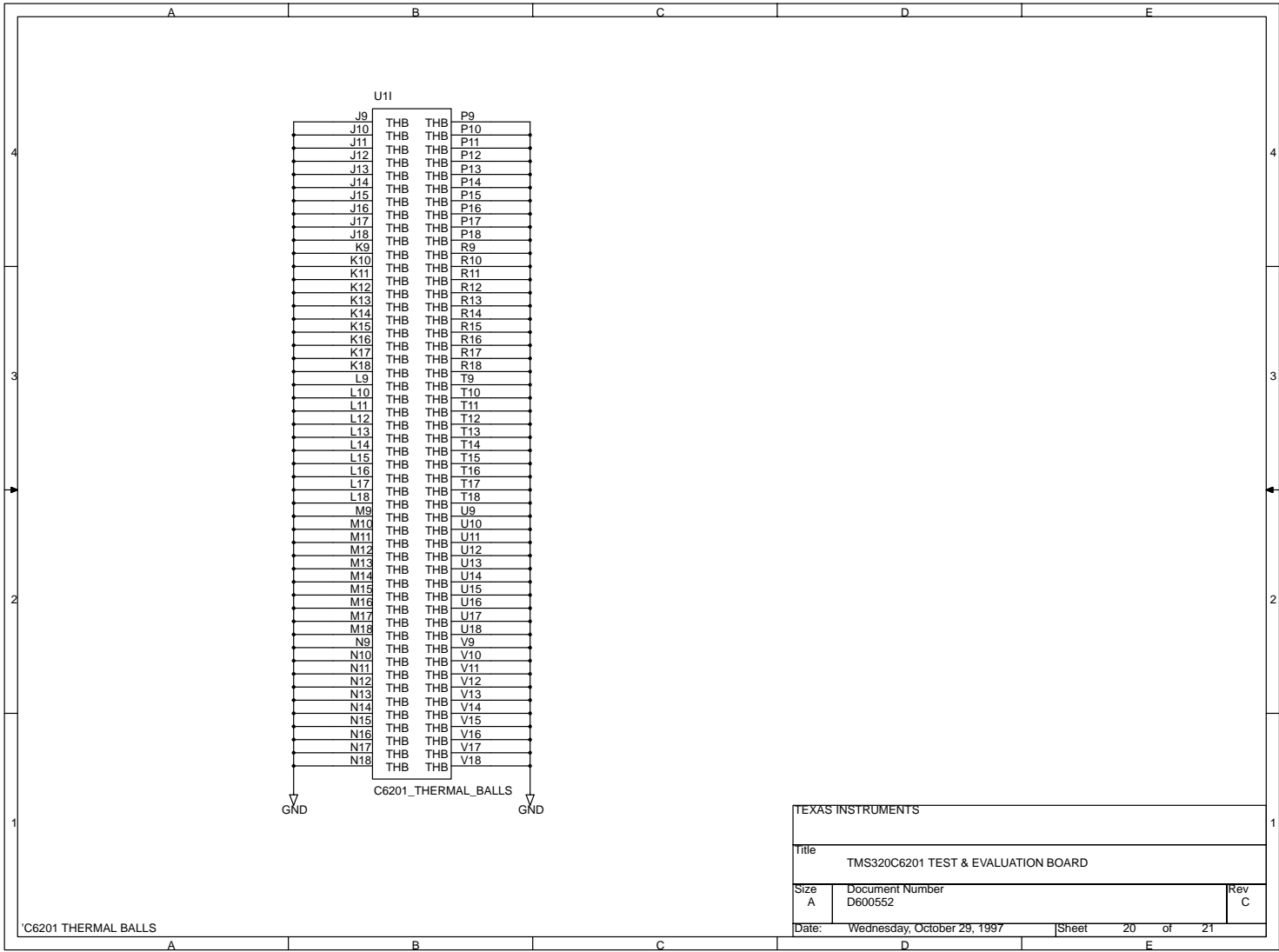


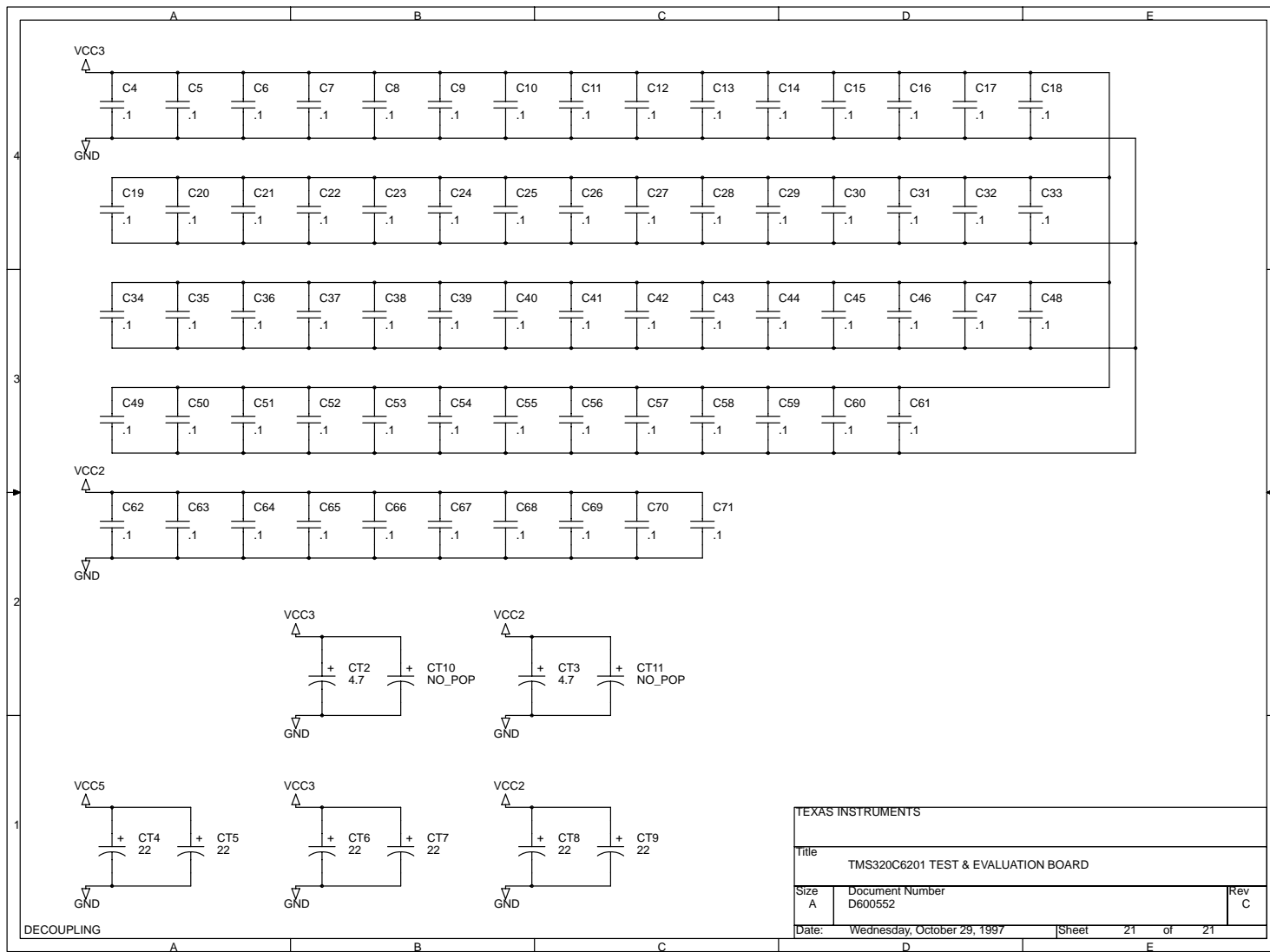












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