TEXAS INSTRUMENTS

TMS320C6x

Addendum to the TMS320 DSP Development Support Reference Guide

Addendum

TI DSP SOLUTIONS

15 YEARS OF LEADERSHIP

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Digital Signal Processing Solutions

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TMS320C6x Addendum

TMS320C6x Addendum to the TMS320 DSP Development Support Reference Guide

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Preface

Read This First

About This Manual

This addendum to the *TMS320 DSP Development Support Reference Guide* (DSRG) adds information on development support available from Texas Instruments for the TMS320C6x digital signal processors. Device names are abbreviated in this book; for example, TMS320C6x is referred to as 'C6x.

The chapters in this addendum do not map directly to the *TMS320 DSP Development Support Reference Guide* because the 'C6x chapter (Chapter 1 of this addendum) should be inserted between chapters 10 and 11 of the DSRG. The remaining chapters of this addendum provide supplemental information for other chapters of the DSRG.

How to Use This Manual

This document contains the following chapters:

Chapter 1, TMS320C6x Devices, describes the main features of the TMS320C6x devices. This chapter should be considered an insert between Chapters 10 and 11 of the *TMS320 DSP Development Support Reference Guide.*

Chapter 2, Tools, describes the code-generation, evaluation, and debug tools for the TMS320C6x devices. This type of information appears in Chapters 15 and 16 of the *TMS320 DSP Development Support Reference Guide.*

Chapter 3, Technical Support and Documentation, describes the workshops, web site, documentation, and third-party support available for the TMS320C6x devices. This type of information appears in Chapters 17 and 18 of the *TMS320 DSP Development Support Reference Guide*.

Related Documentation From Texas Instruments

The following books describe the TMS320C6x devices and related support tools. To obtain a copy of any of these TI documents, call the Texas

Instruments Literature Response Center at (800) 477–8924. When ordering, please identify the book by its title and literature number.

TMS320C6x Assembly Language Tools User's Guide (literature number SPRU186) describes the assembly language tools (assembler, linker, and other tools used to develop assembly language code), assembler directives, macros, common object file format, and symbolic debugging directives for the 'C6x generation of devices.

TMS320C62xx CPU and Instruction Set Reference Guide (literature number SPRU189) describes the 'C62xx CPU architecture, instruction set, pipeline, and interrupts for the TMS320C62xx digital signal processors.

TMS320C6x C Source Debugger User's Guide (literature number SPRU188) tells you how to invoke the 'C6x simulator and emulator versions of the C source debugger interface. This book discusses various aspects of the debugger, including command entry, code execution, data management, breakpoints, profiling, and analysis.

TMS320C6x Optimizing C Compiler User's Guide (literature number SPRU187) describes the 'C6x C compiler. This C compiler accepts ANSI standard C source code and produces assembly language source code for the 'C6x generation of devices. This book also describes the assembly optimizer, which helps you optimize your assembly code.

TMS320C62xx Peripherals Reference Guide (literature number SPRU190) describes common peripherals available on the TMS320C62xx digital signal processors. This book includes information on the internal data and program memories, the external memory interface (EMIF), the host port, serial ports, direct memory access (DMA), clocking and phase-locked loop (PLL), and the power-down modes.

TMS320C62xx Programmer's Guide (literature number SPRU198) describes ways to optimize C and assembly code and includes application program examples.

TMS320C62xx Technical Brief (literature number SPRU197) gives an introduction to the 'C62xx digital signal processor, development tools, and third-party support.

TMS320C6201 Digital Signal Processor Data Sheet (literature number SPRS051) describes the features of the TMS320C6xx and provides pinouts, electrical specifications, and timings for the device.

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Hong Kong DSP Hotline	+852 2 956 7268	Fax: +852 2 956 1002
Korea DSP Hotline	+82 2 551 2804	Fax: +82 2 551 2828
Korea DSP Modem BBS	+82 2 551 2914	
Singapore DSP Hotline		Fax: +65 390 7179
Taiwan DSP Hotline	+886 2 377 1450	Fax: +886 2 377 2718
Taiwan DSP Modem BBS	+886 2 376 2592	

Taiwan DSP Internet BBS via anonymous ftp to ftp://dsp.ee.tit.edu.tw/pub/TI/

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Product Information Center	+0120-81-0026 (in Japan)	Fax: +0120-81-0036 (in Japan)
	+03-3457-0972 or (INTL) 813-3457-0972	Fax: +03-3457-1259 or (INTL) 813-3457-1259
DSP Hotline	+03-3769-8735 or (INTL) 813-3769-8735	Fax: +03-3457-7071 or (INTL) 813-3457-7071
DSP BBS via Nifty-Serve	Type “Go TIASP”	

❑ Documentation

When making suggestions or reporting errors in documentation, please include the following information that is on the title page: the full title of the book, the publication date, and the literature number.

Mail: Texas Instruments Incorporated
Technical Documentation Services, MS 702
P.O. Box 1443
Houston, Texas 77251-1443

Email: comments@books.sc.ti.com

Note: When calling a Literature Response Center to order documentation, please specify the literature number of the book.

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Chapter 1

TMS320C6x Devices

The TMS320C6x devices are the first devices to feature VelociTI™, an advanced very long instruction word (VLIW) architecture developed by Texas Instruments, which allows performance of up to 1600 million instructions per second (MIPS). The first device in the series is the TMS320C6201, a fixed-point digital signal processor (DSP).

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1.1 TMS320C6x Introduction

With a complete set of development tools, the ’C6x devices offer cost-effective solutions to high-performance DSP programming challenges. The ’C6x development tools include a new C compiler, an assembly optimizer, and a Windows-based debugger. VelociTI combines an advanced VLIW architecture with a high degree of parallelism to produce a device that enables applications such as:

- Unlimited Internet bandwidth
- Universal wireless communications
- New telephony features
- Remote medical diagnostics
- Automated cruise control
- Personal home base station
- Personalized home security

The ’C6x devices also can be used for improved performance on existing applications, such as:

- Wireless base stations
- Pooled modems and remote access servers
- Next-generation xDSL modems and cable modems
- Multichannel telephony platforms, including central office switches, PBXs, and voice-messaging systems
- Multimedia systems
- Digital imaging

1.2 Key Features

The TMS320C6201 is the first fixed-point processor in the ’C6x generation. Following are key features of the TMS320C6201:

- VelociTI advanced very long instruction word (VLIW) architecture
  - Load/store architecture
  - Instruction packing for reduced code size
  - 100% conditional instructions for faster execution
  - Intuitive, reduced instruction set computing (RISC)-like instruction set
- CPU
  - Eight independent functional units (including two 16-bit multipliers with 32-bit results and six arithmetic logic units [ALUs] with 32-/40-bit results)
  - 32 32-bit registers
  - 1600 million instructions per second (MIPS)
  - Five-ns cycle time
  - Up to eight 32-bit instructions per cycle
  - Byte-addressable 8-, 16-, 32-bit data
  - 32-bit address range
  - Dual-endian support
  - Saturation
  - Normalization
  - Bit-field instructions (extract, clear, left most bit detection)
- Memory/peripherals
  - Synchronous external memory interface (EMIF)
  - Two multichannel serial ports (MCSPs)
  - Four-channel direct memory access (DMA)
  - Two timers
  - X4 phase-locked-loop (PLL) option
  - Host-port interface (HPI)
  - 1M-bit on-chip memory (divided into 2K by 256 bits of program memory and 64K bytes of data memory)
- 352-pin ball-grid array package

1.3 Central Processing Unit (CPU)

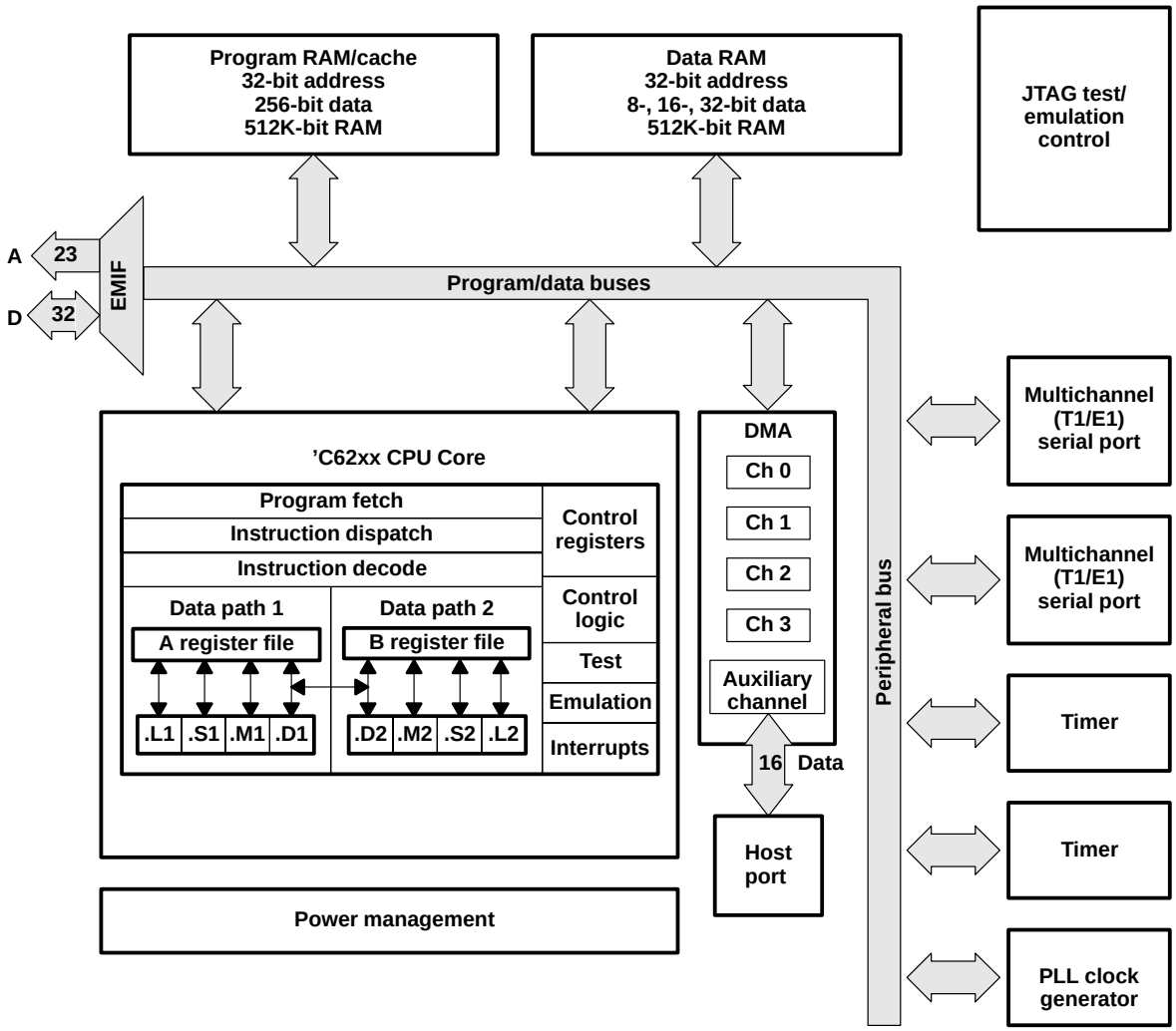
The ’C6x central processing unit (CPU) is the central building block of all the TMS320C62xx devices. The CPU contains:

- Program fetch unit
- Instruction dispatch unit
- Instruction decode unit
- 32 general-purpose, 32-bit registers
- Two data paths, each with four functional units, including one multiplier and three arithmetic logic units (ALUs) on each data path
- Control registers
- Control logic
- Test, emulation, and interrupt logic

The CPU has two data paths where processing occurs. Each data path has four functional units and a register file containing 16 32-bit registers. The functional units execute logic, shifting, multiply, and data address operations. All instructions operate on the registers. The two sets of data-addressing units are exclusively responsible for all data transfers between the register files and the memory.

Figure 1–1 shows the CPU core and peripherals for a TMS320C6201 device.

Figure 1–1. CPU Core With Peripherals



1.3.1 Addressing Modes

The addressing mode options on the 'C62xx are either linear or circular, as specified by the addressing-mode register (AMR).

For more information on addressing modes, see the *TMS320C62xx CPU and Instruction Set Reference Guide*.

1.3.2 Interrupts

The CPU has 14 interrupts. These are the reset interrupt, the nonmaskable interrupt (NMI), and interrupts 4–15. These interrupts correspond to the $\overline{\text{RESET}}$, NMI, and INT4–INT15 signals on the CPU boundary. In some ’C62xx devices, these signals may be tied directly to pins on the device, connected to on-chip peripherals, or may be disabled permanently by being tied inactive on chip. Generally, RESET and NMI are connected directly to pins on the device.

For more information on interrupts, see the *TMS320C62xx CPU and Instruction Set Reference Guide* (literature number SPRU189).

1.4 Internal Memory

The internal memory consists of 512K bits of on-chip program/cache memory and 512K bits of on-chip data memory. The program memory, configurable as cache or program, is organized in 2K of 256-bit fetch packets. The ’C6201 fetches all instructions one fetch packet at a time. The packets are processed at the maximum rate of one packet (eight 32-bit instructions) per CPU cycle or at a minimum of one instruction per cycle. The internal data memory is byte addressable by the CPU (for reads as well as writes) and supports bytes, halfwords, and full word transfers.

1.4.1 Data-Memory System

The TMS320C62xx data-memory system includes SRAM and a memory controller. The CPU can access data memory in 8-bit byte, 16-bit halfword, and 32-bit word-lengths. The data memory system supports two memory accesses per cycle. These accesses can be any combination of loads and stores from the two data buses of the CPU. Similarly, a simultaneous internal and external memory access is supported by the data memory system. The TMS320C62xx data memory system also supports direct-memory access (DMA) and external host accesses. For more information on the data-memory system, see the *TMS320C62xx Peripherals Reference Guide*.

1.4.2 Program-Memory System

The TMS320C62xx program-memory system includes on-chip SRAM and a memory/cache controller. The program memory can operate as either an internal program memory or as a directly mapped program cache. There are four modes under which the program memory system operates:

- Program-memory mode
- Cache-enable mode
- Cache-freeze mode
- Cache-bypass mode

The DMA can write data into an addressed space of program memory. The DMA cannot read from the internal program memory in program memory mode.

For details on cache modes, see the *TMS320C62xx Peripherals Reference Guide.*

1.5 Peripherals

In addition to on-chip memory, the TMS320C6201 contains the following peripherals:

- External memory interface (EMIF)
- Direct-memory access (DMA) controller
- Host-port interface (HPI)
- Power-down logic
- Two multichannel serial ports (MCSPs)
- Two 32-bit timers

1.5.1 External Memory Interface (EMIF)

All external data accesses by the CPU or DMA pass through the external memory interface (EMIF). The EMIF is the interface between the CPU and external memory such as synchronous dynamic random-access memory (SDRAM), synchronous-burst static RAM (SBSRAM), and asynchronous memory. The EMIF also provides 8-bit and 16-bit wide memory read capability to support low-cost boot ROM memories (flash, EEPROM, EPROM, and PROM).

The interface is programmable to adapt to a variety of setup, hold, and strobe widths for asynchronous devices. SBSRAM supports zero-wait-state external access once bursts have begun.

In all these types of access, the EMIF supports 8-bit, 16-bit, and 32-bit addressability for writes. All reads are performed as 32-bit transfers.

For more information on memory, see the *TMS320C62xx CPU and Instruction Set Reference Guide* (literature number SPRU189). For more information on the EMIF, see the *TMS320C62xx Peripherals Reference Guide*.

1.5.2 Direct-Memory Access (DMA)

The on-chip DMA offers four independent, programmable channels that can be configured to transfer information from one location in the memory map to another without interfering with the operation of the CPU. This allows interfacing to slow external memories and peripherals without reducing the throughput to the CPU. The DMA controller contains its own address generators, source and destination registers, and transfer counter. The DMA has its own bus for addresses and data to keep the data transfers between memory and peripherals from conflicting with the CPU.

A DMA operation consists of a 32-bit word transfer to or from any of the three ‘C62xx modules:

- Internal data memory
- Internal program memory that is not configured as cache as a destination of a transfer
- EMIF

One of the DMA channels can be used by the processor during the boot load startup procedure to initialize the internal program memory after reset. The DMA channels can be used to write to internal program memory.

The boot loader uses the DMA to boot load code from off-chip memory to the internal program memory area. An external pin (sampled at reset) selects whether this boot load is performed. The serial port can also be used for booting.

The DMA controller can access all internal program memory, all internal data memory, and all devices mapped to the EMIF. However, the DMA cannot use program memory as the source of a transfer and it cannot access memories configured as cache or memory-mapped on-chip peripheral registers.

See the data sheet for the specific device to find the memory mapping of DMA control registers. These registers are 2-bits wide and must be accessed through 32-bit accesses from the CPU. For more information on the DMA operations, see the *TMS20C62xx Peripheral Reference Guide.*

1.5.3 Host-Port Interface (HPI)

The HPI is a parallel port that can access the CPU memory space directly as an asynchronous interface. A host (external) processor can read from and write to the internal data memory through the 16-bit-wide access of the HPI.

The HPI can boot load the CPU as well as access the full range of the ’C6201 memory. Also, the HPI offers improved performance and can operate without impacting CPU performance.

For more information on the HPI, see the *TMS320C62xx Peripheral Reference Guide*.

1.5.4 Power-Down Logic

The ’C62xx supports three power-down modes (Idle1, 2, and 3) that can reduce system power requirements significantly. Idle1 halts the CPU except for the interrupt logic. Idle2 halts the CPU and the peripherals (except for the interrupt logic). Idle3 halts the phase-locked loop (PLL), stopping the clock tree from switching, which effectively halts the entire chip. Idle 3 requires a reset to wake up the device, while the other two modes can be restored using an interrupt or reset. For more details on the power-down logic, see the *TMS320C62xx Peripherals Reference Guide*.

1.5.5 Multichannel Serial Port (MCSP)

The ’C6201 includes two MCSPs, supporting multivendor interface protocol (MVIP) and timers to allow easy algorithm integration. The MCSP is based on the standard TMS320C2x/C5x/C54x serial-port interface. In addition, it has the ability to buffer serial samples in memory automatically with the aid of the DMA. It also has multichannel capability compatible with the T1, E1, and MVIP standards.

The MCSP provides:

- ❑ Full-duplex communication
- ❑ Double-buffered data registers
- ❑ Direct interface to other devices
- ❑ Clock generation or an internal programmable frequency shift clock
- ❑ Multichannel transmit and receive

1.5.6 Timers

The device has two 32-bit general purpose timers that you can use to:

- ❑ Time events
- ❑ Count events
- ❑ Generate pulses
- ❑ Interrupt the CPU
- ❑ Send synchronization events to the DMA

The timer has two signaling modes and can be clocked by an internal or an external source. The timer has an I/O pin that functions as an input clock, as an output clock, or as a general-purpose I/O pin.

Chapter 2

TMS320C6x Tools

The TMS320C6x design environment reflects the nature of the advanced very long instruction word (VLIW) architecture. The environment includes code-generation tools, evaluation tools, on-line help, and technical documentation. This chapter provides addenda to Chapters 15 and 16 of the DSRG.

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2.1 Code-Generation Tools (Chapter 15 Addendum)

Code-generation tools for both the PC and Sun workstations are as follows:

- C compiler
- Assembly optimizer
- Assembler
- Linker

The tools take C or assembly source code and implement many different optimizations, including software pipelining, to find and exploit the unique instruction-level parallelism of the ’C6x. After each step in the process, the ’C6x tools allow you to evaluate the results and take appropriate steps to achieve the most parallel code.

2.1.1 C Compiler

The ’C6x C compiler accepts ANSI C source code and produces ’C6x assembly language source code, performing a variety of optimizations to improve the efficiency of the compiled code. The compiler incorporates four levels of generic and target-specific optimizations. The level of optimizations is selectable. The optimizations specific to the ’C6x DSP include:

- Software pipelining
- If conversion/predicated execution
- Memory address cloning
- Memory address dependence elimination

2.1.2 Assembly Optimizer

Once the dynamic profiler identifies critical code segments that can benefit most from being generated in assembly language, the assembly optimizer schedules the instructions, taking into account the architectural parallelism of the ’C6x DSP. The assembly optimizer allows you to write assembly code without being concerned with pipeline structure of the device or with assigning registers. The tool honors ’C6x latency requirements, maximizes parallel code, and allocates registers for the unlimited number of named, virtual registers that are available to the user. The assembly optimizer takes in linear assembly instructions and creates an intermediate file that is input into the code generator. The code generator then produces optimized and/or software pipelined assembly code.

2.1.3 Assembler

The assembler translates assembly language source code files into machine language common object file format (COFF) object files. The assembly files can contain ’C6x assembly language instructions, assembler directives, and macro directives.

2.1.4 Linker

The linker allows you to combine COFF object files into a single executable COFF output file. The linker allocates relocatable sections and symbols and resolves external references between input files. It also accepts previously linked files and library members as input.

2.2 Evaluation Tools (Chapter 16 Addendum)

The evaluation tools include the following:

- Windows-based debugger interface
- Simulator
- Hardware emulation board

The ’C6x development environment provides a new intuitive Windows 95 based graphical user interface (GUI) for debugging. The debugger interface features windows for source, assembly, call stack, memory, registers, and watch expressions as well as menus and tool bars. The debugger offers one-click breakpoint setting and dialogs for editing breakpoints. The debugger also incorporates the dynamic profiler to help users find bottlenecks and improve code efficiency.

The profiler integrated into the ’C6x debugger creates cycle histograms that are continuously updated as the code runs. It can show graphically which functions, ranges and lines in an application are performance bottlenecks. The profiler can show:

- The percentage of total execution time spent in any function
- The number of times a function is called
- Total cycles in the application, function, or line

A timing display can be built into the application by inserting a few function calls in the code. The resulting simple cycle counts, obtained without using the profiler or the debugger, can be printed automatically to allow you to track the changes in execution speed of an algorithm over time. This output, while less sophisticated, is continuously available with no further action.

TI provides scan-based emulation systems that support hardware and software debugging of target systems via a JTAG emulation cable. Scan-based emulation is a unique, nonintrusive approach to system emulation, integration, and debugging.

Initially, TI offers a stand-alone ’C6201 test and emulation board (TEB) that interfaces with the host platform through the XDS510™ and XDS 510WS™ emulators through the IEEE Standard 1149.1 (JTAG) compliant port. The board features a prototyping area for adding user-defined peripherals.

2.2.1 Debugger Interface Features

The debugger allows you to run and halt the processor; step through instructions; view and modify registers, memory values and C variables; view source and profile code by line, by range, or by C function. Debugger features include:

- ❑ Windows 95 interface
- ❑ Menu options for entering and leaving the profiler without exiting the debugger
- ❑ C input/output displays in the command window
- ❑ Options for starting and halting the ’C6x, including single-step, step-over, return from called function, and run and halt commands
- ❑ Support for debugging in C, assembly language, or both
- ❑ Identification of time-consuming sections of the program through the profiler
- ❑ Memory window that displays the values of a block of memory in any format specified
- ❑ Watch window that displays the values of variables in the native C format
- ❑ C source window that displays the C code and highlights the current line

2.2.2 Simulator

The ’C6x simulator is a software program that uses the TMS320 debugger graphical user interface to simulate the operation of the ’C6x processor on the host processor rather than on an actual target system. It uses object code produced by the macro assembler/linker or ANSI C compiler with the debugger interface. The simulator provides XDS510 software debug capability for the ’C6x with external memory without using the DSP hardware.

Each of the simulator software programs simulates the ’C6x operation and allows monitoring of the state of the processor. Key features of the ’C6x simulator include:

- ❑ Execution of user-oriented DSP programs on a host computer
- ❑ Modification and inspection of registers
- ❑ Data and program memory modification and display
- ❑ Simulation of peripherals, caches, and pipelined timings

- Extraction of instruction-cycle timing for device performance analysis
- Programmable breakpoints on instruction acquisition and error conditions
- Single stepping of instructions
- Additional features to the debugger interface
  - Memory-mapped I/O can be connected to a host file to simulate I/O such as synchronous serial port I/O
  - Simulation of external interrupts

Chapter 3

Technical and Third-Party Support

TI support includes a web site, documentation, workshops, seminars, and a hot-line. Third-party support, the products developed by other companies to support TI devices, is also available.

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3.1 Web Site and Documentation

Visit the web site at **www.ti.com/sc/c6x** for information, an interactive multimedia technical overview (MeTO), documentation, and a schedule of 'C6x design workshops. The MeTO describes features of the devices visually with graphics in a point-and-click display for ease of navigation. The web site offers a complete training schedule of design workshops and seminars. Applications assistance and answers to frequently asked questions (FAQ) are available.

Some documentation is available directly from the web site in down-loadable files for printing. There is a complete list of documentation that can be ordered in the preface of this book under *Related Documentation from Texas Instruments*.

3.2 Third-Party Support

TI third-party support continues with the ’C62xx devices. Table 3–1 lists the third-party support contacts with telephone numbers and electronic mail addresses. Table 3–2 lists some of the companies supporting the ’C62xx devices and the product areas.

Table 3–1. Contacts for Third-Party Support

Third-Party Contact	Phone Number	E-mail Address
Ariel Corporation	609–860–2900	ariel@ariel.com
Cheops GmbH & Co KG	+49 8861 2369 0	100541.3370@compuserve.com
D2 Technologies, Inc.	805–564–3424	sales@d2tech.com
DSP Research, Inc.	408–773–1042	info@dspr.com
DSP Software Engineering, Inc.	617–275–3733	info@dspse.com
Eonic Systems, Inc.	301–572–5000	info@eonic.com
GO DSP Corporation	416–599–6868	gdasilva@go–dsp.com
HotHaus Technologies, Inc.	604–278–4300	info@hothaus.com
Innovative Integration, Inc.	818–865–6150	techsprt@innovative-dsp.com
Loughborough Sound Images	+44 0 1509 634444	
Pentek, Inc	201–818–5900	info@pentek.com
Signals & Software Ltd. (SASL)	+44 181 426 9533	davem@sasl.demon.co.uk
Sonitech, Inc.	617–235–6824	info@sonitech.com http://www.sonitech.com
Spectron Microsystems	805–968–5100	info@spectron.com http://www.spectron.com/news/presrel/C6xannce.htm
Spectrum Signal Processing	800–663–8986 or 604–421–5422	sales@spectrumsignal.com http://www.spectrumsignal.com
ViaDSP, Inc.	508–369–0048	dpenny@viadsp.com
White Mountain DSP, Inc.	603–883–2430	info@wmdsp.com

Table 3–2. Third-Party Support Companies and Product Area Supported

Company	Product Area
Ariel Corporation	High-performance VME64 platform and computer telephony products
Cheops GmbH & Co KG	Industrial and medical imaging and high speed/high resolution videoconferencing
D2 Technologies, Inc.	Embedded Voice Processing (EVP™) computer telephony software
DSP Research, Inc.	TIGER development boards and OEM systems
DSP Software Engineering, Inc.	Multi-channel V.34bis soft-modem and telecom software
Eonic Systems, Inc.	Real-time operating systems – Virtuoso Nano™, Classico™, and MicroLite™
Go DSP Corporation	Code Composer™ support and next generation development tool, Code Maestro™
HotHaus Technologies, Inc.	HausWare – DSP software architecture for embedded telecommunications applications
Innovative Integration	PCI6201 DSP coprocessor for telecom, communications and data acquisition applications
Loughborough Sound Images	PCI/C6200 – signal processing platform and PCI/C6220 telecommunications/ high density DSP telephony platform
Pentek, Inc.	Scaleable multi-processor board for the VMEbus – model 9134
Signals & Software Ltd. (SASL)	Very high density ISP modem solution
ViaDSP, Inc.	InvisiLink™ – line of software and firmware for high density computer telephony boards
Sonitech, Inc.	SPIRIT-6000 series of high-performance board-level platforms and software development tools
Spectron Microsystems, Inc.	SPOX real-time operating systems
Spectrum Signal Processing, Inc.	Hardware, interface silicon, and CTI software for DSPs
White Mountain DSP, Inc.	Emulation and multiplatform debug support – Mountain–510, Mountain–510/WS and Mountain-510/LT PCMCIA Card

Appendix A

Glossary

A

address: The number representing a particular memory or peripheral storage location.

ALU: *Arithmetic logic unit.* The high-speed CPU circuit that performs arithmetic and logic operations. Numbers are transferred from registers into the ALU for calculation, and the results are sent back to a register.

ASIC: *Application-specific integrated circuit.* A custom chip designed for a specific application. It is designed by integrating standard cells from a library.

assembler: A software program that creates a machine-language program from a source file that contains assembly language instructions, directives, and macro definitions. The assembler substitutes absolute operation codes for symbolic operation codes, and absolute or relocatable addresses for symbolic addresses.

assembly optimizer: A software program that optimizes linear assembly code, which is assembly code that has not been register-allocated or scheduled. The assembly optimizer is automatically invoked with the shell program when one of the input files has an .sa extension.

B

boot loader: A built-in segment of code that transfers code from an external source to program memory at power up.

C

clock cycles: A repeated set of events based on the input from the external clock.

code: A set of instructions written to perform a task; a computer program or part of a program.

CPU: *Central processing unit.* The computing part that coordinates the functions of a processor.

D

data memory: Memory accessed through the ’C6x RAM interface.

DMA: *Direct memory access.* The mechanism by which an external device or peripheral can access the processor memory to transfer data without the processor having to execute data movement instructions.

DRAM: *Dynamic random access memory.* The most common type of computer memory, usually using one transistor and a capacitor to represent a bit. The capacitors must be energized hundreds of times per second to maintain the charges and lose their content when the power is removed.

E

EMIF: *External memory interface*. The boundary between the CPU and external memory through which information is conveyed.

execute packet: A set of instructions that execute in parallel.

external interrupt: A hardware reset triggered by a pin.

F

fetch packet: A packet containing up to eight instructions held in memory for execution by the CPU.

functional unit: An operational portion of the CPU used to compute a result.

G

global interrupt enable (GIE): A bit in the control status register (CSR) that is used to enable or disable maskable interrupts.

H

hardware interrupt: A suspension of the processor triggered through physical connections with on-chip peripherals or external devices.

HPI: *Host port interface.* A 16-bit wide access port through which a host (external) processor can read from and write to internal data memory.

I

interrupt: A condition caused either by an event external to the CPU or by a previously executed instruction. It forces the current program to be suspended and causes the processor to execute an interrupt service routine corresponding to the interrupt.

L

latency: The delay between when a condition occurs and when the device reacts to the condition. Also, in a pipeline, the necessary delay between the execution of two instructions to ensure that the values used by the second instruction are correct.

LSB: *Least significant bit*. The lowest order bit in a word.

M

maskable interrupt: A hardware interrupt that can be enabled or disabled through software.

memory interleaving: A category of techniques for increasing memory speed.

MIPS: *Million instructions per second*. A unit of execution speed of a computer.

MSB: *Most significant bit*. The highest-order bit in a word.

N

NMI: *Nonmaskable interrupt*. An interrupt that can be neither masked nor disabled.

O

overflow: A condition in which the result of an arithmetic operation exceeds the capacity of the register used to hold that result.

P

parallelism: The ability to extract multiple instructions from an algorithm that can be executed at the same time.

pipeline: A method of executing instructions in an assembly-line fashion.

pipeline processing: A category of techniques that provide simultaneous, or parallel, processing within the computer. It refers to overlapping operations by moving data or instructions into a conceptual pipe with all stages of the pipe processing simultaneously.

PLL: *Phase-locked loop.* A unit within a system that uses phase to lock on to a signal to ensure synchronous clocking of digital signals.

R

RAM: *Random-access memory.* The primary workspace of a computer or processor. Random means that the contents of each byte can be directly accessed without regard to the bytes before or after it. RAM chips require power to maintain their content.

register: A group of bits used for temporarily holding data or for controlling or specifying the status of a device.

reset: A means of bringing the CPU to a known state by setting the registers and control bits to predetermined values and signaling execution to start at a specified address.

RISC: *Reduced instruction set computing.* A computer architecture that minimizes chip complexity by using simple instructions.

S

SBSRAM: *Synchronous burst static random-access memory.*

SDRAM: *Synchronous dynamic random-access memory.* A high-speed memory that can transfer bursts of noncontiguous data at 100M bytes per second.

shifter: A hardware unit that moves bits in a word to the left or to the right in relation to the current position.

V

VelociTI: Architecture developed by TI that features very long instruction words

VLIW: *Very long instruction word.* Architecture using words between the sizes of 256 bits and 1024 bits.

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