

# ***TMS320 DSP Development Support Reference Guide***

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# Read This First

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### ***About This Manual***

The *TMS320 DSP Development Support Reference Guide* details the extensive development support available from TI for the TMS320 family of digital signal processors. As a reference manual, it provides helpful and essential information to assist you in selecting the proper TI tools for design and development of TMS320 applications.

More than 250 third-party suppliers provide development support tools and application hardware/software that supplement the TI DSP products and tools. Information on those offerings is provided in the *TMS320 Third-Party Support Reference Guide* (literature number SPRU052).

### ***How to Use This Manual***

The chapters and appendices that make up this book provide detailed reference information on the TMS320 family of DSPs. The information is arranged in the following manner.

Chapter 1, *Introduction*, outlines the advantages and applications of DSP technology. This chapter also gives an overview of TI DSPs and lists the development support products for the TMS320 family.

Chapter 2, *Selection Guide*, presents an overview of the TI DSP offerings and a listing of the TMS320 digital signal processors now available. Also included in this chapter are tables detailing part information, typical TI DSP applications, and performance benchmarks for the TMS320 DSPs.

Chapters 3 through 12 describe the TMS320 family of digital signal processors according to generation. Included in each chapter are the key features of the devices.

Chapter 13, *Mixed Signal Products*, describes products that provide interfaces for DSP solutions: analog-to-digital converters, digital-to-analog converters, and analog interface circuits.

Chapter 14, *Customizable DSPs (cDSP™)*, provides the attributes, benefits, and key features of these joint customer- and TI-designed DSPs that enable custom solutions for specific applications.

Chapter 15, *Code Generation Tools*, provides an overview of software development. A discussion of software development products includes information on the TMS320C2x/C2xx/C5x, the TMS320C54x, TMS320C3x/C4x, and TMS320C8x C compilers and the TMS320 macro assembler/linker.

Chapter 16, *System Integration and Debugging Tools*, gives the reader an overview of the integration and debugging process. This chapter also discusses system integration and debugging products such as the TMS320 debugger's interface (C/assembly source debugger) and the TMS320 software simulators and emulators. Chapter 15 also covers system integration and evaluation tools, TMS320C2x/C3x/C5x DSP starters kits (DSKs), TMS320 XDS upgrade packages, and the parallel processing development system (PPDS) for the TMS320C40.

Chapter 17, *TMS320 Technical Support*, provides an overview of the technical literature and technical assistance. The chapter's technical literature overview covers application reports, data sheets, the TMS320 newsletter (*Details on Signal Processing*), product bulletins, technical articles, user's guides, and textbooks. The overview of the technical assistance covers the TMS320 Hotline, FAX capabilities, and the TMS320 Bulletin Board Service (BBS).

Chapter 18, *TMS320 Third-Party Support*, covers the TMS320 Software Cooperative and the third-party reference guide for development products. Included is a listing of third-party algorithms currently available and information on how to license third-party software. This chapter also lists the third-party companies and consultants who support the TMS320 DSP family.

Chapter 19, *TMS320 Seminars and Workshops*, covers seminars and 3-day (or longer) workshops offered by the TI Technical Training Organization (TTO). The chapter discusses design assistance services offered by the TI worldwide Customer Design Centers and lists their offices and addresses.

Chapter 20, *TMS320 University Program*, presents an overview of TMS320 code-generation, system-integration, and debugging tools available to universities. Additionally, it lists textbooks on DSP theories and applications using the TMS320 devices and discusses how to establish a DSP lab/research environment.

Appendix A covers *Factory Repair and Exchange Instructions*, while Appendix B presents the *Program License Agreements*. Appendix C discusses the *ROM Codes*, and Appendix D covers *TMS320 PROM Programming*.

## Notational Conventions

This document uses the following conventions.

- Program listings, program examples, and interactive displays are shown in a `special typeface` similar to a typewriter's. Examples use a **bold version** of the special typeface for emphasis; interactive displays use a **bold version** of the special typeface to distinguish commands that you enter from items that the system displays (such as prompts, command output, error messages, etc.).

Here is a sample program listing:

```
0011 0005 0001      .field    1, 2
0012 0005 0003      .field    3, 4
0013 0005 0006      .field    6, 3
0014 0006           .even
```

Here is an example of a system prompt and a command that you might enter:

```
C:  csr -a /user/ti/simuboard/utilities
```

## Related Documentation From Texas Instruments

Texas Instruments provides extensive documentation to support the TMS320 family devices and development tools. The *TMS320 DSP Product Overview* (SPRZ094) and *TMS320 Digital Signal Processing Solutions Selection Guide* (SSDV004) are prime sources of information. See Chapter 17 of this book, *TMS320 Technical Support*, for complete lists of related materials.

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**Note:** When calling a Literature Response Center to order documentation, please specify the literature number of the book.



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# Introduction

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Since the first TMS320 DSP was introduced in 1982, Texas Instruments has been dedicated to the advancement of digital signal processing technology and its applications. TI recognizes that fast time to market, increased productivity, and design ease are of primary importance in the development of DSP-based applications. Therefore, TI offers an innovative, comprehensive program of development support for TMS320 DSPs to facilitate the design process from system concept to production.

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## 1.1 Why Use TI DSPs?

Since the introduction of the first TMS320 digital signal processor, the TMS320 family has established itself as the industry standard. The following list of characteristics highlights the advantages of designing with DSPs over other micro-processors:

- ☐ High-speed number crunching
- ☐ Real-time performance, simulation, and emulation
- ☐ Flexibility
- ☐ Reliability
- ☐ Increased system performance
- ☐ Reduced system cost

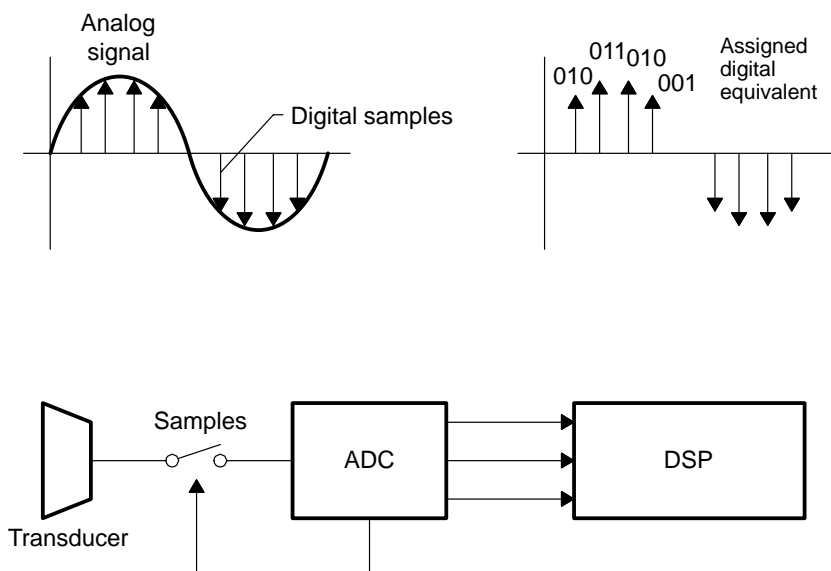
The advantages of the TMS320 family of DSPs are as follow:

- ☐ Broad portfolio
- ☐ Market leaders in solutions
- ☐ Manufacturing strength and commitment
- ☐ Mixed-signal support devices
- ☐ Wide variety of packaging options
- ☐ Better support from concept to completion
- ☐ Low-cost starter kits and evaluation modules
- ☐ Cycle-accurate simulators
- ☐ Optimizing high-level-language compilers
- ☐ Debuggers
- ☐ Real-time scan-based emulators
- ☐ Application software library
- ☐ Technical hotline and bulletin board service
- ☐ Third-party support
- ☐ DSP Solutions web site, including TI & ME Internet Information Service, DSP On-Line Lab™, and Hotline On-Line™

## 1.2 From the Real World: DSP Technology

The natural environment that we wish to interpret is analog. Signals vary continually with time and may feasibly take any value. The digital domain is fixed between two values: high and low. Conversion from the analog domain to the digital domain (and back) is essential to sense signals, manipulate them, and reintroduce them to the environment. The advantages gained from digital manipulation justify the conversion. Special devices that perform this conversion are manufactured to interface with DSPs. These devices are called analog-to-digital (A/D) and digital-to-analog (D/A) converters. A binary code is assigned to a periodic sample of an analog signal that is in proportion to its magnitude; this gives a digital representation (see Figure 1–1).

Figure 1–1. A/D-D/A Conversion



Assigning a binary code to an analog signal introduces some error, as there is a limit to the accuracy to which an analog value can be defined. This error is called quantization.

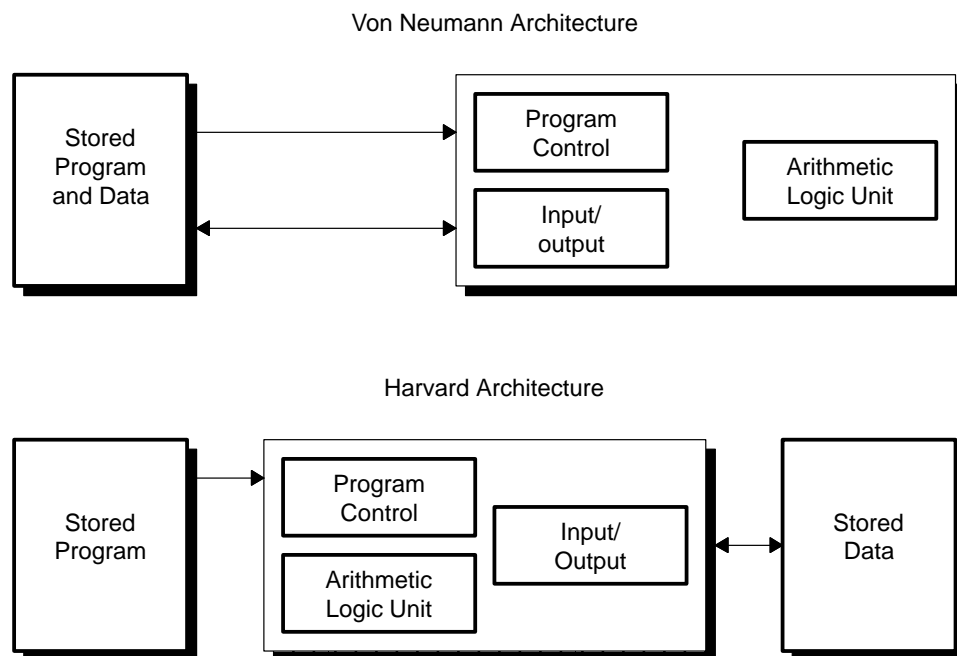
Texas Instruments provides a wide selection of different analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and codecs (coders/decoders). A variety of performance levels and prices ensures that there is a device to suit your application.

### 1.2.1 DSP Architecture

All DSPs consist of several fundamental modules: a digital signal processing core to perform mathematical operations, memory to store data and program instructions, and possibly a mixed-signal product to converse between the analog and digital worlds.

As a stored-program machine, the processor must be told what to do every clock cycle. Typically, a DSP fetches an instruction and some data from memory, operates on these, and then returns the manipulated data to storage. The way this is conducted is not the same for all processors. Two different architectures can be identified: Von Neumann and Harvard (see Figure 1–2). The DSP application, in addition to the memory and peripheral configuration, usually governs the type of architecture employed.

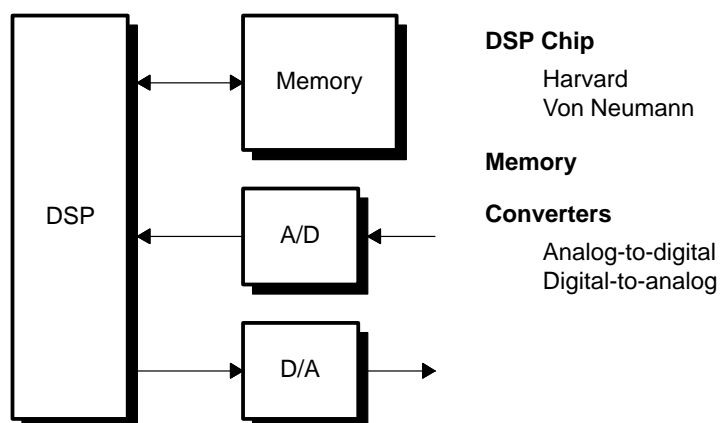
Figure 1–2. Architectures of Digital Processors



Von Neumann architecture has set the standard for computer development over the past 40 years. Essentially, the architecture is very simple. Both program and data can reside in the same memory-mapped space. This architecture forms a basis for more general-purpose processing needs, as seen in the x86 range. The disadvantage with this architecture is that there is only one bus, which shares both data and memory addresses. Therefore, only data space or program space can be accessed in one cycle at any one time.

Where fast data manipulation is vital, accessing both program and data memory in a single cycle is advantageous. Harvard architecture separates the program and data memory spaces. Having two buses to serve each address space ensures that data and program access occurs in parallel, increasing processing speed. Unfortunately, processing power comes with a cost penalty. Two memory spaces require twice as many addresses, and therefore, twice as many data pins. An elegant solution has been found that is a compromise between price and performance. Modified Harvard architecture has only one external bus (thus reducing pin count), yet has both program and data internal buses. Many of the DSPs supplied by Texas Instruments support modified Harvard architecture to reduce cost for the customer while maintaining speed.

Figure 1–3. Typical DSP System



Some of the common features in a typical DSP system (see Figure 1–3) are as follows:

- ☐ A DSP to perform mathematical operations
- ☐ Memory (both on-chip and external) to store data and program instructions
- ☐ Converters to convert signals from analog to digital and from digital to analog

The DSP system may require external memory. In practice, the program to be run is normally held in external memory and then downloaded onto the DSP when the system is started.

### **1.2.2 The Need for Speed**

The main concern for real-time algorithms is the amount of processing that can be done before a new sample arrives. DSP-type algorithms are generically of the form involving a multiply and add operation:

$$A = BC + D$$

The addition function is quite simple for conventional computers and can be performed in a single clock cycle. The same is true of subtraction. Most computers subtract by negating one number and then adding it to the other. Multiply functions take much longer, especially when considering numbers such as  $\pi$ . A general-purpose processor may take several hundreds of clock cycles to implement such a calculation. A machine is needed that can perform a multiply and an add in just one clock cycle. This requires an architecture molded to the specific application. DSPs have hardwired units within the processors for completing a multiply and add within one single clock cycle. Because such multiply and accumulate (MAC) instructions are the fundamental building blocks for many DSP applications, efficient execution is imperative.

Pipelining is an additional method of speeding up the instruction throughput of a processor, rather than speeding up the actual time to execute a single instruction. The simplest analogy is that of a car production line. It might take 10 hours to assemble a complete car, but because the construction of the car is broken down into many subsections, a car might be finished every 10 minutes. Computer instructions can be broken down into stages, such as fetching the instruction, decoding the instruction, fetching any data, executing the instruction, and storing the result. In a way similar to that of a production line, instructions are executed more quickly.

### **1.2.3 Example Architecture**

Programmable DSPs can be categorized into two distinct groups according to their math type: floating point and fixed point. Each has a different architecture that benefits some applications and reduces the effectiveness of others.

- Fixed-point DSPs represent a number in a fixed range with a finite number of bits of precision. For example, a 16-bit processor will give a  $\pm 2^{15}$  range. The earliest DSPs were based on this technology and, for the majority of applications today, the industry chooses 16-bit fixed-point processors. The price advantage gained from fixed-point 16-bit DSPs is significant.

- ❑ Floating-point DSPs express numbers between +1.0 and –1.0 using a mantissa. In addition, the representation also contains a scaling function called the exponent. This method of representation gives a greater dynamic range and therefore reduces the chance of overflow. Floating-point algorithms are well-suited to optimizing high-level-language (HLL) compilers. The reduced quantization error introduced in a 32-bit floating-point processor makes it ideal for audio applications.

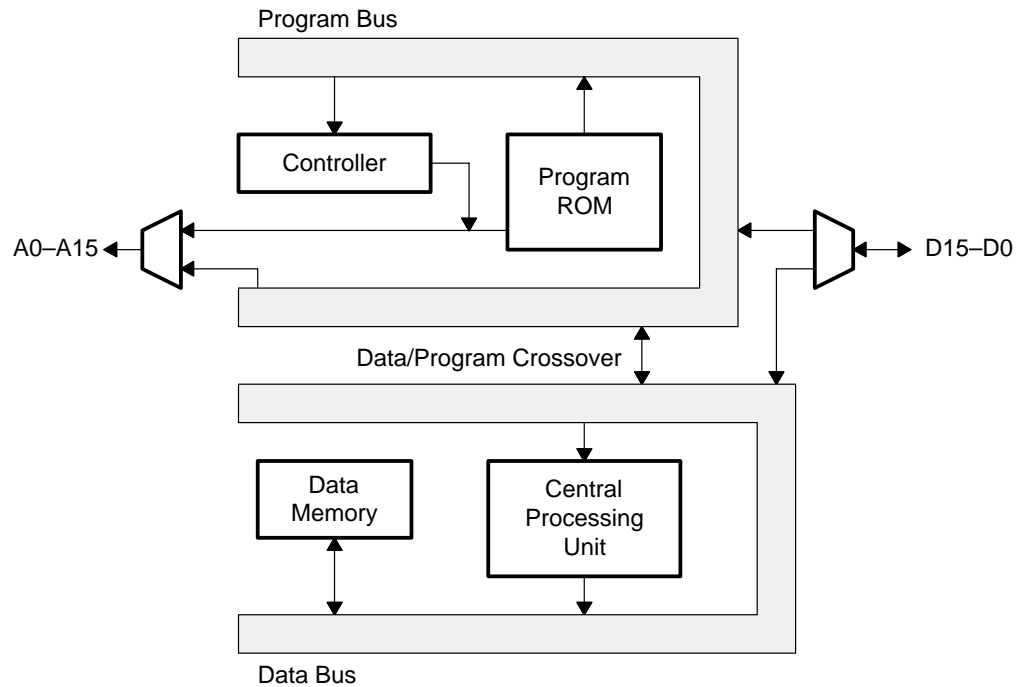
Multiprocessor systems such as the TMS320C80 introduce parallel processing to DSP on one-chip applications. Four fixed-point processors, working independently yet in a coordinated fashion, can process data much more quickly.

Figure 1–4, a simplified block diagram of a fixed-point DSP, shows the separation of data and program buses and the modification giving a crossover between them. Externally, the device could be mistaken for a von Neumann architecture processor, since it only has one set of data and program buses visible. Internally, data and program buses are separated with a crossover. The advantage gained on cost far outweighs the performance penalty.

The architecture is built around two major buses: the program bus and the data bus. The program bus carries the instruction code and immediate operands from program memory. The data bus interconnects various elements, such as the central arithmetic logic unit (CALU) and the auxiliary register file, to the data memory. Together, the program and data buses can carry data from on-chip data memory and internal or external program memory to the multiplier in a single cycle for multiply and accumulate operations.

The device has a high degree of parallelism; that is, while the data is being operated on by the CALU, arithmetic operations may also be executed in the auxiliary register arithmetic unit (ARAU). Such parallelism results in a powerful set of arithmetic, logic, and bit-manipulation operations that may all be performed in a single machine cycle.

Figure 1–4. Example Architecture



The internal hardware of the processor executes functions that other processors typically implement in software or microcode. For example, the device contains hardware for single-cycle 16 x 16-bit multiplication, data shifting, and address manipulation. This hardware-intensive approach provides computing power previously unavailable on a single chip.

## **1.3 Complete DSP Solutions**

Texas Instruments not only designs, manufactures, and markets high-performance DSP semiconductors but also provides customer added value. An established network of customer support is already in place within Texas Instruments for your convenience. Design and training workshops, online help, bulletin boards, and comprehensive documentation are only a few of the ways that we help our customers find a complete DSP solution. We actively encourage the publication of papers in both industry and academic institutions and have substantial third-party support to help you in your projects. In our experience, a partnership with Texas Instruments enables you to extract the most from our products while bringing new and innovative designs to the marketplace.

The commitment of Texas Instruments to the customer is also seen in our range of peripheral products. While the heart of many systems may be the DSP, several devices are frequently required to support the solution. Texas Instruments provides chipsets to complement the most common application solutions, consisting of specifically designed peripherals such as codecs and memories. Such peripherals are designed for our processors, making interfacing simple. As with all Texas Instruments products, these chipsets are backed by our full support and quality assurance.

## **1.4 Typical Applications**

The TMS320 family's unique versatility and real-time performance offer flexible design approaches in a variety of applications. In addition, TMS320 devices can simultaneously provide the multiple functions often required in those complex applications. Table 1–1 lists typical TMS320 family applications.



Table 1–1. Typical Applications of the TMS320 Family

<b><u>General-Purpose DSP</u></b> Digital filtering Convolution Correlation Hilbert transforms Fast Fourier transforms (FFTs) Adaptive filtering Windowing Waveform generation Discrete cosine transforms Hartley transforms  <b><u>Instrumentation</u></b> Spectrum analysis Function generation Pattern matching Seismic processing Transient analysis Digital filtering Phase-locked loops  <b><u>Control</u></b> Disk control Servo control Robot control Laser printer control Engine control Motor control  <b><u>Automotive</u></b> Engine control Vibration analysis Antilock brakes Antiskid brakes Adaptive ride control Global positioning navigation Voice commands Digital radio Cellular telephones Active suspension Noise suppression Electronic power steering 4-wheel steering Air bag control System diagnosis Radar detectors Intelligent cruise control	<b><u>Telecommunications</u></b> Hand-free speaker phones/ echo cancellations ADPCM transcoders Digital PBXs Line repeaters Channel multiplexing 1200- to 33,600-bps modems Adaptive equalizers DTMF encoding/decoding Data encryption Low-speed transcoders/ vocoders ISDN basic/primary rate interfaces FAX Cellular telephones Cordless telephones Digital speech interpolation (DSI) Packet switching and protocol Videoconferencing/video com- pression/multimedia Spread spectrum communications Answering machines Cable modems Network switching Modems  <b><u>Consumer</u></b> Radar detectors Power tools Digital audio/TV Music synthesizer Educational toys Answering machines Multimedia Digital cameras Digital videodisk players White goods (dishwashers, washing machines, etc.) Karaoke Feature phones Arcade games Set top boxes	<b><u>Graphics/Imaging</u></b> 3-D rotation Robot vision Image transmission/ compression Pattern recognition Image enhancement Homomorphic processing Workstations Animation/digital map  <b><u>Voice/Speech</u></b> Voice mail Speech vocoding Speech recognition Speaker verification Speech enhancement Speech synthesis Text-to-speech  <b><u>Industrial</u></b> Robotics Numeric control Security access Power line monitors Active noise cancellation Electronic meters  <b><u>Computers</u></b> Laser printers/copiers Scanner/bar-code scanner Optical character recognition (OCR) Neural networks High-speed array processors Imaging Videoconferencing Modems Networking controller  <b><u>Military</u></b> Secure communications Radar processing Sonar processing Image processing Navigation Missile guidance Radio frequency modems
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## **1.5 Telecommunications Applications**

Telecommunications is one of the fastest growing areas within the electronics market. Decentralization has necessitated more remote business control and collaboration between physically separated business entities. The information age has also generated a thirst for more data, creating the need for fast and effective communications.

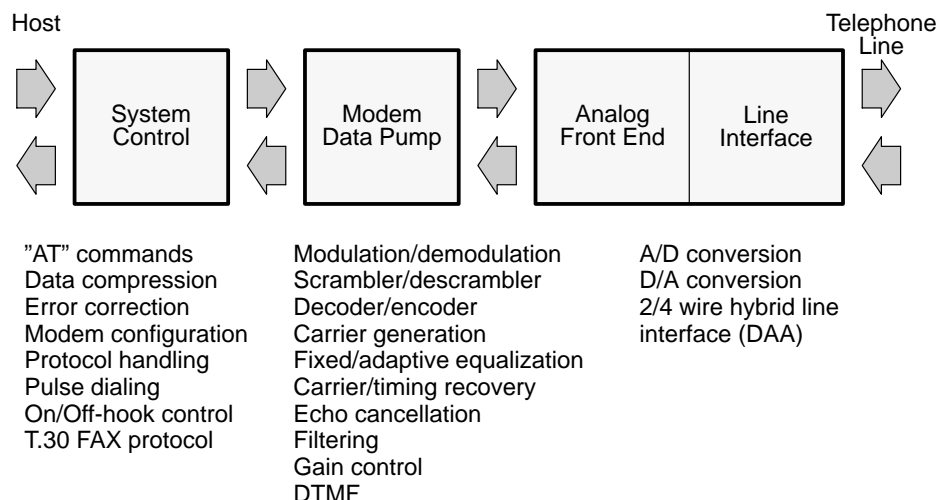
The telecommunications network is under great pressure as more data is being transmitted, and there is always a call for higher data-transmission rates. The high processing power achieved using DSPs provides a natural solution for the demands put on the telecommunications industry. Specific architectural advantages inherent in DSP devices reduce cycle times and operations per function. Consequently, implementing real-time telecommunication solutions relies heavily on DSP products.

### **1.5.1 Modems**

The past decade has seen modem transmission rates increase from 2.8 baud to 14.4 baud. Today, the modem market is rapidly moving toward transmission-rate standards in excess of 28.8 baud. The mathematically intensive calculations inherent in modem design dictate using the most powerful and sophisticated DSP performance levels. Typically, when modem data rates double for a given bandwidth, DSP performance must increase fourfold. Typical modem tasks are shown in Figure 1–5.

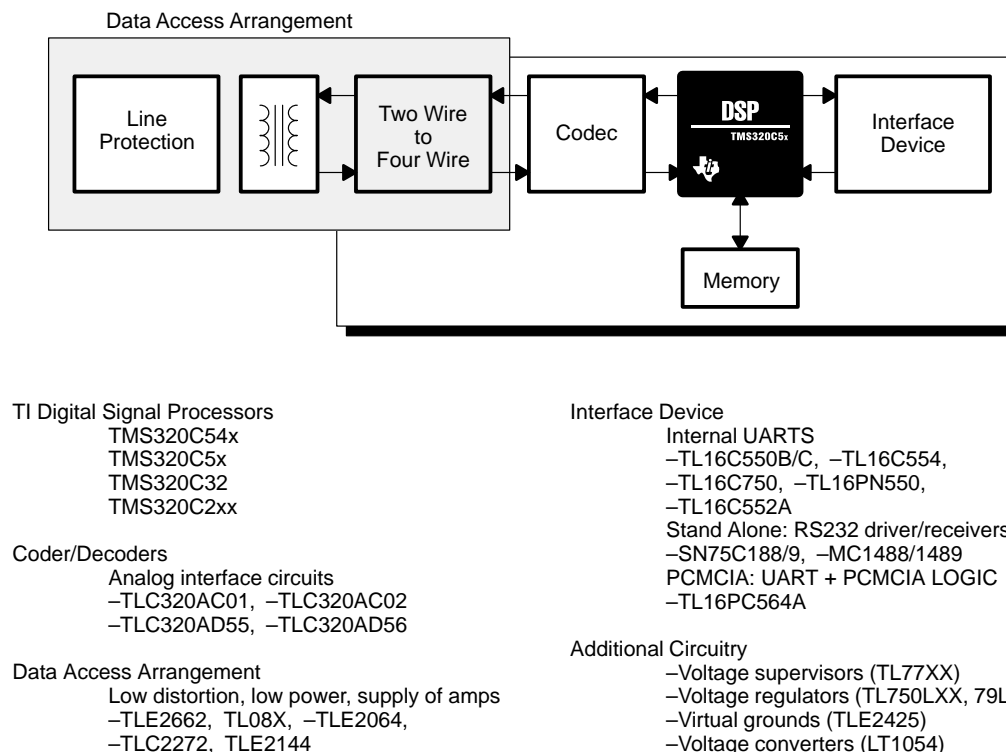
Modem evolution is dominated by the processing power of DSPs to the extent that virtually all modems available today use a DSP or a chipset with an embedded DSP equivalent. Application-specific DSPs and customizable DSP (cDSP™) devices are also being increasingly used in modems for notebook and portable computers, where size, weight, and power consumption are key concerns.

Figure 1–5. Modem Tasks



Originally, modem architectures included a microcontroller to govern the host interface and overall system control functions. Multiple DSPs were also required in parallel to manage baud rates in excess of 19.2 kbps. Today, DSPs from TI can implement a high-speed data modem on a single microchip. A TMS320C5x DSP with approximately 45 million instructions per second (MIPS) can perform both control and data pump functions at 33.6 baud (based on V.34 + standard). A 50-MIPS capacity allows further capabilities, such as voice/data or speakerphone, to be included in the design. Texas Instruments provides a complete modem chipset comprising core processor, codec, and memory to implement the most appropriate solution. Figure 1–6 shows the block diagram of a fax/modem design, which includes the dedicated mixed-signal products from TI.

Figure 1–6. TI Fax/Modem System Solutions



DSPs in modems are not only increasing processing power, they are also saving energy through low-power modes and providing circuit flexibility through high speed, smaller form factors, and greater functionality.

### 1.5.2 ISDN

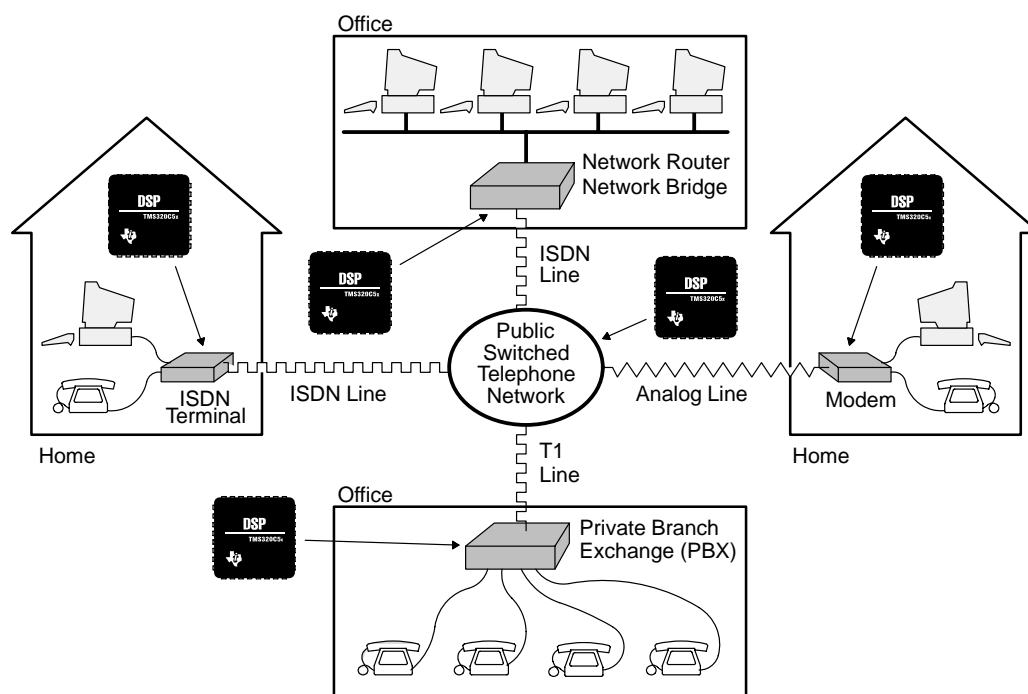
The Integrated Services Digital Network (ISDN) offers a dramatic increase in the speed of data and document transfer at a significantly reduced cost. The speed achieved through ISDN empowers a new breed of applications:

- ☐ Interactive publishing
- ☐ Telecommuting
- ☐ Inexpensive videoconferencing
- ☐ LAN-to-LAN connectivity
- ☐ Teleradiology
- ☐ Remote health care
- ☐ Teleteaching
- ☐ Remote broadcasting
- ☐ Collaborative CAD/CAM engineering

ISDN brings the digital network to the individual user. The same twisted-pair copper telephone line that could traditionally only support one voice or one digital conversation can now carry as many as three separate conversations simultaneously through the same line.

Texas Instruments DSPs provide the necessary processing performance to ensure that the secure connection between multiple devices in the ISDN is maintained. TI DSPs support all the equipment incorporated in the ISDN interface device and in the PSTN (Public Switched Telephone Network), as shown in Figure 1–7.

Figure 1–7. TI DSPs for ISDN Infrastructure

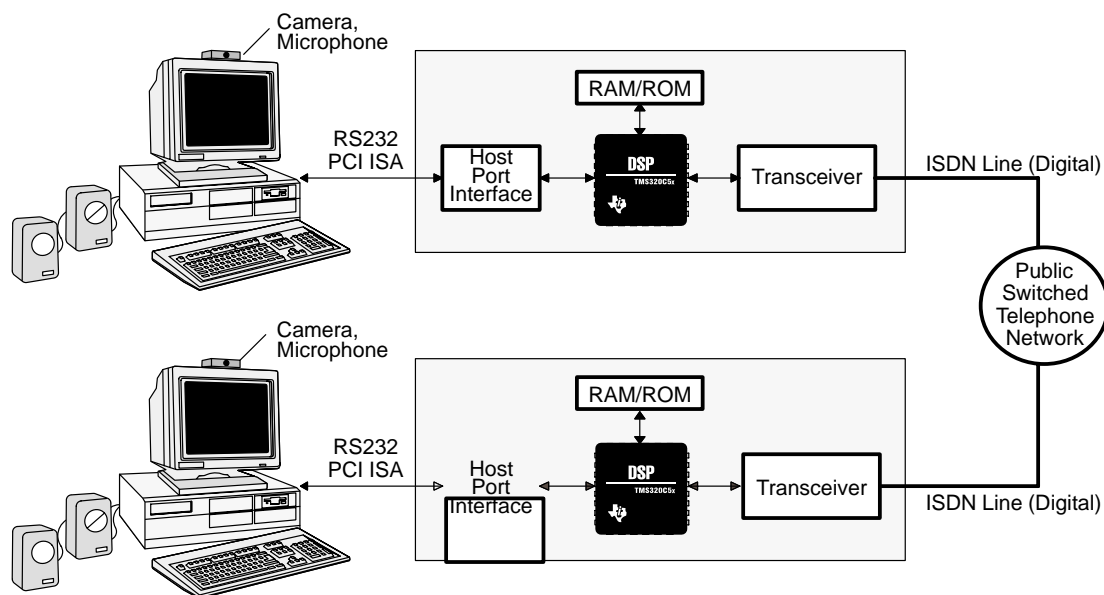


### 1.5.3 ISDN Videoconferencing

The high transmission rates associated with videoconferencing require significant bandwidth. Traditionally, such bandwidth requirements dictated dedicated broad-band lines that often had to be leased. It is now possible, through ISDN, to use videoconferencing without the added expense of leased lines (see Figure 1–8).

A TI third-party (IAT, see Chapter 18, Third Party Support) videoconferencing solution is based on the TMS320C80. The H.320 code is compatible with international videoconferencing services and ISDN videophones. This includes the possibility to run a videoconference with only six single ISDN Basic Rate Service (BRI) connections (six B-channels).

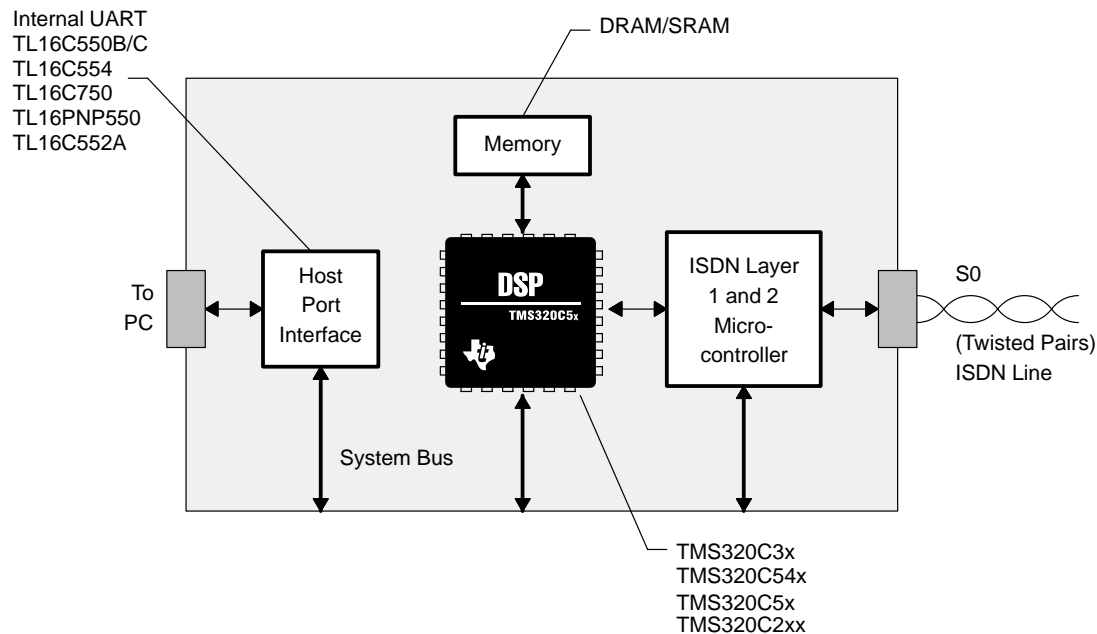
Figure 1–8. ISDN Terminal Videoconferencing



#### 1.5.4 Dual-Mode ISDN Modems

A dual-mode modem (see Figure 1–9) communicates with either an ISDN terminal or an analog modem transceiver. In addition to executing algorithms such as acoustic echo cancellation and ISDN supervisory code, the modem must automatically switch between analog and digital mode. When communicating with an analog modem, the dual-mode modem switches to an analog mode. In this mode, the DSP performs modem modulation and demodulation. However, if the signal is sent through an ISDN, it must be transmitted in digital format, since the ISDN line is digital only.

Figure 1–9. Dual Mode ISDN Modem



TI DSPs can also be used for high-end ISDN telephone sets with features including hands-free function with echo cancellation, high-quality speech compression (G.722), and digital answering machine functions.

## 1.6 Audio Applications

Today, the consumer is demanding increasing functionality and multiple capabilities from electronic products. Computerization has led to digital systems rapidly replacing analog ones, giving better quality, flexibility, and performance. Where processing power limits what is achieved by conventional central processing units, DSPs provides a natural solution to satisfy the demands of the market. In most situations, lack of processing power results in poor quality, slow response time, and single tasking. A dedicated DSP has sufficient real-time processing power to cope with the real-time data manipulation that audio solutions require.

### 1.6.1 Multimedia

Multimedia is being driven by the conversion of traditional analog video signals to digital signals. Movies and video segments are already available on CDs for games, business presentations, and educational purposes. Digital video data will soon be transmitted over cable TV channels, telephone lines, and cellular channels and through satellites. The massive amounts of data generated by digitizing video require high-performance DSPs that reduce storage space and transmission bandwidth for cost-effective delivery of digital video.

Standard multipurpose CPUs work well at directing a variety of host functions; however, they are not well-suited for the multitasking and computing-intensive processing of real-time multimedia. Optimized for processing power, DSPs provide a cost-effective means of off-loading the digital signal processing from host CPUs. Telephone answering, speech and audio processing, sound effects, and music are rapidly becoming standard functions in workstations and PCs. DSPs are designed specifically to execute numeric-intensive tasks like these, where processing information must correspond to real-time events and several tasks are often performed simultaneously.

Texas Instruments offers programmable 16-bit fixed-point and 32-bit floating-point DSPs ranging from 20 MIPS to 2 billion operations per second (BOPS), as well as a family of application-specific MPEG audio and video decoders. Table 1–2 summarizes the compatibility of the TMS320 family with multimedia applications.



Table 1–2. TMS320 Digital Signal Processors for Multimedia

Application	'C3x/'C4x	'C5x	'C54x	'C8x	'AVxxx	Mixed Signal
Modems	X	X	X	X		X
Audio	X	X	X	X	X	X
Speech	X	X	X	X		X
Digital Tapeless Answering Device (DTAD)		X	X	X		X
Graphics/Imaging	X			X		
Video				X	X	X
Videoconference				X		X

#### 1.6.1.1 DSPs for High-Speed Communications

For the cost-sensitive PC market, TI's 16-bit TMS320C5x DSPs offer an optimum combination of price and performance. Fully programmable processors deliver up to 50 MIPS performance. Prices for the 'C5x family of devices start at less than \$10. This processing power provides the freedom to cost-effectively implement very complicated applications, such as transmitting real-time voice and data simultaneously for telegaming and collaborative computing. With the 'C5x DSPs' variety of speed, memory, and peripheral configurations, you will certainly find one to meet your needs.

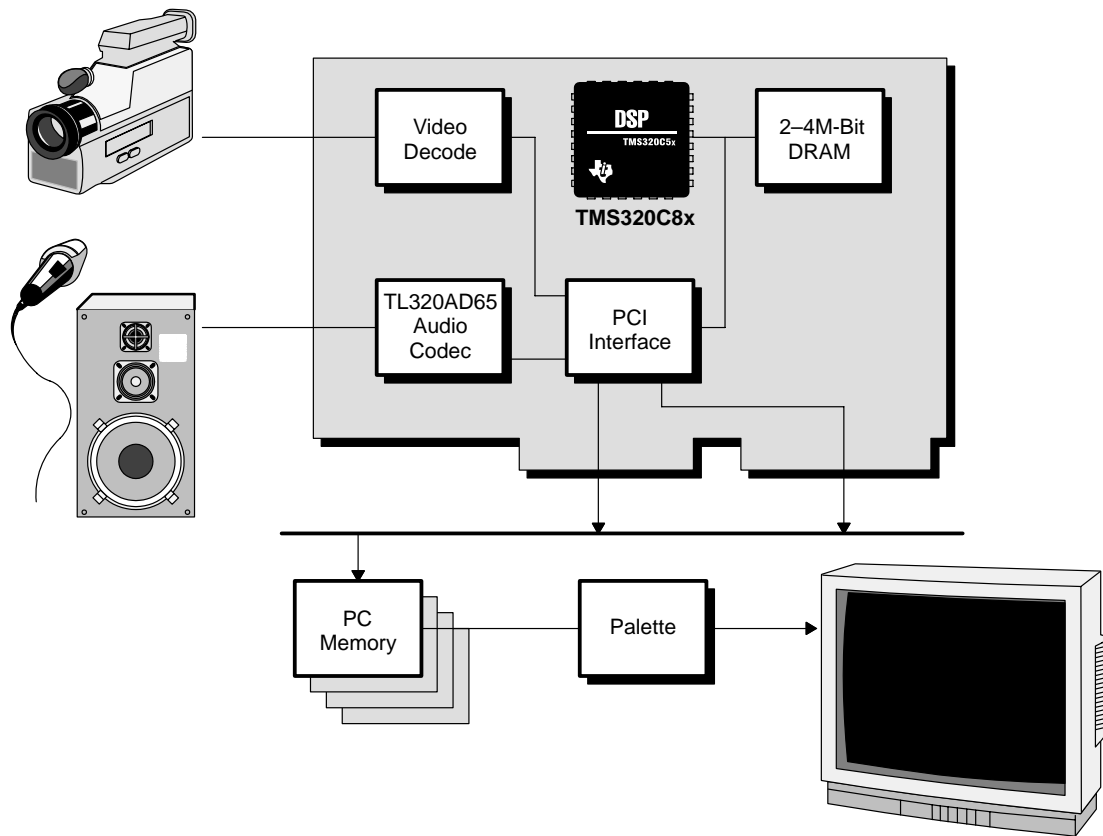
The flexible 32-bit TMS320C32 is designed to bring the benefits of floating-point processing to the desktop. The 'C32 is driving the development of affordable speech and audio subsystems for videoconferencing, integrated voice mail, and video games. With 60 million floating-point operations per second (MFLOPS), 'C32 also has the processing power to execute real-time three-dimensional graphics. High-performance DSPs like the 'C32 will continue to drive the evolution of a user-friendly environment for multimedia:

- ☐ Voiceover data standards
- ☐ V.34 modem/V.17 fax
- ☐ Music synthesis
- ☐ Acoustic echo cancellation
- ☐ Full-duplex speaker phone
- ☐ Speech recognition
- ☐ Vocoders
- ☐ Voice mail
- ☐ Digital telephone answering functions
- ☐ Moving Picture Expert Group (MPEG) audio
- ☐ Joint Photographic Experts Group (JPEG)

The real-time multitasking capability of the 'C80 enables the parallel execution of video and audio encoding/decoding, video scaling, color space conversion, acoustic echo cancellation, filtering, error correction, multiplexing, and bit-stream protocol handling (see Figure 1–10). The 'C80 is the only single-chip DSP solution available today that offers these capabilities. Videoconferencing, Video CD (MPEG-1 or MPEG-2), and collaborative computing are emerging technologies that are supported by the real-time manipulation of multiple data streams offered by the 'C8x. With its full programmability, the 'C80 provides the flexibility to respond to evolving standards and to create products with many features.

The 'C8x generation supports all industry-standard algorithms, such as H.320, MPEG, and JPEG, while offering designers the opportunity to blend their own proprietary algorithms to clearly differentiate their products. To simplify development of 'C8x-based video systems, TI now offers a library of popular functions and standard algorithms, including a complete H.320 software library. Additional standards libraries such as H.324 and imaging/graphics libraries are planned for the future.

Figure 1–10. Multimedia Opportunities



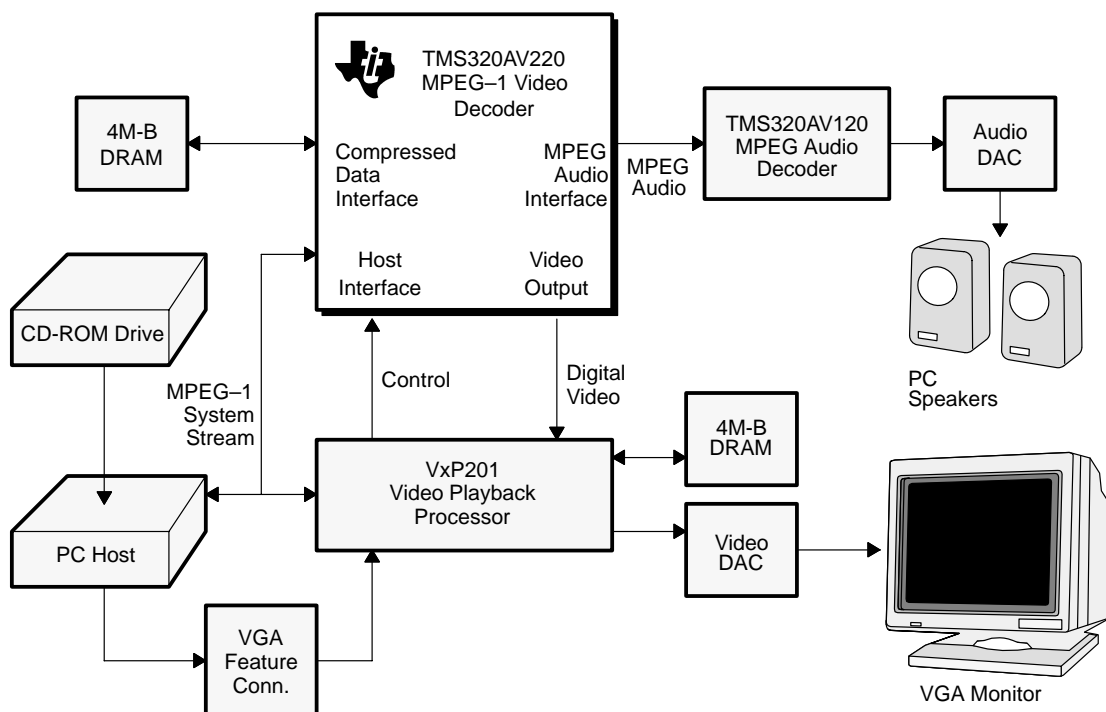
TI's family of TMS320AVxxx application-specific DSPs delivers the required combination of high performance and cost sensitivity. The 'AV110 and 'AV120 provide MPEG audio decoding for applications such as digital broadcast satellite systems, karaoke systems, Video CD players, and PC multimedia cards.

The 'AV220 MPEG-1 video decoder integrates system stream parsing and audio/video synchronization. These features significantly improve the performance of a broad class of full-motion, full-resolution PC video applications.

The Video CD chipset ('AV120/AV220/AV420) provides a complete integrated-circuit solution for the full-motion video subsystem used in VideoCD and karaoke CD applications (see Figure 1–11). The chipset parses, synchronizes, and decompresses MPEG-1 system streams containing audio and video data. The chipset produces CD-quality audio and National Television Standards Committee (NTSC) video without a microprocessor for system control.

The new 'AV411 is a flexible, cost-effective Digital NTSC/PAL encoder that is designed for use in digital set-top boxes and DVD players. The support of multiple input and output data formats, on-chip as well as external sync signal generation, and 16-color on-screen overlay with closed-caption capability provides a video solution for getting from the digital world back to the television format.

Figure 1–11. TI MPEG Solution



#### 1.6.1.2 MSLP 1394: The Standard for Multimedia

Multimedia data on the information superhighway must be processed in an ongoing, real-time manner by the entire system, not just by the DSP or host processor. A proposed IEEE standard (1394) that bridges computer and consumer applications is the emerging protocol for high-speed serial buses in multimedia systems. Other high-speed protocols exist, but only IEEE 1394 provides asynchronous data transfer (guaranteed bandwidth) to address the challenges of manipulating multiple data mediums on a real-time basis.

IEEE 1394 offers other benefits in addition to its guaranteed bandwidth for high-speed data transfer. An obvious advantage for both system designers and consumers is 1394's ability to interface with different types of peripherals. This in effect eliminates the numerous I/O interconnects normally required for peripherals like CD ROM, digital cameras, and printers. With the new standard, separate ports, including the parallel, audio, video, serial power, and SCSI ports, can be consolidated into an IEEE 1394 port — all connected by a single cable.

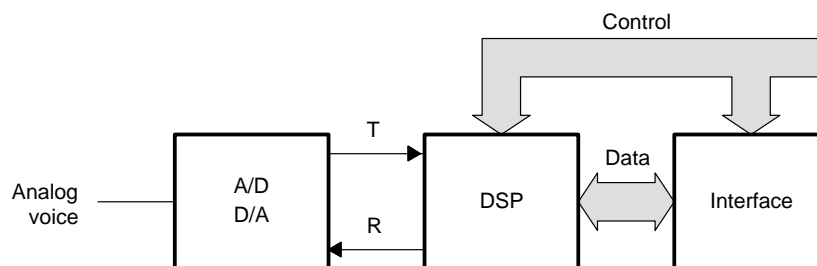
Data on the 1394 serial bus can be moved among a maximum of 63 different peripherals without ever burdening the host processor. This is vital for multimedia applications, where processing power is at a premium. The standard also enables both branching and daisy-chaining of nodes for increased flexibility and true "plug and play" capabilities required for next-generation operating systems.

TI currently offers the industry's first fully-compatible 1394 chipset. One manufacturer, Sony™, has already used the two-chip solution in prototypes for a 1394-based digital camera that will be used for both PC and workstation applications.

## 1.6.2 Speech

The need for embedded processing systems for speech in general-purpose computing machinery is growing fast. Multimedia speech processing applications include recognition, verification, voice mail, and text-to-speech voice processing, all of which are computationally demanding. The solution is to convert analog voice to a digital equivalent and then compress this digital signal for efficient storage and/or transmission. A general speech-processing system is shown in Figure 1–12.

*Figure 1–12. Voice Processing*



### 1.6.2.1 Speech Compression

Representing speech with a minimum number of bits while keeping the highest quality at the lowest cost, all within the application's environmental constraints,

is the challenge of speech compression. Contemporary single-chip DSPs have made implementing real-time speech compression algorithms relatively inexpensive and easy and therefore commercially viable.

In general, high-quality speech compression at low bit rates is accomplished using very complex and computing-intensive coding algorithms. For example, a real-time implementation of a low-rate algorithm may require up to 40 MIPS of DSP processing power. Among the different types of speech coders, two families can be distinguished: waveform coders and parametric coders.

Waveform coders use direct quantization, that is, a binary representation of the speech samples themselves. They often operate in the time domain by quantizing the derivative of amplitude. Parametric coders, however, are based on a mathematical representation of speech model and spectral parameters. Most of the existing standards result from modifications and enhancements of a few different algorithmic approaches including adaptive differential pulse code modulation (ADPCM) and code excited linear prediction (CELP).

Table 1–3 shows different standards in speech coding referring to the performance needs in terms of MIPS on TI DSPs.

*Table 1–3. Speech Coding Standards*

Standard	Data Rate (kbps)	Technique	Encoder MIPS (DSP)
G.711	64	LOG	0–0.5 (C1x, C2x, C3x, C5x)
G.721	32	ADPCM	5 (C1x, C2x, C5x), 4 (BBSP)
G.723	24/32/40	ADPCM	8 (BBSP), 11 (C5x)
G.726	16/24/32/40	ADPCM	8 (BBSP), 11 (C5x)
G.722	48/56/64	ADPCM Band split	7 (C2x, C5x, C3x)
G.728	16	LD CELP	38 (C5x), 16 (C3x)
GSM	13	RPE–LTP	3.2 (C5x), 1.8 (C5xx)
TETRA	7.2	ACELP	≈10 (C5x)
IS-54	7.9	VSELP	18 (C5x), 11 (C5xx)
DOD 4.8	4.8	CELP	10 (C3x)
MPEG	64–256	Perceptive	17 (C3x)
LPC	2.4	LPC	3 (C1x)
LPC	9.6	LPC	4 (C1x)

### **1.6.2.2 Speech Recognition**

Automatic speech recognition lets computer users replace their keyboards with verbal instructions. Until recently, use of such systems, which carry out the user's spoken commands, have been restricted by the limitations inherent in voice recognition technology, as well as by the problems associated with language dialects and noisy environments. However, many of these limitations are being overcome through the use of powerful DSP technology.

Speech recognition is primarily used for telecommunications applications, such as hands-free dialing for cellular telephones and caller identification. Demand is also growing in industrial applications, including visual inspection processes, inventory control, and hands-free operations. Hands-free operations enhance safety in areas where dangerous machinery, toxic chemicals, or high temperatures pose a potential threat to workers. In the event of an emergency, the ability to issue commands to the equipment by voice allows the user to quickly shut down a process without having to search for a shut-down switch. In the multimedia world, speech recognition systems are beginning to allow users to navigate through their PC software applications by voice.

Today, high-performance DSPs are proving to be the enablers for industrial speech-recognition controls. DSPs are 10 to 50 times more powerful than other computer CPUs in terms of their ability to handle tasks as computing-intensive as speech recognition. This level of performance ensures that they can process data in real time. The bandwidth of information is reduced by digitally compressing communications signals. DSPs can process more information to meet the requirements of sophisticated speech recognition systems. For example, in systems requiring a high degree of security, designers can use DSPs in voice recognition systems to compare the user's voice pattern to a prerecorded voice print and grant access only if the two match. In addition, designers can use DSPs with noise-canceling and echo-canceling software to ensure higher degrees of reliability in noisy manufacturing environments.

### **1.6.3 Answering Machines**

An existing Texas Instruments solution for a solid-state answering machine application — the digital tapeless answering machine or DTAD — is based on the chipset containing the MSP58C80 and the MSP58C20. This high-performance mixed-signal processor chipset has incorporated CMOS technology to give low power consumption. With its internal phase-locked loop (PLL), it is capable of running at an internal clock speed of 65.536 MHz by referencing an external oscillator of 4.096 MHz. Designing a DTAD system is simplified by using the glueless logic interface supported by the MSP58C80. The total system component count, and thus the cost, is minimal with a range of peripherals

and advanced built-in DSP algorithms incorporated in the MSP58C80. Further cost saving in speech storage is provided by an internal 4.8-kbps MCELP vocoder, which can achieve close to 15 minutes of recording time using just 4M-bits of audio random-access memory (ARAM).

Texas Instruments DTAD chipset can be driven by an external host MCU. A powerful command set is included as a software interface to the MSP58C80 for implementation of a DTAD system. Programming using this command set is made very simple with the random access feature in the message management commands. The command set also supports direct control over the peripherals in the MSP58C80. Intelligent and flexible data transfer protocol is incorporated in the command set to minimize communication error.

The advantages of a DTAD are as follows:

- ☐ Digital recording with selectable compression rate: MCELP 4.8 kbps and 7.2 kbps
- ☐ Recording time up to 20 minutes per 4 Mbits at 4.8 kbps with silence compression
- ☐ Directs parallel MCU interface (eight data plus four control lines)
- ☐ Supports direct external ROM interface for customized DTS, Voice Menu, or add-on DSP functions
- ☐ On-chip ARAM refresh with direct 4Mx1, 1Mx4, 16Mx1, or 4Mx4 bits ARAM interface
- ☐ 4.096-MHz external crystal with internal PLL
- ☐ Real-time clock function
- ☐ Two 8-bit general-purpose user I/O ports (MSP58C024)
- ☐ Three 8-bit ADC inputs with user-defined thresholds for event monitoring
- ☐ User-programmable single/dual tone generator with adjustable tone level
- ☐ Call progress tone detect for U.S., Germany, France, and United Kingdom
- ☐ Reliable DTMF detect
- ☐ Ring detect with programmable bandwidth
- ☐ Internal day-time stamp with voice clock (English version — male voice)
- ☐ Ease of use and powerful MCU command set
- ☐ Supports up to eight mailboxes



- ☐ Random access of out-going message (OGM) record, playback, delete, and message information retrieval
- ☐ Allows a total of 128 messages in any combination of OGMs, incoming messages (ICMs), or memos
- ☐ Two power-down mode options
- ☐ +5 V single voltage supply
- ☐ 100-pin QFP package with MSP58C80, 20-pin wide body small outline IC (SOIC) with MSP58C20

A typical DTAD is based on the MSP58C80 and the MSP58C20. The MSP58C80 supports a direct interface for an external host MCU and for x1 or x4 ARAM. Its on-chip peripherals also allow direct control for external analog switching, supervision of power supply circuitry, and ring signal detection, so that a solid-state answering machine can be implemented with a minimal component count. The MSP58C20 is a delta-sigma converter that provides analog-to-digital conversion for the MSP58C80. With the MCU version of MSP58C80, you would be shielded from the complexity of the MSP58C80 and be able to impart more flexibility to your products by using separate MCU code.

System architecture cost for stand-alone answering machines can be optimized by suppressing the MCU. All the functions are then taken over by the DSP.

## 1.7 Control Applications

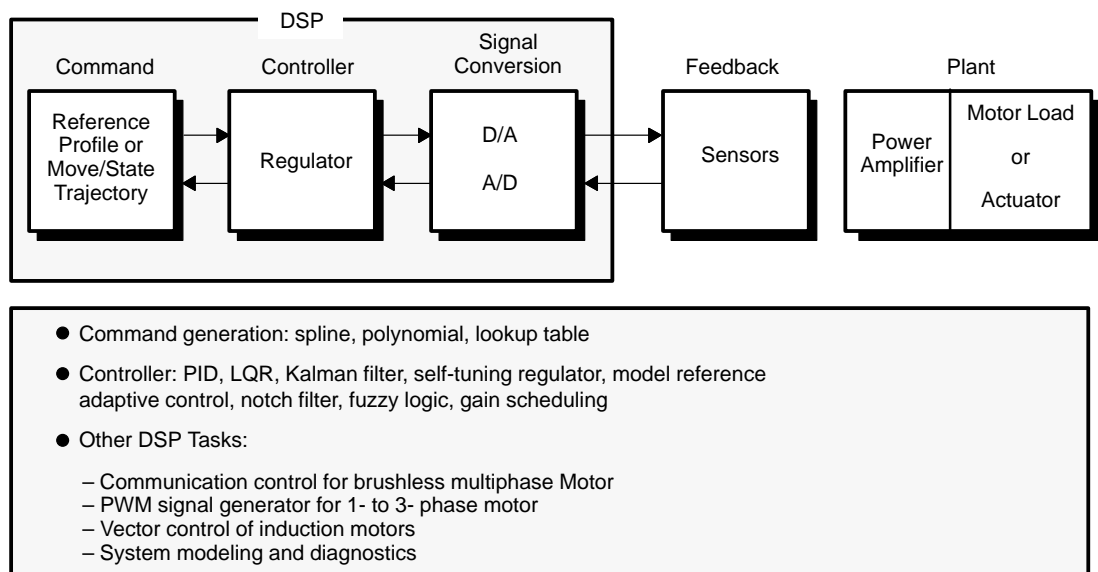
Digital signal processors are probably the most truly embedded of all controllers. Their presence is of little significance to the user, yet their effects are far-reaching. In a world of automation, DSP is becoming increasingly important in applications such as networking, signal reproduction, and power generation. The embedded nature of DSP and the high level of computational power enables control of the most complicated system.

### 1.7.1 Motor Control

Today's generations of automated systems must be designed with environmental consciousness in mind, with more efficient power conservation and a more robust control function implementation. Such systems are now possible through the use of digital motor control technologies (see Figure 1–13).

To address this growing market, TI offers a broad line of semiconductor technology oriented to motor control applications, as well as an extensive selection of development tools and third-party support. Optimized specifically for digital motor and motion control, TI offers the TMS320C24x DSP controllers, as well as other TMS320 digital signal processors. The TMS370 family of micro-controllers and the industry's only family of integrated power switching transistors completes TI's spectrum of motor control solutions.

Figure 1–13. Digital Motor Control



Motor control systems have traditionally been implemented using analog and passive components such as operational amplifiers, resistors, capacitors, and voltage regulators. Alternatively, control may be performed digitally by converting a discrete sample of the analog input signal to a digital equivalent. The input signal is not processed continuously but is sampled at discrete intervals. A sampling interval of at least six to ten times the bandwidth of the system is usually implemented, placing significant performance demands on the system processor.

Due to the high performance and low cost of digital signal processors and micro-controllers, digital motor control systems are replacing analog controllers in today's designs.

Advantages of DSP-based motor control include:

- ☐ Real-time generation of smooth reference and move profiles
- ☐ Integration of memory (lookup tables) or multiple processors into a single DSP
- ☐ Use of advanced algorithms, resulting in fewer sensors and lower system cost
- ☐ Vector control of brushless and induction motors
- ☐ Control of power switching inverters and the generation of high-resolution pulse-width-modulation (PWM) outputs
- ☐ Control of multivariable and complex systems using modern intelligent methods such as neural networks and fuzzy logic

### 1.7.2 Laser Printers and Copiers

The TMS320C8x generation of DSPs can turn the office copier into an intelligent document management station. Desktop scanners already have the ability to read a document into digital form, while laser printers can convert a digital file into a paper copy. Linking these two machines through a microprocessor, as some new small-business-oriented products do today, produces a rudimentary digital copier. Unfortunately, these machines are restricted to making simple copies and usually reproduce images with artifacts introduced by the scanning process.

Digital copiers enhance the reproduction process by applying digital signal processing techniques. By compressing images and storing them on disk, the digital copier increases the reliability and simplifies the process of reproducing multiple collated copies. The use of digital processing for improving on analog and electromechanical methods has existed for some time. However, more revolutionary products will emerge as advanced image/signal processing is applied to do more than simply copy documents.

DSP solutions are the key to the transformation of copiers into document processing workstations. Already, high-performance DSP devices, such as the TMS320C80 and TMS320C3x, offer the processing power to take copying machines to a higher level. The 'C8x brings a unique combination of processing power and flexibility for implementing a versatile document input and output system. The 'C8x's fully programmable architecture allows additional features to be added through software.

A single processor that can handle both image printing and recognition reduces the overall system cost. When scanning a document for faxing, the 'C8x could analyze the document and correct it for rotation, also carrying out the process known as grid stretching in order to send a document. This would eliminate most of the "jaggies" commonly associated with faxed material. Similarly, image processing could clean up a document sent by a machine that did not have "jaggy removal."

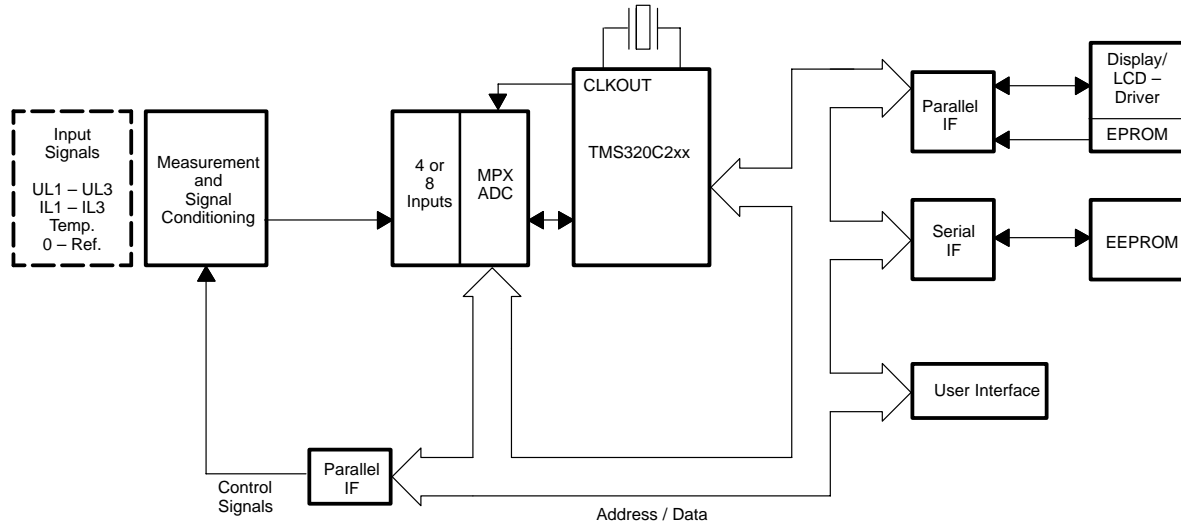
The move to digital processing on high-end, high-volume copiers and color copiers is already prolific. However, much of the digital processing in these products is dedicated to specific copying tasks. These copiers are using digital processing to improve their reliability, ease of use, and image quality.

### **1.7.3 High-End Metering with DSPs**

Programmability, low power consumption, and the advantage of reduced maintenance and operating costs of electronic meters are the driving forces behind the replacement of the Ferrari's wheel meters. DSPs are a key feature of such systems and are suited to high-feature (multitariff) 1-phase or 3-phase meters. These applications require 16- x 16-bit multiply operations in real time at a high sampling rate to measure the harmonic content of the current. Traditional solutions using low-cost controllers would require one microcontroller for each phase, whereas a single DSP can handle all three phases on its own at relatively low clock frequencies.

A DSP solution based on standard devices, such as the 'C2xx, would be as shown in Figure 1-14. The low-power mode and the 16-bit architecture of the 'C2xx family have enabled DSPs to be suitable for high-end metering applications.

Figure 1–14. TMS320C2xx-Based Electricity Meter



With special scanning and computation algorithms, the power consumption of a 3-phase-system load can be measured with minimum error. System calibration, self-checking, and setup menus for system parameter modification are implemented in software.

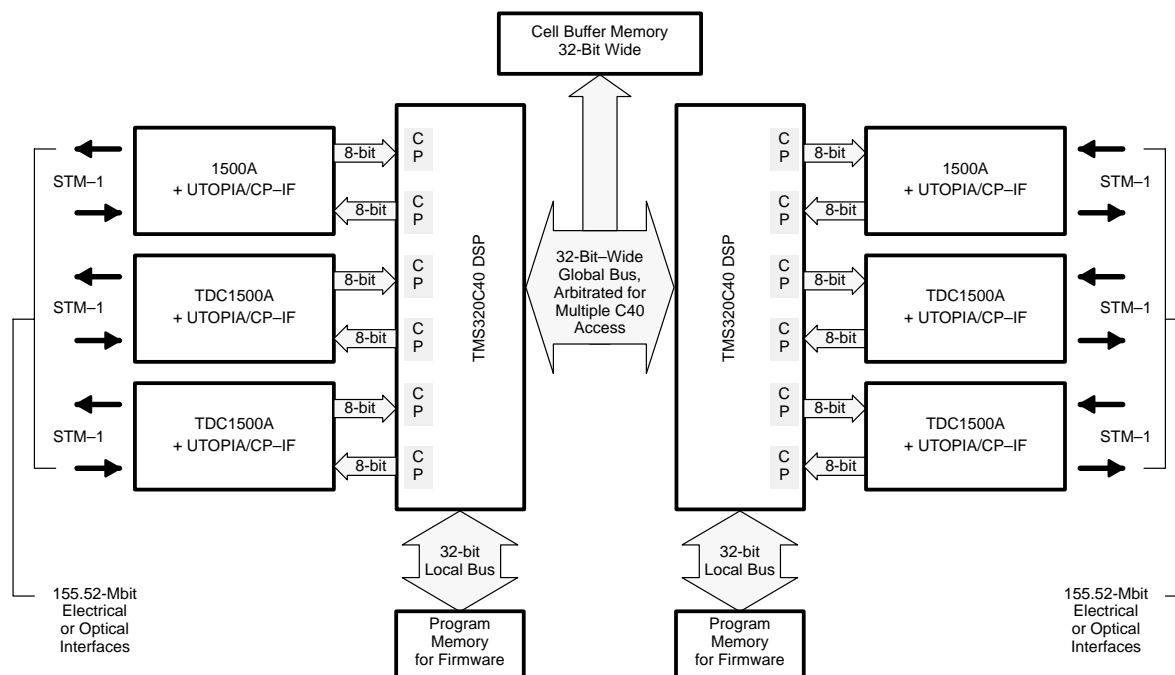
In high-volume applications, a customizable DSP (cDSP) could integrate the interface functions on-chip. These functions include LCD drivers, a remote meter-reading interface, analog-to-digital converters, a smart card interface, and an external memory interface. Such a single-chip solution would result in lower standby currents and improved battery life, thereby reducing maintenance costs.

#### 1.7.4 Networking Controllers

Emerging applications such as videomail, virtual reality, and interactive television require flexible transmission bandwidths. In addition, they must have their own worldwide standards and maintain compatibility with existing systems and networks.

ISDN and multimedia networks must therefore have the capability of transmitting a combination of signals of varying bandwidths simultaneously on the same transmission line. High-performance networks already exist with the capacity to transmit image, voice, and data for these applications cost-effectively and in real time. asynchronous transfer mode (ATM) is becoming the worldwide standard for high-speed data communication. Texas Instruments offers solutions based on standard products like the 'C40 for ATM switching (see Figure 1–15).

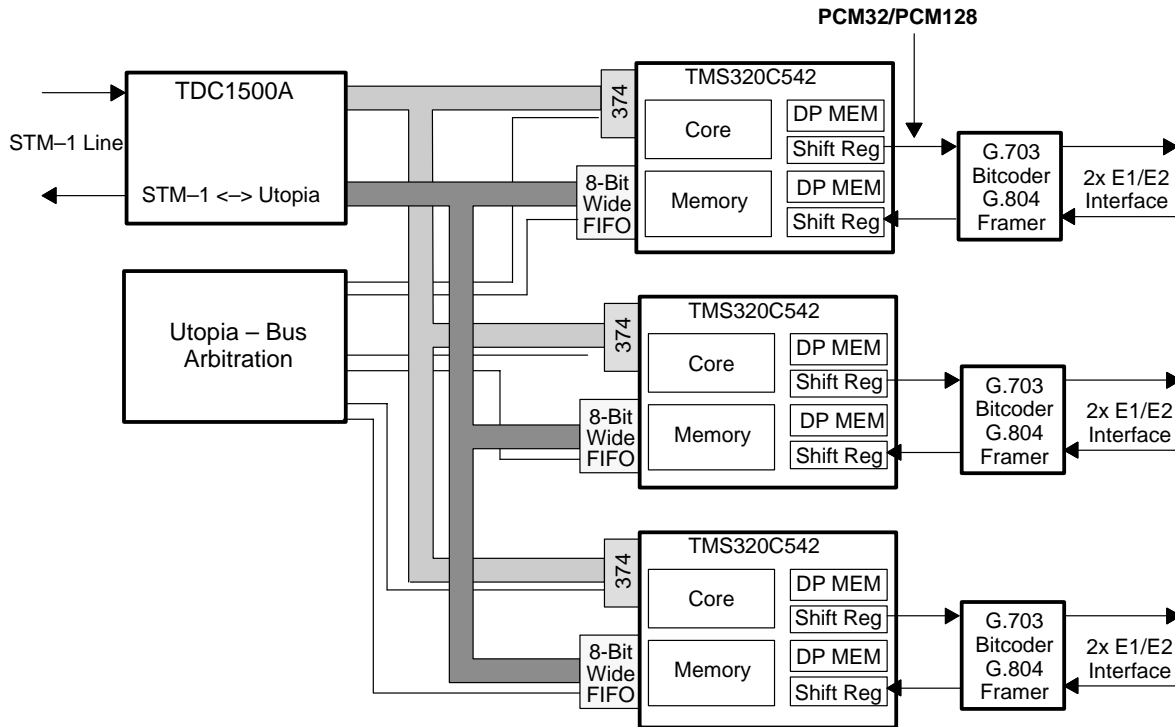
Figure 1–15. ATM Switch Based on a TMS320C40



The data flow to and from the TDCs is controlled via internal direct memory access (DMA) channels. Data bandwidths of 60M bytes/s per 'C40 are achievable with the system. For data exchange to other lines, the 'C40's global bus can be shared by several other processors. Access arbitration, internal data routing, and signaling are all performed with software. The TNETA1500 single-chip line interface to STM-1/STC3c scrambles and descrambles the signal and facilitates framing, idle cell insertion, and extraction. It also generates status messages on dedicated error lines for fast reaction. This configuration allows a fast time to market and can be used as a cheap emulation tool.

DSPs can also be used to connect narrow-band ISDN networks with ATM networks, as shown in Figure 1–16. The 'C542 offers 10K words of on-chip RAM, used for cell buffering. Internal logic interfaces directly to PCM32/PCM128. OAM flow, control flow, and feedback control are performed by software. Connection, rewiring, and software updates are done by OAM cell booting. This configuration allows flexible algorithms like multiple SRTS handling in those areas where specifications are not fully defined.

Figure 1–16. N-ISDN to ATM Switch Based on a TMS320C542



## **1.8 TI DSP Support Overview**

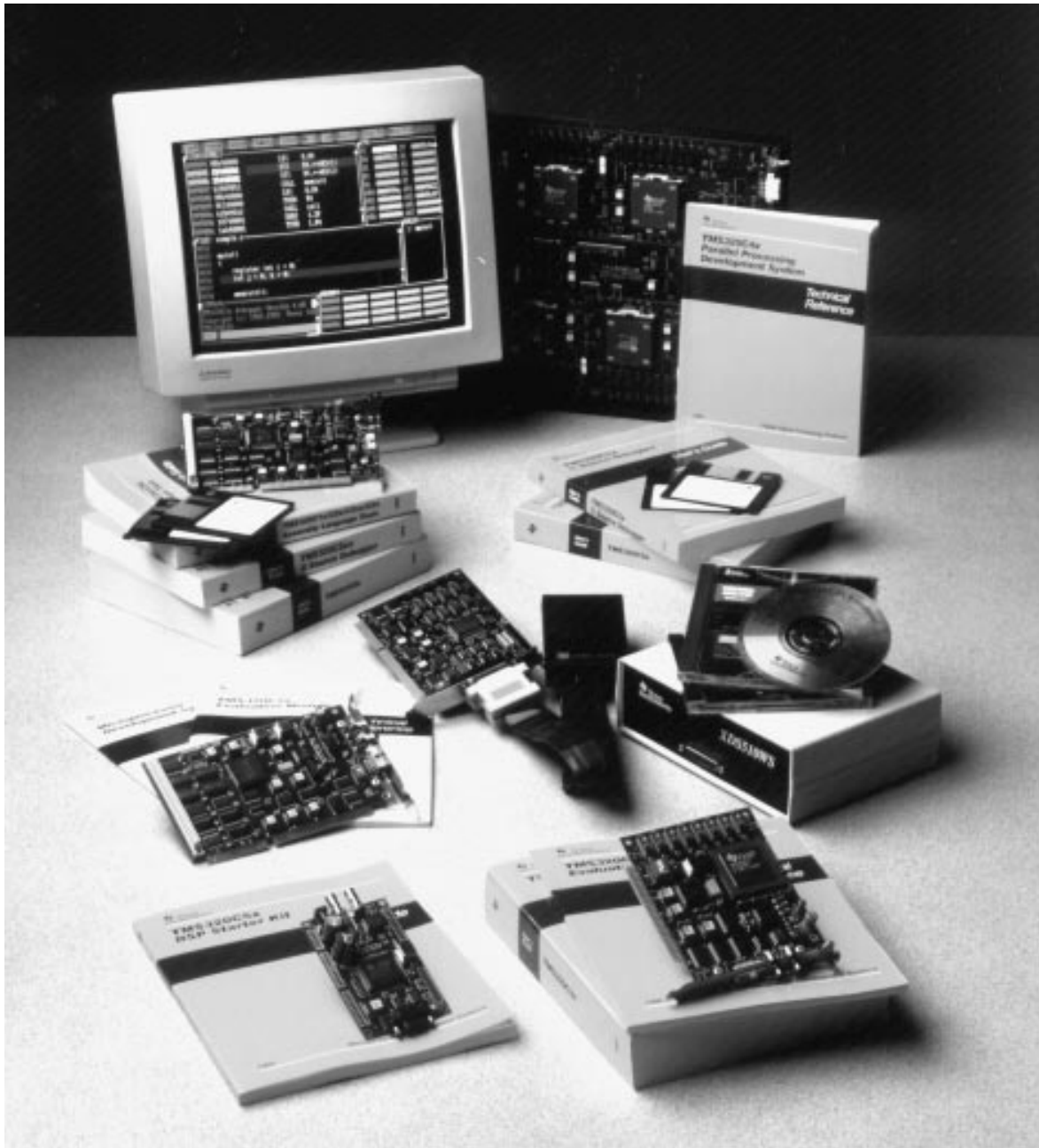
The TMS320 support program includes leading-edge hardware and software development systems from TI and TMS320 third parties: optimizing C compilers, a user-friendly programming interface consisting of C/assembly language source debuggers with code-profiling capabilities, low-cost evaluation tools, simulators, real-time emulators, real-time operating systems, and application software. More than ever, TMS320 DSP users enjoy a development environment that is comparable to the environment available for general-purpose microprocessor systems. Figure 1–17 shows the wide range of development tools available.

Various other support services are also available through the technical hotline, World Wide Web and FTP sites, Bulletin Board Service, field technical staff, and the Technical Training Organization. A library of textbooks and over 2500 pages of application notes provide extensive information about the TMS320 DSP products.

The TMS320 third-party product offerings and consultant services can be found in Chapter 18 of this book.



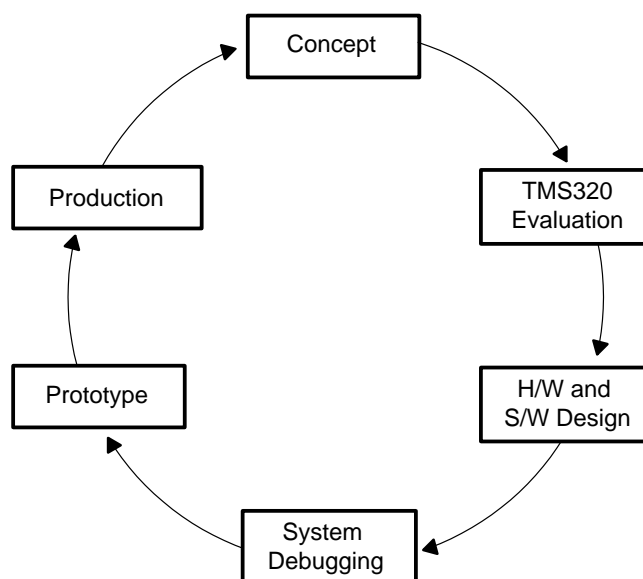
Figure 1–17. TMS320 Family Development Support



## 1.9 TMS320 Development Support Products

Texas Instruments supports designers in complete application development, from concept through production. TI offers an extensive line of development support products to assist you in all aspects of TMS320 design and development. These products range from development and application software to complete hardware integration and debugging systems. Figure 1–18 shows a typical application flow. Products to support this flow are described in the list that follows the figure.

Figure 1–18. Typical TMS320 Application Development Flow

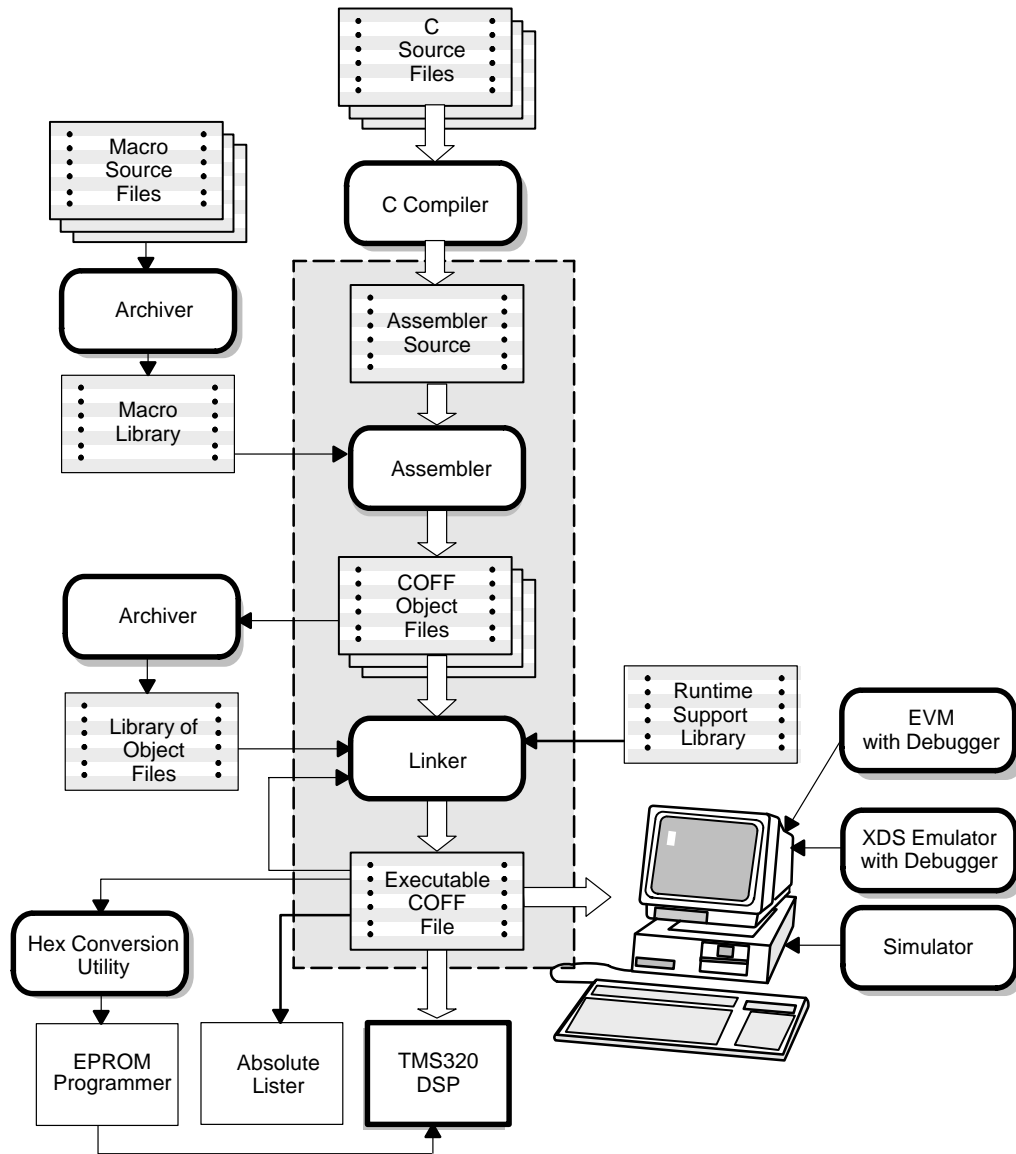


- ❑ **Concept.** Application development for a new or upgraded design often begins with research. TMS320 developers have numerous resources for conceptual designs, including system benchmarks, application notes, algorithms, user's guides, Internet sites, the TI field technical staff, and the DSP hotline.
- ❑ **TMS320 system evaluation.** Support tools for design evaluation include DSP Starter Kits (DSKs), evaluation modules (EVMs), simulators, assembler/linkers, and compilers from TI and from third parties. Using these tools, a developer can benchmark code and determine single or multiple DSP system configurations. TI's extensive documentation provides the necessary information on specifications and capabilities.

- ☐ **Hardware and software designs.** You can design these modules in parallel by using a TMS320 simulator, assembler/linker, compiler, or EVM for software development and by using TMS320 behavioral models and emulators for hardware development. The hotline, Internet sites, and field technical staff offer technical support during this phase; technical documentation and third-party tools are also available.
- ☐ **System Debugging.** Typically, the next phase is integration of the software and hardware modules and debugging of the entire DSP system. You can use emulators and the new source-level debugger at this stage; technical assistance is available from the hotline and/or field technical staff.
- ☐ **Prototype.** When you complete your system prototype, you can submit and/or release your device's ROM code to TI through the BBS. EPROM DSPs provide for early prototype development and smooth the transition to the production phase.
- ☐ **Production.** Once system production begins, you can design a system upgrade. TMS320 family compatibility, a well-defined product migration path, and high-level-language compilers facilitate this phase of the system development cycle.

Figure 1–19 shows development product integration. The appropriate TMS320 support product is indicated for each stage of development. Table 2–13 provides a matrix of the features of the TMS320 simulation/emulation development tools, comparing capabilities such as development purpose and software and hardware features.

Figure 1–19. TMS320 Development Product Integration



# Selection Guide

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Choosing the right DSP for your needs is an important process, and one that can be confusing given the wide range of choices. This chapter is intended to help with the selection process.

Topic	Page
2.1 TMS320 Family Overview .....	2-2
2.2 TMS320 Device Naming Conventions .....	2-4
2.3 TMS320 DSP Overview .....	2-6
2.4 TMS320 Development and Support Tools Overview .....	2-32

## 2.1 TMS320 Family Overview

The TMS320 family consists of 16-bit fixed-point, 32-bit floating-point, and 64-bit multiprocessor single-chip DSPs. These processors have the operational flexibility of high-speed controllers and the numerical capability of array processors. Combining these two qualities, the TMS320 processors are inexpensive alternatives to custom-fabricated VLSI and multichip bit-slice processors. The following characteristics make this family the ideal choice for a wide range of processing applications:

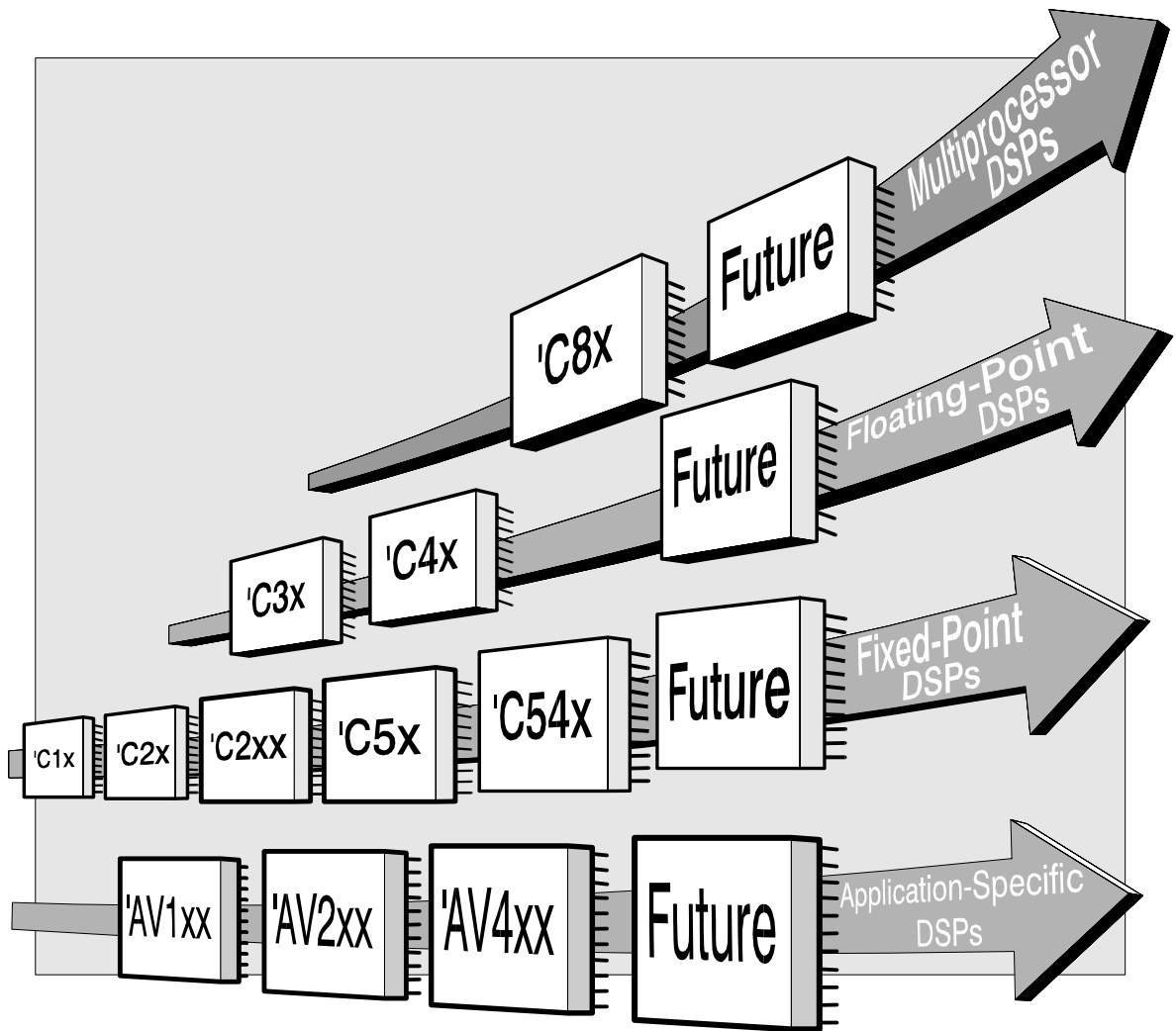
- ☐ Flexible instruction set
- ☐ Inherent operational flexibility
- ☐ High-speed performance
- ☐ Innovative, parallel architecture
- ☐ Cost-effectiveness

In 1982, Texas Instruments introduced the TMS32010—the first fixed-point DSP in the TMS320 family. The TMS32010 became the model for future TMS320 generations.

Today, the TMS320 family (see Figure 2–1) consists of these generations: the 'C1x, 'C2x, 'C2xx, 'C5x, and 'C54x 16-bit fixed-point generations; the 'C3x and 'C4x 32-bit floating-point generations; the 'C8x 64-bit multiprocessor generation; and the 'AVxxx audio/video encoders and decoders. These generations are all complemented by mixed-signal products such as data converters.

Each generation of TMS320 devices has the same CPU structure combined with a variety of on-chip memory and peripheral configurations. New combinations of on-chip memory and peripheral options are used to create spin-off devices that satisfy a wide range of needs in the worldwide electronics market. When memory and peripherals are integrated into one processor, the overall system cost is greatly reduced and board space is saved.

Figure 2–1. The TMS320 Family Road Map



## 2.2 TMS320 Device Naming Conventions

This section explains the nomenclature used in the TMS320 device numbering system.

To classify the stages in the product development cycle, Texas Instruments assigns prefix designators in the part number nomenclature. In addition to the prefix, the device nomenclature includes a two-part suffix that follows the device's family name. This suffix indicates the package type (for example, FN) and temperature range (for example, L). The speed (in MHz), if included, follows the temperature suffix (for example, –40). Figure 2–2 provides a legend for reading the complete nomenclature of any TMS320 family member.

TMX and TMP devices are shipped with the following disclaimer:

**Developmental product intended for internal evaluation purposes.**

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**Note:**

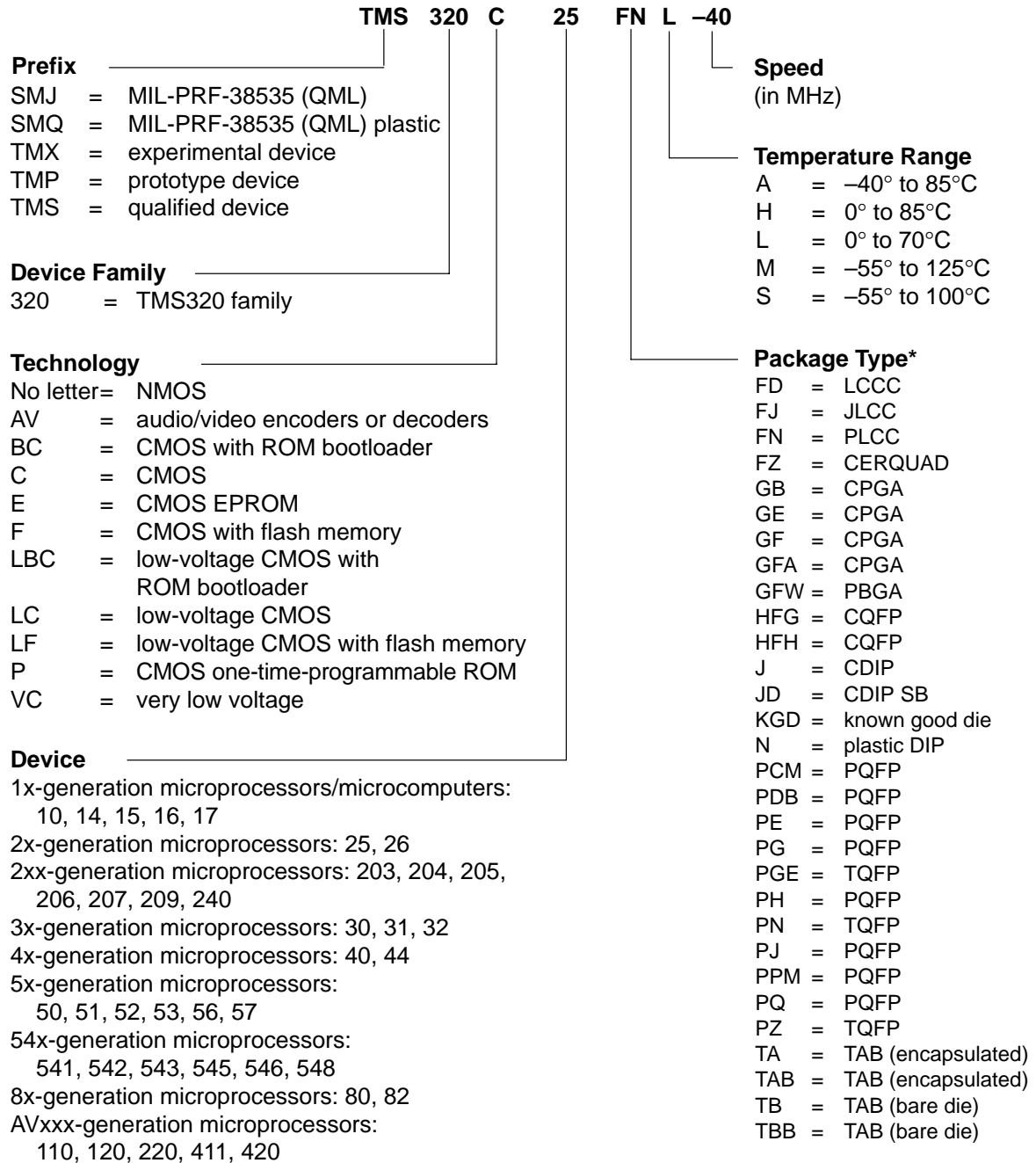
Texas Instruments recommends that prototype devices (TMX or TMP) not be used in production systems, because their expected end-use failure rate is undefined but is predicted to be greater than the failure rate of standard, qualified production devices.

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TMS devices and SMJ devices have been properly tested, and the quality and reliability of the devices have been successfully demonstrated. TI's standard warranty applies.



Figure 2–2. TMS320 Device Nomenclature



**Note:** Questions on availability should be directed to the nearest TI Sales Office, Authorized TI Distributor, or TI Semiconductor Product Information Center (PIC).

## 2.3 TMS320 DSP Overview

The powerful instruction sets, inherent flexibility, and innovative architectural designs have made the TMS320 digital signal processor family the ideal solution for many automotive, computer, consumer, industrial, military, and telecommunication applications. An overview of the TMS320 family (see Table 2–1) consists of the following generations of devices. Further expansion of this family is planned, creating even higher-performing spin-offs and new generations. Presently, the members (by generation) of the TMS320 family are:

- TMS320C1x generation
  - TMS320C10 — a fixed-point, 16-bit DSP with versions that run up to 25 MHz
  - TMS320C14 — a version of the 'C15 with serial ports and timers necessary for control applications
  - TMS320P14 — a one-time-programmable (OTP) version of the 'C14.
  - TMS320C15 — a version of the TMS320C10 with additional on-chip RAM and ROM, with speeds up to 25 MHz
  - TMS320LC15 — a low-power version of the 'C15
  - TMS320P15 — an OTP version of the 'C15
  - TMS320C16 — a fixed-point, 16-bit DSP with 8K words of ROM that runs up to 35 MHz
  - TMS320C17 — a version of the 'C15 with peripherals suited for telecommunications applications
- TMS320C2x generation
  - TMS320C25 — a fixed-point, 16-bit DSP with 544 words of RAM and 4K words of ROM that runs up to 50 MHz.
  - TMS320P25 — an OTP version of the 'C25
  - TMS320C26 — a fixed-point, 16-bit DSP with 1.5K words of RAM that runs at 40 MHz
- TMS320C2xx generation
  - TMS320C203 — a 16-bit, fixed-point DSP with 544 words of on-chip RAM and two serial ports that runs up to 80 MHz. Pin compatible with the 'C204, 'C205, and 'F206
  - TMS320LC203 — a low-power version of the 'C203
  - TMS320C204 — a 16-bit fixed-point DSP with 544 words of on-chip RAM, 4K words of ROM, and two serial ports that run up to 80 MHz. Pin compatible with the 'C203, 'C205, and 'F206

Table 2–1. TMS320 Device Overview

C1x	C2x	C2xx	C3x	C4x	C5x	C54x	C8x	AVxxx
C10	C25	C203	C30	C40	C50	C541	C80	AV110
C14	P25	LC203	C31	C44	LC50	LC541	C82	AV120
P14	C26	C204	LC31		C51	VC541		AV220
C15		F206	C32		LC51	C542		AV411
LC15		C209	LC32		C52	LC542		AV420
P15		C240			LC52	VC542		
C16		F240			C53	LC543		
C17					LC53	VC543		
P17					C53S	LC545		
					LC53S	VC545		
					LC56	LC546		
					LC57	VC546		
					BC57S	LC548		
						VC548		

- TMS320F206 — a 16-bit, fixed-point DSP with 4.5K words of on-chip RAM, 32K words of on-chip flash memory, and two serial ports that runs up to 80 MHz. Pin compatible with the 'C203, 'C204, and 'C205
- TMS320C209 — a 16-bit, fixed-point DSP with 4.5K words of on-chip RAM and 4K words of ROM that runs up to 57 MHz
- TMS320C240 — a 16-bit, fixed-point DSP with an optimized event manager, dual on-chip 10-bit A/D converters, SPI and SCI ports, 16K words of ROM, 28 bidirectional I/O pins, and a watchdog timer
- TMS320F240 — a 16-bit, fixed-point DSP with an optimized event manager, dual on-chip 10-bit A/D converters, SPI and SCI ports, 16K words of flash memory, 28 bidirectional I/O pins, and a watchdog timer

❑ TMS320C3x generation

- TMS320C30 — a 33-million floating-point operations per second (MFLOPS) (33-MHz) floating-point DSP with two memory expansion buses, two serial ports, on-chip ROM, 2K words of on-chip RAM, one channel DMA, and CMOS technology
- TMS320C31 — similar to the 'C30 with one memory expansion bus, no on-chip ROM, 2K words of on-chip RAM, one serial port, a boot-loader, and one channel of DMA
- TMS320LC31 — a low-power version of the 'C31
- TMS320C32 — the lowest-cost version of the 'C3x with a flexible memory interface, 512 words of on-chip RAM, low-power modes, a boot-loader, and two channels of DMA with configurable priorities
- TMS320LC32 — a low-power version of the 'C32

❑ TMS320C4x generation

- TMS320C40 — a high-performance, 330-MOPS, 384 Mbytes/s, 32-bit floating-point, multiport, parallel-processing digital signal processor
- TMS320C44 — a lower-cost version of the 'C40 with four communications ports and a smaller address reach

❑ TMS320C5x generation

- TMS320C50 — a complete system on a single chip. With 2K 16-bit words boot ROM and 10K 16-bit words on-chip RAM, an entire DSP can be integrated into a 132-pin plastic quad flat pack (PQFP).
- TMS320LC50 — a low-voltage version of the 'C50; 3.3-V power supply
- TMS320C51 — in the 'C51, the 'C50's 10K-word block of RAM is replaced by 8K x 16-word ROM. This provides a considerable advantage in cost and performance for users who require large amounts of on-chip program space.
- TMS320LC51 — a low-voltage version of the 'C51; 3.3-V power supply
- TMS320C52 — a superb combination of both low cost and high performance. Traditionally, devices in the same price range have offered 10 million instructions per second (MIPS) performance.
- TMS320LC52 — a low-voltage version of the 'C52; 3.3-V power supply
- TMS320C53 — provides even greater integration of on-chip ROM than the 'C51. With 16K 16-word on-chip ROM and 4K 16-word on-chip RAM, an entire DSP system can be integrated into the 132-pin PQFP.

- TMS320LC53 — a low-voltage version of the 'C53; 3.3-V power supply
  - TMS320C53S — similar to the 'C53 specification with the exception of two standard serial ports, the 100-pin thin quad flat pack (TQFP), and preprogrammed ROM.
  - TMS320LC53S — a low-voltage version of the 'C53S; 3.3-V power supply
  - TMS320LC56 — a 3.3-V device with 32K 16-word on-chip ROM and 7K 16-word on-chip RAM, integrated into a 100-pin TQFP. The communication ports consist of a standard serial port and a buffered serial port (BSP). Available at 35- or 25-ns cycle times
  - TMS320LC57 — similar to the 'LC56 with an additional parallel host port interface (HPI) and a 128-pin TQFP.
  - TMS320BC57S — a 5-V device with 2K 16-word boot ROM and 7K 16-word on-chip RAM. The communication ports are similar to the 'LC57's and consist of a standard serial port, a host port interface, and a buffered serial port.
- TMS320C54x generation
- TMS320C541 — available with an instruction cycle time of 25 ns for 5K words of RAM and 28K-words of ROM and a 5-V power supply
  - TMS320LC541/VC541 — low-voltage versions of the 'C541, available with instruction cycle times of 25 or 20 ns, and 3.3- or 3.0-V power supplies
  - TMS320C542 — available with an instruction cycle time of 25 ns for 10K-words of RAM and 2K-words of ROM and a 5-V power supply
  - TMS320LC542/VC542 — low-voltage versions of the 'C542 available with instruction cycle times of 25 or 20 ns, and 3.3- or 3.0-V power supplies
  - TMS320LC543/VC543 — available with instruction cycle times of 25 or 20 ns, 3.3- or 3.0-V power supplies, and the same memory mix as the 'C542 but with fewer peripherals
  - TMS320LC545/VC545 — available with instruction cycle times of 25 or 20 ns, 3.3- or 3.0-V power supplies, and 6K-words of RAM and 48K-words of ROM
  - TMS320LC546/VC546 — available with instruction cycle times of 25 and 20 ns, 3.3- or 3.0-V power supplies, and the same memory mix as the 'C545 but with fewer peripherals
  - TMS320LC548/VC548 — available with instruction cycle times of 25, 20, or 15 ns, 3.3- or 3.0-V power supplies, and 32K-word RAM and 2K-word ROM

□ TMS320C8x generation

- TMS320C80 — a high-performance 2-billion-operations-per-second (BOPS), 400 Mbytes/s multiprocessor device with up to 400 Mbytes of on-chip memory. The 'C80 offers 50K bytes of static RAM (SRAM) and can handle up to 64-bit instruction words.
- TMS320C80-50 — a 50-MHz version of the 'C80
- TMS320C82 — a cost-effective version of the 'C80 without the video controller, and with only two parallel processors, and with some added features

□ TMS320AVxxx generation

- TMS320AV110—a single-chip ISO-MPEG audio decoder with a low-power, submicron CMOS technology that is fully TTL compatible. Accepts compressed audio at up to 15-Mbps burst rate; has 16- or 18-bit serial PCM output and an 8-bit microprocessor control interface
- TMS320AV120—a low-cost, stand-alone, single-chip ISO-MPEG audio decoder with a low-power, submicron CMOS technology that is fully TTL compatible. Does not require a host microprocessor for initialization or operation, accepts SCR and audio PCR; supports 16- or 18-bit serial PCM data.
- TMS320AV220—a single-chip video CD ISO-MPEG decoder that interfaces directly with the 'AV110, 'AV120, and 'AV420. Automates audio/video synchronization, supports NTSC and PAL™ video output timing formats and SIF and CCIR601 resolution
- TMS320AV411 — a digital NTSC/PAL encoder that has multiple input and output formats. Has three on-chip digital-to-analog converters, on/off-chip synchronization signal generation, closed-caption encoding, and a 16-color overlay with color lookup table. For support of the Macrovision anti-copy function, the TMS320AV410 is available to Macrovision licensees.
- TMS320AV420—a single-chip digital NTSC encoder that has vertical line interpolation of MPEG-1 video. Does not require a host microprocessor or off-chip memory; has on/off-chip synchronization signal generation; has an overlay function for on-screen display; and interfaces directly to the 'AV220

Table 2–2 through Table 2–10 give detailed operating characteristics of the commercial devices. Table 2–11 lists similar information about each military DSP chip.

Table 2–2. TMS320C1x Commercial Devices

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals			Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O					
'C10NL	20	200	5	144	1.5K	–	–	4K	8 × 16	–	–	40 DIP (p)‡	165	0/70
'C10FNA	20	200	5	144	1.5K	–	–	4K	8 × 16	–	–	44 PLCC	165	–40/85
'C10FNL	20	200	5	144	1.5K	–	–	4K	8 × 16	–	–	44 PLCC	165	0/70
'C10NL–25	25	160	6.25	144	1.5K	–	–	4K	8 × 16	–	–	40 DIP (p)‡	200	0/70
'C10FNL–25	25	160	6.25	144	1.5K	–	–	4K	8 × 16	–	–	44 PLCC	200	0/70
'C14FNA	20	160	6.25	256	4K	–	–	4K	7 × 16	1	4	68 PLCC	165	–40/85
'C14FNL	25	160	6.25	256	4K	–	–	4K	7 × 16	1	4	68 PLCC	275	0/70
'P14FNL	25	160	6.25	256	–	4K	–	4K	7 × 16	1	4	68 PLCC	325	0/70
'C15NL	20	200	5	256	4K	–	–	4K	8 × 16	–	–	40 DIP (p)‡	225	0/70
'C15FNL	20	200	5	256	4K	–	–	4K	8 × 16	–	–	40 PLCC	225	0/70
'C15NA	20	200	5	256	4K	–	–	4K	8 × 16	–	–	44 DIP (p)‡	225	–40/85
'C15FNA	20	200	5	256	4K	–	–	4K	8 × 16	–	–	44 PLCC	225	–40/85
'C15FNL–25	25	160	6.25	256	4K	–	–	4K	8 × 16	–	–	40 PLCC	250	0/70
'C15FNL–25	25	160	6.25	256	4K	–	–	4K	8 × 16	–	–	44 PLCC	250	0/70
'LC15FNL	16	250	4	256	4K	–	–	4K	8 × 16	–	–	44 PLCC	50	0/70
'LC15NL	16	250	4	256	4K	–	–	4K	8 × 16	–	–	40 DIP (p)‡	50	0/70
'P15FNL	20	200	5	256	–	4K	–	4K	8 × 16	–	–	44 PLCC	275	0/70
'P15FNL–25	25	160	6.25	256	–	4K	–	4K	8 × 16	–	–	44 PLCC	325	0/70
'P15NA	20	200	5	256	–	4K	–	4K	8 × 16	–	–	40 DIP (p)‡	275	–40/85

† See Figure 2–2 for explanation of device nomenclature.

‡ Plastic package

Table 2–2. TMS320C1x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals			Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O					
'P15NL	20	200	5	256	–	4K	–	4K	8 x 16	–	–	40 DIP (p)‡	275	0/70
'P15NL–25	25	160	6.25	256	–	4K	–	4K	8 x 16	–	–	40 DIP (p)‡	325	0/70
'C16PGL	35	114	8.779	256	8K	–	–	64K	8 x 16	–	–	64 PQFP	300	0/70
'LC16PGL	16	114	8.779	256	8K	–	–	64K	8 x 16	–	–	64 PQFP	100	0/70
'C17FNA	20	200	5	256	4K	–	–	–	6 x 16	2	1	44 PLCC	250	–40/85
'C17FNL	20	200	5	256	4K	–	–	–	6 x 16	2	1	44 PLCC	250	0/70
'C17NA	20	200	5	256	4K	–	–	–	6 x 16	2	1	40 DIP (p)‡	250	–40/85
'C17NL	20	200	5	256	4K	–	–	–	6 x 16	2	1	40 DIP (p)‡	250	0/70
'P17FNL	20	200	5	256	–	4K	–	–	6 x 16	2	1	44 PLCC	275	–40/85
'P17FNL	20	200	5	256	–	4K	–	–	6 x 16	2	1	44 PLCC	275	0/70
'P17FNA	20	200	5	256	–	4K	–	–	6 x 16	2	1	44 PLCC	275	–40/85
'P17NL	20	200	5	256	–	4K	–	–	6 x 16	2	1	40 DIP (p)‡	275	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ Plastic package



Table 2–3. TMS320C2x Commercial Devices

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals			Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O					
'C25FNL	40	100	10	544	4K	–	64K	64K	16 × 16	1	1	68 PLCC	550	0/70
'C25FNL–33	33	120	8.3	544	4K	–	64K	64K	16 × 16	1	1	68 PLCC	450	0/70
'C25GBA	40	100	10	544	4K	–	64K	64K	16 × 16	1	1	68 CPGA	550	–40/85
'C25GBL	40	100	10	544	4K	–	64K	64K	16 × 16	1	1	68 CPGA	550	0/70
'C25FNL–50	50	80	12.5	544	4K	–	64K	64K	16 × 16	1	1	68 PLCC	700	0/70
'C25PHL	40	100	10	544	4K	–	64K	64K	16 × 16	1	1	80 PQFP	550	0/70
'C25PHL–33	33	120	8.3	544	4K	–	64K	64K	16 × 16	1	1	80 PQFP	475	0/70
'P25FNA	40	100	10	544	–	4K	64K	64K	16 × 16	1	1	68 PLCC	550	–40/85
'C26FNL	40	100	10	1.5K	256	–	64K	64K	16 × 16	1	1	68 PLCC	550	0/70

† See Figure 2–2 for explanation of device nomenclature.

Table 2–4. TMS320C2xx Commercial Devices

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals			Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	Package Type		
				RAM	ROM	Flash	Data	Prog	I/O					
'C203PZ	40	50	20	544	BL	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	190	0/70
'C203PZ–57	57	35	28.5	544	BL	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	270	0/70
'C203PZ–80	80	25	40	544	BL	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	380	0/70
'LC203PZ	40	50	20	544	BL	–	64K	64K	64K × 16	2	1	100 TQFP	73	0/70
'LC203PZA	40	50	20	544	BL	–	64K	64K	64K × 16	2	1	100 TQFP	73	–40/85
'C204PZ	40	50	20	544	4K	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	190	0/70
'C204PZ–57	57	35	28.5	544	4K	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	270	0/70
'C204PZ–80	80	25	40	544	4K	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	380	0/70
'C205PZ	40	50	20	4.5K	BL	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	190	0/70
'C205PZ–57	57	35	28.5	4.5K	BL	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	270	0/70
'C205PZ–80	80	25	40	4.5K	BL	–	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	380	0/70
'F206PZ	40	50	20	4.5K	–	32K	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	190	0/70
'F206PZ–57	57	35	28.5	4.5K	–	32K	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	270	0/70
'F206PZ–80	80	25	40	4.5K	–	32K	64K	64K	64K × 16	2	1	100 TQFP (p) ‡	380	0/70
'F207PZ	40	50	20	4.5K	–	32K	64K	64K	64K × 16	3	1	144 TQFP (p) ‡	190	0/70
'F207PZ–57	57	35	28.5	4.5K	–	32K	64K	64K	64K × 16	3	1	144 TQFP (p) ‡	270	0/70
'F207PZ–80	80	25	40	4.5K	–	32K	64K	64K	64K × 16	3	1	144 TQFP (p) ‡	380	0/70
'C209PZ	40	50	20	4.5K	4K	–	64K	64K	64K × 16	–	1	80 TQFP (p) ‡	190	0/70
'C209PZ–57	57	35	28.5	4.5K	4K	–	64K	64K	64K × 16	–	1	80 TQFP (p) ‡	270	0/70
'C240	20	50	20	544	16K	–	64K	64K	64K × 16	2	4	132 PQFP	TBD	–40/85
'F240	20	50	20	544	–	16K	64K	64K	64K × 16	2	4	132 PQFP	TBD	–40/85

† See Figure 2–2 for explanation of device nomenclature.

‡ Plastic package

Table 2–5. TMS320C3x Commercial Devices

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	MOPS	Memory (Words)				Peripherals				Typ Diss (mW)	Temp Range (°C)
					On-Chip			Off-Chip	Serial Port	Timer	DMA Channels	Package Type		
					RAM	ROM	Cache	Parallel						
'C30GEL	33	60	16.667	183.337	2K	4K	64	16M x 32‡	2	2	1§	181 CPGA	1000	0/70
'C30GEL–40	40	50	20	220	2K	4K	64	16M x 32‡	2	2	1§	181 CPGA	1250	0/70
'C30GEL–50	50	60	25	275	2K	4K	64	16M x 32‡	2	2	1§	181 CPGA	1500	0/70
'C30PPM–40	40	50	20	220	2K	4K	64	16M x 32‡	2	2	1§	208 PQFP	850	0/70
'C31PQL	33	60	16.667	183.337	2K	BL	64	16M x 32	1	2	1§	132 PQFP	750	0/70
'LC31PQL	33	60	16.667	183.337	2K	BL	64	16M x 32	1	2	1§	132 PQFP	500	0/70
'C31PQL–40	40	50	20	220	2K	BL	64	16M x 32	1	2	1§	132 PQFP	900	0/70
'LC31PQ–40	40	50	20	220	2K	BL	64	16M x 32	1	2	1§	132 PQFP	700	0/70
'C31PQL–50	50	40	25	275	2K	BL	64	16M x 32	1	2	1§	132 PQFP	1100	0/70
'C31PQL–60	60	33	30	330	2K	BL	64	16M x 32	1	2	1§	132 PQFP	1300	0/70
'C31PQA	33	60	16.667	183.337	2K	BL	64	16M x 32	1	2	1§	132 PQFP	750	–40/85
'C32PCM–40	40	50	20	220	512	BL	64	16M x 8/16/32	1	2	2¶	144 PQFP	900	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ Two external parallel buses

§ Fixed priority

¶ Configurable priority

|| Plastic package

Table 2–5. TMS320C3x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	MOPS	Memory (Words)				Peripherals				Typ Diss (mW)	Temp Range (°C)
					On-Chip			Off-Chip	Serial Port	Timer	DMA Channels	Package Type		
					RAM	ROM	Cache							
'C32PCMA–40	40	50	20	220	512	BL	64	16M x 8/16/32	1	2	2¶	144 PQFP	900	–40/85
'C32PCM–50	50	40	25	275	512	BL	64	16M x 8/16/32	1	2	2¶	144 PQFP	1100	0/70
'C32PCMA–50	50	40	25	275	512	BL	64	16M x 8/16/32	1	2	2¶	144 PQFP	1100	–40/85
'C32PCM–60	60	33	30	330	512	BL	64	16M x 8/16/32	1	2	2¶	144 PQFP	1300	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ Two external parallel buses

§ Fixed priority

¶ Configurable priority

|| Plastic package

Table 2–6. TMS320C4x Commercial Devices

Device Name†	FREQ (MHZ)	Cycle Time (ns)	MIPS	MOPS	Memory (Words)				Peripherals				Typ Diss (mW)	Temp Range (°C)
					On-Chip			Off-Chip	Serial Port	Timer	DMA Channels	Package Type		
					RAM	ROM	Cache	Parallel						
'C40GFL–40	40	50	20	220	2K	BL	128	4G x 32	–	2	6 (12)	325 CPGA	1200	0/70
'C40GFL–50	50	40	25	275	2K	BL	128	4G x 32	–	2	6 (12)	325 CPGA	1500	0/70
'C40GFL–60	60	33	30	330	2K	BL	128	4G x 32	–	2	6 (12)	325 CPGA	1800	0/70
'C44PDB–50	50	40	25	275	2K	BL	128	32M x 32	–	2	6 (12)	304 PQFP	1800	0/70
'C44PDB–60	60	33	30	330	2K	BL	128	32M x 32	–	2	6 (12)	304 PQFP	1800	0/70
'C44GFW–50	50	40	25	275	2K	BL	128	32M x 32	–	2	6(12)	388 BGA		0/70
'C44GFWA–50	50	40	25	275	2K	BL	128	32M x 32	–	2	6(12)	388 BGA		–40/85
'C44GFW–60	60	33	30	330	2K	BL	128	32M x 32	–	2	6(12)	388 BGA		0/70

† See Figure 2–2 for explanation of device nomenclature.

Table 2–7. TMS320C5x Commercial Devices

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals				Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O						
'C50PQ	40	50	20	10K	BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	0/70
'C50PQ–57	57	35	28.57	10K	BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	0/70
'C50PQ–80	80	25	40	10K	BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	825	0/70
'C50PQA	40	50	20	10K	BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	–40/85
'C50PQA–57	57	35	28.57	10K	BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	–40/85
'LC50PQ	40	50	20	10K	BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	155	0/70
'LC50PQ–50	50	40	25	10K	BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	195	0/70
'C51PQ	40	50	20	2K	8K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	0/70
'C51PQ–57	57	35	28.57	2K	8K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	0/70
'C51PQ–80	80	25	40	2K	8K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	825	0/70
'C51PQ–100	100	20	50	2K	8K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	975	0/70
'C51PQA	40	50	20	2K	8K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	–40/85
'C51PQA–57	57	35	28.57	2K	8K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	–40/85
'C51PZ	40	50	20	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	500	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port

Table 2–7. TMS320C5x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals				Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O						
'C51PZ–57	57	35	28.57	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP	650	0/70
'C51PZ–80	80	25	40	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP§	750	0/70
'C51PZA	40	50	20	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP§	500	–40/85
'BC51PQ	40	50	20	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	0/70
'BC51PQ–57	57	35	28.57	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	0/70
'BC51PQ–80	80	25	40	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	825	0/70
'BC51PQ–100	100	20	50	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	975	0/70
'BC51PQA	40	50	20	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	–40/85
'BC51PQA–57	57	35	28.57	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	–40/85
'LBC51PQ–57	57	35	28.57	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	190	0/70
'C51PZ	40	50	20	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP§	525	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port

Table 2–7. TMS320C5x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals				Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O						
'C51PZ–57	57	35	28.57	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	590	0/70
'C51PZ–80	80	25	40	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	825	0/70
'C51PZ–100	100	20	50	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	975	0/70
'C51PZA	40	50	20	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	525	–40/85
'BC51PZ	40	50	20	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	525	0/70
'BC51PZ–57	57	35	28.57	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	590	0/70
'BC51PZ–80	80	25	40	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	825	0/70
'BC51PZ–100	100	20	50	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	975	0/70
'BC51PZA	40	50	20	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	100 TQFP \$	525	–40/85
'LC51PZ	40	50	20	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	155	0/70
'LC51PZ–57	57	35	28.57	2K	8K	–	64K	64K	64K × 16	2‡	1	–	100 TQFP\$	190	0/70
'LBC51PZ	40	50	20	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	155	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port



Table 2–7. TMS320C5x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals			Package Type	Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI			
				RAM	ROM	OTP	Data	Prog	I/O						
'LBC51PZ–57	57	35	28.57	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	190	0/70
'LBC51PZA	40	50	20	2K	8K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	–40/85
'C52PJ	40	50	20	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	525	0/70
'C52PJ–57	57	35	28.57	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	590	0/70
'C52PJ–80	80	25	40	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	825	0/70
'C52PJA	40	50	20	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	525	–40/85
'C52PJA–57	57	35	28.57	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	590	–40/85
'BC52PJ	40	50	20	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	525	0/70
'BC52PJ–57	57	35	28.57	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	590	0/70
'BC52PJ–80	80	25	40	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	825	0/70
'BC52PJA	40	50	20	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	525	–40/85

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port

Table 2–7. TMS320C5x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals			Package Type	Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI			
				RAM	ROM	OTP	Data	Prog	I/O						
'BC52PJA–57	57	35	28.57	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	590	–40/85
'LBC52PJ	40	57	20	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	155	0/70
'LBC52PJ–57	57	35	28.57	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	195	0/70
'LBC52PJA	40	50	20	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 PQFP	155	–40/85
'C52PZ	40	50	20	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP\$	525	0/70
'C52PZ–57	57	35	28.57	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP\$	590	0/70
'C52PZ–80	80	25	40	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP\$	825	0/70
'C52PZ–100	100	20	50	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP\$	975	0/70
'C52PZA	40	50	20	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP\$	525	–40/85
'C52PZA–57	57	35	28.57	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP\$	590	–40/85
'BC52PZ	40	50	20	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 TQFP\$	525	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port

Table 2–7. TMS320C5x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals			Package Type	Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI			
				RAM	ROM	OTP	Data	Prog	I/O						
'BC52PZ–57	57	35	28.57	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	590	0/70
'BC52PZ–80	80	25	40	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	825	0/70
'BC52PZ–100	100	20	50	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	975	0/70
'BC52PZA	40	50	20	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	525	–40/85
'BC52PZA–57	57	35	28.57	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	590	–40/85
'LC52PZ	40	50	20	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	155	0/70
'LC52PZ–57	57	35	28.57	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	190	0/70
'LC52PZA	40	50	20	1K	4K	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	155	–40/85
'LBC52PZ–57	57	35	28.57	1K	4K/ BL	–	64K	64K	64K × 16	1¶	1	–	100 TQFP§	190	0/70
'C53PQ	40	50	20	4K	16K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port

Table 2–7. TMS320C5x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals				Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O						
'C53PQ–57	57	35	28.57	4K	16K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	0/70
'C53PQ–80	80	25	40	4K	16K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	825	0/70
'C53PQA	40	50	20	4K	16K	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	–40/85
'BC53PQ	40	50	20	4K	16K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	0/70
'BC53PQ–57	57	35	28.57	4K	16K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	590	0/70
'BC53PQ–80	80	25	40	4K	16K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	825	0/70
'BC53PQA	40	50	20	4K	16K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	525	–40/85
'LBC53PQ	40	50	20	4K	16K/ BL	–	64K	64K	64K × 16	2‡	1	–	132 PQFP	155	0/70
'C53SPZ	40	50	20	4K	16K	–	64K	64K	64K × 16	2#	1	–	100 TQFP	525	0/70
'C53SPZ–57	57	35	28.57	4K	16K	–	64K	64K	64K × 16	2#	1	–	100 TQFP	590	0/70
'BC53SPZ	40	50	20	4K	16K/ BL	–	64K	64K	64K × 16	2#	1	–	100 TQFP	525	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port

Table 2–7. TMS320C5x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)						Peripherals				Typ Diss (mW)	Temp Range (°C)
				On-Chip			Off-Chip			Serial Port	Timers	HPI	Package Type		
				RAM	ROM	OTP	Data	Prog	I/O						
'BC53SPZ–57	57	35	28.57	4K	16K/ BL	–	64K	64K	64K × 16	2#	1	–	100 TQFP	590	0/70
'BC53SPZ–80	80	25	40	4K	16K/ BL	–	64K	64K	64K × 16	2#	1	–	100 TQFP	825	0/70
'LC53SPZ	40	50	20	4K	16K	–	64K	64K	64K × 16	2#	1	–	100 TQFP	155	0/70
'LBC56PZ–57	57	35	28.57	7K	32K	–	64K	64K	64K × 16	2	1	–	100 TQFP	190	0/70
'LBC56PZ–80	80	25	40	7K	32K	–	64K	64K	64K × 16	2	1	–	100 TQFP	305	0/70
'LBC57PBK–57	57	35	28.57	7K	32K	–	64K	64K	64K × 16	2	1	1	128 TQFP	190	0/70
'LBC57PBK–80	80	25	40	7K	32K	–	64K	64K	64K × 16	2	1	1	128 TQFP	305	0/70
'BC57SPGE–57	57	35	28.57	7K	BL	–	64K	64K	64K × 16	2	1	1	144 TQFP	590	0/70
'BC57SPGE–80	80	25	40	7K	BL	–	64K	64K	64K × 16	2	1	1	144 TQFP	825	0/70

† See Figure 2–2 for explanation of device nomenclature.

‡ One TDM serial port; one standard serial port

§ Plastic package

¶ One standard serial port

# Two standard serial ports

|| One buffered serial port; one standard serial port

Table 2–8. TMS320C54x Commercial Devices

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)					Peripherals				Typ Diss (mW)	Temp Range (°C)
				On-Chip		Off-Chip			Serial Port	HPI	Timers	Package Type		
				RAM	ROM	Data	Prog	I/O						
'C541#–40	80	25	40	5K	28K	64K	64K	64K × 16	2	–	1	100 TQFP‡	600	–40/85
'C542#–40	80	25	40	10K	2K	64K	64K	64K × 16	2	1	1	128/144 TQFP‡	600	–40/85
'LC541#–40	80	25	40	5K	28K	64K	64K	64K × 16	2	–	1	100 TQFP‡	200	–40/85
'LC541#–50	100	25	40	5K	28K	64K	64K	64K × 16	2	–	1	100 TQFP‡	225	–40/85
'LC542#–40	80	25	40	10K	2K	64K	64K	64K × 16	2§	1	1	128/144 TQFP‡	200	–40/85
'LC542#–50	100	20	50	10K	2K	64K	64K	64K × 16	2§	1	1	128/144 TQFP‡	225	–40/85
'LC543#–40	80	25	40	10K	2K	64K	64K	64K × 16	2§	–	1	100 TQFP‡	200	–40/85
'LC543#–50	100	20	50	10K	2K	64K	64K	64K × 16	2§	–	1	100 TQFP‡	225	–40/85
'LC545#–40	80	25	40	6K	48K	64K	64K	64K × 16	2¶	1	1	128 TQFP‡	200	–40/85
'LC545#–50	100	20	50	6K	48K	64K	64K	64K × 16	2¶	1	1	128 TQFP‡	225	–40/85
'LC546#–40	80	25	40	6K	48K	64K	64K	64K × 16	2¶	–	1	100 TQFP‡	200	–40/85
'LC546#–50	100	20	50	6K	48K	64K	64K	64K × 16	2¶	–	1	100 TQFP‡	225	–40/85
'LC548#–50	100	20	50	32K	2K	64K	4M	64K × 16	3#	1	1	144 TQFP‡	225	–40/85
'LC548#–66	133	15	66	32K	2K	64K	4M	64K × 16	3#	1	1	144 TQFP‡	255	–40/85

† See Figure 2–2 for explanation of device nomenclature.

‡ Plastic package

§ One buffered serial port; one TDM serial port

¶ One buffered serial port; one standard serial port

# Two BSPs; one TDM serial port

Table 2–8. TMS320C54x Commercial Devices (Continued)

Device Name†	Freq (MHz)	Cycle Time (ns)	MIPS	Memory (Words)					Peripherals				Typ Diss (mW)	Temp Range (°C)
				On-Chip		Off-Chip			Serial Port	HPI	Timers	Package Type		
				RAM	ROM	Data	Prog	I/O						
'VC541#–40	80	25	40	5K	28K	64K	64K	64K × 16	2	–	1	100 TQFP‡	170	–40/85
'VC541#–50	100	20	50	5K	28K	64K	64K	64K × 16	2	–	1	100 TQFP‡	200	–40/85
'VC542#–40	80	25	40	10K	2K	64K	64K	64K × 16	2§	1	1	128/144 TQFP‡	170	–40/85
'VC542#–50	100	20	50	10K	2K	64K	64K	64K × 16	2§	1	1	128/144 TQFP‡	200	–40/85
'VC543#–40	80	25	40	10K	2K	64K	64K	64K × 16	2§	–	1	100 TQFP‡	170	–40/85
'VC543#–50	100	20	50	10K	2K	64K	64K	64K × 16	2§	–	1	100 TQFP‡	200	–40/85
'VC545#–40	80	25	40	6K	48K	64K	64K	64K × 16	2¶	1	1	128 TQFP‡	170	–40/85
'VC545#–50	100	20	50	6K	48K	64K	64K	64K × 16	2¶	1	1	128 TQFP‡	200	–40/85
'VC546#–40	80	25	40	6K	48K	64K	64K	64K × 16	2¶	–	1	100 TQFP‡	170	–40/85
'VC546#–50	100	20	50	6K	48K	64K	64K	64K × 16	2¶	–	1	100 TQFP‡	200	–40/85
'VC548#–50	100	20	50	32K	2K	64K	64K	64K × 16	3#	1	1	144 TQFP‡	200	–40/85

† See Figure 2–2 for explanation of device nomenclature.

‡ Plastic package

§ One buffered serial port; one TDM serial port

¶ One buffered serial port; one standard serial port

# Two BSPs; one TDM serial port

Table 2–9. TMS320C8x Commercial Devices

Device Name	Freq (MHz)	Cycle Time (Ns)	BOPS	Memory (Words)				Additional Processors					Typ Diss (W)	Temp Range (°C)
				On-Chip			Off-Chip	Video Cont	Transfer Cont	Parallel Proc	Package Type			
				SRAM	ROM	Cache	Parallel							
'C80GF-40	40	25	2	50K			4G x 8	2	1	4	305 PGA	7	0-85	
'C80GF-50	50	20	2	50K			4G x 8	2	1	4	305 PGA	6.5	0-85	
'C80GF-60	60	16	2.5	50K			4G x 8	2	1	4	305 BGA	5	0-85	
'C82GGP	50	20	1.5	44K			4G x 8	–	1	2	352 BGA	3	0-85	

Table 2–10. TMS320AVxxx Commercial Devices

Device Name†	Function	Input Format	Output Format	Controller Interface	Off-Chip Memory	Package Type
'AV110	MPEG Audio Decoder	MPEG Audio Stream or MPEG System Stream	16- or 18-bit serial PCM	8-bit	Optional 1M DRAM	120-pin PQFP
'AV120	MPEG Audio Decoder	MPEG Audio Stream Serial PCM	16- or 18-bit	None	None	44-pin PLCC
'AV220	Video CD MPEG Decoder	MPEG System Stream	704 x 240 at 60 Hz 704 x 288 at 50 Hz	8-bit	4M DRAM	160-pin PQFP
'AV411	Digital NTSC Encoder	RGB, YCbCr	RGB, Y/C (S-Video) or composite video	9-bit		100-pin PQFP
'AV420	Digital NTSC/PAL Encoder	RGS, YUV 4:4:4, or YUV 4:2:2	S-Video (Y&C)	None	None	80-pin PQFP

† See Figure 2–2 for explanation of device nomenclature.



Table 2–11. TMS320 DSP Military Part Numbers

Device Name	Operating Frequency	Package Type	Typical <sup>†</sup> Dissipation	Temp Range, °C
SMJ320C10JDM	20.5 MHz	Ceramic 40-pin DIP	165 mW	–55/125
SMJ320C10JDM25	25.6 MHz	Ceramic 40-pin DIP	200 mW	–55/125
SMJ320C15JDM	20.5 MHz	Ceramic 40-pin DIP	165 mW	–55/125
SMJ320C15JDM25	25.6 MHz	Ceramic 40-pin DIP	200 mW	–55/125
SMJ320C15FJM	20.5 MHz	44-pin JLCC	165 mW	–55/125
SMJ320C15FJM25	25.6 MHz	44-pin JLCC	200 mW	–55/125
SMJ320E14GBM	20.5 MHz	68-pin PGA	325 mW	–55/125
SMJ320E14FJM	20.5 MHz	68-pin JLCC	325 mW	–55/125
SMJ320C25GBM	40 MHz	68-pin PGA	550 mW	–55/125
SMJ320C25GBM50	50 MHz	68-pin PGA	700 mW	–55/125
SMJ320C25FJM	40 MHz	68-pin JLCC	550 mW	–55/125
SMJ320C25FJM50	50 MHz	68-pin JLCC	700 mW	–55/125
SMJ320C25FDM	40 MHz	68-pin LCCC	550 mW	–55/125
SMJ320C26BGBM	40 MHz	68-pin PGA	550 mW	–55/125
SMJ320C26BFDM	40 MHz	68-pin JLCC	550 mW	–55/125
SMJ320C30GBM33	33.3 MHz	181-pin PGA	1100 mW	–55/125
SMJ320C30HFGM33	33.3 MHz	196-pin CQFP	1100 mW	–55/125
SMJ320C30GBM40	40 MHz	181-pin PGA	1250 mW	–55/125
SMJ320C30HFGM40	40 MHz	196-pin CQFP	1250 mW	–55/125
SMJ320C30TAM33	33.3 MHz	203 OLB TAB	1100 mW	–55/125
SMJ320C30TBM33	33.3 MHz	203 OLB TAB	1100 mW	–55/125
SMJ320C30TAM40	40 MHz	203 OLB TAB	1250 mW	–55/125
SMJ320C30TBM40	40 MHz	203 OLB TAB	1250 mW	–55/125
TMP320C30TAL40	40 MHz	203 OLB TAB	1250 mW	0/70
SMJ320C30KGDM33	33.3 MHz	203-pad KGD	1100 mW	–55/125
SMJ320C30KGDM40	40 MHz	203-pad KGD	1250 mW	–55/125

<sup>†</sup> Calculated from typical I<sub>CC</sub> current and nominal V<sub>CC</sub> supply voltage

Table 2–11. TMS320 DSP Military Part Numbers (Continued)

Device Name	Operating Frequency	Package Type	Typical† Dissipation	Temp Range, °C
TMP320C30KGD40	40 MHz	203-pad KGD	1250 mW	0/70
SMJ320C31GFAM33	33.3 MHz	141-pin PGA	750 mW	–55/125
SMJ320C31HFGM33	33.3 MHz	132-pin CQFP	750 mW	–55/125
SMJ320C31GFAM40	40 MHz	141-pin PGA	1250 mW	–55/125
SMJ320C31HFGM40	40 MHz	132-pin CQFP	1250 mW	–55/125
SMJ320C31GFAM50	50 MHz	141-pin PGA	1750 mW	–55/125
SMJ320C31HFGM50	50 MHz	132-pin CQFP	1750 mW	–55/125
SMJ320C31TAM33	33.3 MHz	132 OLB TAB	750 mW	–55/125
SMJ320C31TBM33	33.3 MHz	132 OLB TAB	750 mW	–55/125
SMJ320C31TAM40	40 MHz	132 OLB TAB	1250 mW	–55/125
SMJ320C31TBM40	40 MHz	132 OLB TAB	1250 mW	–55/125
SMJ320C31TAM50	50 MHz	132 OLB TAB	1750 mW	–55/125
SMJ320C31TBM50	50 MHz	132 OLB TAB	1750 mW	–55/125
TMP320C31TAL50	50 MHz	132 OLB TAB	1750 mW	0/70
SMJ320C31KGDM33	33.3 MHz	132-pad KGD	750 mW	–55/125
SMJ320C31KGDM40	40 MHz	132-pad KGD	1250 mW	–55/125
SMJ320C31KGDM50	50 MHz	132-pad KGD	1750 mW	–55/125
TMP320C31KGD40	40 MHz	132-pad KGD	1250 mW	0/70
TMP320C31KGD50	50 MHz	132-pad KGD	1750 mW	0/70
SMQ320C32PCMM50	50 MHz	144-pin PQFP	1000 mW	–55/125
SMJ320C40GFM33	33.3 MHz	325-pin PGA	1000 mW	–55/125
SMJ320C40HFHM33	33.3 MHz	352-pin CQFP	1000 mW	–55/125
SMJ320C40GFM40	40 MHz	325-pin PGA	1750 mW	–55/125
SMJ320C40HFHM40	40 MHz	352-pin CQFP	1750 mW	–55/125
SMJ320C40GFM50	50 MHz	325-pin PGA	2500 mW	–55/125
SMJ320C40HFHM50	50 MHz	352-pin CQFP	2500 mW	–55/125
SMJ320C40TABM40	40 MHz	325 OLB TAB	1750 mW	–55/125

† Calculated from typical  $I_{CC}$  current and nominal  $V_{CC}$  supply voltage

Table 2–11. TMS320 DSP Military Part Numbers (Continued)

Device Name	Operating Frequency	Package Type	Typical† Dissipation	Temp Range, °C
SMJ320C40TBBM40	40 MHz	325 OLB TAB	1750 mW	–55/125
SMJ320C40TABM50	50 MHz	325 OLB TAB	2500 mW	–55/125
SMJ320C40TBBM50	50 MHz	325 OLB TAB	2500 mW	–55/125
TMP320C40TABL50	50 MHz	325 OLB TAB	2500 mW	0/70
TMP320C40TABL60	60 MHz	325 OLB TAB	3250 mW	0/70
SMJ320C40KGDM40	40 MHz	325-pad KGD	1750 mW	–55/125
SMJ320C40KGDM50	50 MHz	325-pad KGD	2500 mW	–55/125
TMP320C40KGDL50	50 MHz	325-pad KGD	2500 mW	0/70
TMP320C40KGDL60	60 MHz	325-pad KGD	3250 mW	0/70
TMP320C50KGDL40	40 MHz	117-pad KGD	525 mW	0/70
TMP320C50KGDL57	57 MHz	117-pad KGD	590 mW	0/70
SMJ320C50KGDM50	50 MHz	117-pad KGD	450 mW	–55/125
SMJ320C50KGDM66	66 MHz	117-pad KGD	600 mW	–55/125
SMJ320C50GFAM50	50 MHz	141-pin PGA	450 mW	–55/125
SMJ320C50GFAM66	66 MHz	141-pin PGA	600 mW	–55/125
SMJ320C50HFGM50	50 MHz	132-pin CQFP	450 mW	–55/125
SMJ320C50HFGM66	66 MHz	132-pin CQFP	600 mW	–55/125
SMQ320C50PQM66	66 MHz	132-pin PQFP	600 mW	–55/125
TMP320BC51KGDL40	40 MHz	117-pad KGD	525 mW	0/70
TMP320BC51KGDL57	57 MHz	117-pad KGD	590 mW	0/70
SMJ320C80GFM40	40 MHz	305-pin CPGA	3 W	–55/125
SMJ320C80GFM50	50 MHz	320-pin CPGA	TBD	–55/125
SMJ320C80HFHM40	40 MHz	305-pin CQFP	3 W	–55/125
SMJ320C80HFHM50	50 MHz	320-pin CQFP	TBD	–55/125

† Calculated from typical  $I_{CC}$  current and nominal  $V_{CC}$  supply voltage

## 2.4 TMS320 Development and Support Tools Overview

Fast time to market, increased productivity, and ease of design-in are of primary importance when developing a DSP-based system. To meet these needs, TI offers a complete suite of code-generation and debug tools as well as a broad and innovative range of third-party tools (See Chapter 18). TMS320 DSP tool support eases the design process from initial concept through integration and production, enabling customers to take full advantage of rapidly evolving DSP technologies. Table 2–12 shows an overview of the TMS320 development and support tools. Table 2–13 summarizes the features of the simulation and emulation development tools.

Table 2–12. TMS320 Development and Support Tools Overview

'C1x	'C2x	'C2xx	'C3x	'C4x	'C5x	'C54x	'C8x
EVM†	EVM DSK		EVM DSK	Parallel Processing Development System (PPDS)	EVM DSK	EVM DSKplus	Software Development Board (SDB)
Simulator Software With Debugger	Simulator Software With Debugger	Simulator Software With Debugger	Simulator Software With Debugger	Simulator Software With Debugger	Simulator Software With Debugger	Simulator Software With Debugger	Simulator Software With Debugger
C Compiler/ Assembler/ Linker	C Compiler/ Assembler/ Linker	C Compiler/ Assembler/ Linker	C Compiler/ Assembler/ Linker	C Compiler/ Assembler/ Linker	C Compiler/ Assembler/ Linker	C Compiler/ Assembler/ Linker	C Compiler/ Assembler/ Linker
XDS/22	XDS/22	XDS510/ XDS510WS Hardware	XDS510/ XDS510WS Hardware	XDS510/ XDS510WS Hardware	XDS510/ XDS510WS Hardware	XDS510/ XDS510WS Hardware	XDS510/ XDS510WS Hardware
		Conversion Cable	Conversion Cable	Conversion Cable	Conversion Cable	Conversion Cable	Conversion Cable
		Emulator Porting Kit	Emulator Porting Kit	Emulator Porting Kit	Emulator Porting Kit	Emulator Porting Kit	Emulator Porting Kit
		Code Composer	Code Composer	Code Composer	Code Composer	Code Composer	

† Evaluation module

‡ DSP starter kit

Table 2–13. Features of TMS320 Simulation/Emulation Development Tools

Features	EVM, SDB or PPDS†	Simulator	XDS/22	XDS510
<b>TMS320 device supported:</b>	'C16	'C1x	'C1x	'C2xx
	'C26	'C2x	'C2x	'C3x
	'C30	'C2xx		'C4x
	'C50	'C3x		'C5x
	'C54x	'C4x		'C54x
	'C8x	'C5x		'C8x
		'C54x		
		'C8x		
<b>Development purpose:</b>				
Evaluation/benchmarking	Yes	Yes	Yes	Yes
Software design	Yes	Yes	Yes	Yes
Hardware design	No	No	Yes	Yes
Line-by-line or reverse assembler	Yes	Yes	Yes	Yes
Modify/display memory and registers	Yes	Yes	Yes	Yes
Single-stepping	Yes	Yes	Yes	Yes
Breakpoint on instruction acquisition	Yes	Yes	Yes	Yes
Breakpoint on memory access/read/write	No	Yes	Yes	Yes
Time-stamping/clock counter	No	Yes	Yes	No
Real-time trace samples	No	No	Yes	No
Multiuser system	No	Yes	No	Yes
HLL user interface	Yes	Yes	Yes	Yes
Files associated with I/O ports	No	Yes‡	No	No
<b>Full-speed in-circuit emulation:</b>				
From on-board memory	Yes	N/A	Yes	No
From target memory	No	N/A	Yes	Yes
<b>Amount of external memory (words):</b>				
On-board program/data ('C1x)	64K	N/A	4K/256	N/A
On-board program/data ('C2x)	64K	N/A	4K/512	N/A
On-board program/data ('C3x)	16K	N/A	N/A	N/A
On-board program/data ('C4x)	384K	N/A	N/A	N/A
On-board program/data ('C5x)	64K	N/A	N/A	N/A
On-board program/data ('C54x)	64K	N/A	N/A	N/A
Program/data expansion	N/A	N/A	64K§	N/A¶

† EVM = evaluation module, SDB = software development board, PPDS = parallel processing development system

‡ This purpose is not supported by the 'C1x simulator.

§ The memory expansion board (included in the 'C2x XDS/22) allows for memory expansion to 64K total words of program and data memory, configurable in 1K-word blocks.

¶ Program/data expansion depends on the user's target system.

### 2.4.1 TMS320 Tool Numbering System

To classify the stages in the support tool development cycle, Texas Instruments assigns prefix designators in the part number nomenclature. There are three development support tool prefix designators — TMDX, TMDS, and TMDC — that represent the evolutionary stages of tool development from engineering prototypes (TMDX) through fully qualified production units (TMDS). The development flow is defined as follows:

#### Support Tool Development Evolutionary Flow

TMDX	Developmental product that has not yet completed TI internal qualification testing
TMDS	Fully qualified development support product
TMDC	Development support product that is unsupported or obsolete

TMX and TMP devices and TMDX development support tools are shipped with the following disclaimer:

**Developmental product intended for internal evaluation purposes.**

#### Note:

Texas Instruments recommends that prototype devices (TMX or TMP) not be used in production systems, because their expected end-use failure rate is undefined but is predicted to be greater than the failure rate of standard, qualified production devices.

TMDS development support tools have been properly tested, and the quality and reliability of the devices have been successfully demonstrated. TI's standard warranty applies.

### 2.4.2 Development and Support Tools

The standard flow for development begins with code written in a high-level language (such as C) or assembly language. This code can be debugged on one of several debug platforms (simulator, software development board, emulator, etc.), all of which feature the same debugger hardware. Software and hardware can be developed in parallel by using the TMS320 compiler, assembler/linker, simulator, evaluation module (EVM), or software development board (SDB) for software development, and by using the TMS320 emulators for hardware development. Table 2–14 and Table 2–15 give part numbers and host/operating system requirements for, respectively, code development and debug support functions.

Table 2–14. TMS320 Code Development Support Tools

Device	Product Description	Part Number	Host	Operating System <sup>†</sup>
'C1x	Assembler/Linker	TMDS3242850–02	PC	OS/2 DOS Ext
'C2x	Assembler/Linker	TMDS324850–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMDS3242855–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMD3242555–08	SPARC HP9000	N/A
'C2xx	Assembler/Linker	TMDS3242850–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMDS3242855–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMDS3242555–08	SPARC HP9000	N/A
'C3x	Assembler/Linker	TMDS3243850–02	PC	OS/2 DOS Ext Win32
	C Compiler Assembler/Linker	TMDS3243855–02	PC	OS/2 DOS Ext Win32
	C Compiler Assembler/Linker	TMDS3243555–08	SPARC HP9000	N/A

<sup>†</sup> PC = MS-DOS 5.x or higher, OS/2.2x or higher  
 DOS Ext = DOS/4GW DOS Extender  
 Win16 = Windows 3.xx  
 Win32 = Windows NT and Windows 95  
 SPARC = SunOS 4.1.3 or higher or Solaris 2.x  
 OpenWin = Open Windows 3.x  
 HP9000 series 700 = HP-UX 9.x or higher  
 N/A = Not applicable

Table 2–14. TMS320 Code Development Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C4x	Assembler/Linker	TMDS3243850–02	PC	OS/2 DOS Ext Win32
	C Compiler Assembler/Linker	TMDS3243855–02	PC	OS/2 DOS Ext Win32
	C Compiler Assembler/Linker	TMDS3243555–08	SPARC HP9000	N/A
'C5x	Assembler/Linker	TMDS3242850–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMDS3242855–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMDS3245555–08	SPARC HP9000	N/A
'C54x	Assembler/Linker	TMDS324L850–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMDS324L855–02	PC	OS/2 DOS Ext
	C Compiler Assembler/Linker	TMDS324L555–09	SPARC	N/A

† PC = MS-DOS 5.x or higher, OS/2.2x or higher  
 DOS Ext = DOS/4GW DOS Extender  
 Win16 = Windows 3.xx  
 Win32 = Windows NT and Windows 95  
 SPARC = SunOS 4.1.3 or higher or Solaris 2.x  
 OpenWin = Open Windows 3.x  
 HP9000 series 700 = HP-UX 9.x or higher  
 N/A = Not applicable



Table 2–14. TMS320 Code Development Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C8x	Code Generation Software Toolkit (includes Compiler, Assembler, Linker, and Simulator Debugger)	TMDS3248555–67	SPARC	N/A
	Code Generation Software Toolkit (includes Compiler, Assembler, and Linker)	TMDS3248855–07	PC	Windows NT

† PC = MS-DOS 5.x or higher, OS/2.2x or higher

DOS Ext = DOS/4GW DOS Extender

Win16 = Windows 3.xx

Win32 = Windows NT and Windows 95

SPARC = SunOS 4.1.3 or higher or Solaris 2.x

OpenWin = Open Windows 3.x

HP9000 series 700 = HP-UX 9.x or higher

N/A = Not applicable

Table 2–15. TMS320 Code Debug Support Tools

Device	Product Description	Part Number	Host	Operating System <sup>†</sup>
'C1x	Simulator	TMDS3240811–02	PC	DOS
	'C14 XDS/22	TMDX3262214	N/A	N/A
	'C10/C15 XDS/22	TMDS3262215	N/A	N/A
	'C17 XDS/22	TMDS3262217	N/A	N/A
	Analog I/F Board	RTC/AIB320A–06	XDS/22	N/A
	'C16 EVM Debugger	TMDS3260016	PC (ISA)	Win16
'C2x	Simulator	TMDS3242851–02	PC	DOS Win16
	Simulator	TMDS3242551–09	SPARC	SunView
	'C25/C26 XDS/22	TMDS3262221	N/A	N/A
	Analog I/F Board	RTC/AIB320A–06	N/A	N/A
	'C26 EVM Board Debugger	TMDS3260026	PC (ISA)	Win16 DOS
	'C26 DSK Assembler/Debugger	TMDS3200026	PC (UART)	DOS

<sup>†</sup> PC = MS-DOS 5.x or higher, OS/2.2x or higher

DOS Ext = DOS/4GW DOS Extender

Win16 = Windows 3.xx

Win32 = Windows NT and Windows 95

SPARC = SunOS 4.1.3 or higher or Solaris 2.x

OpenWin = Open Windows 3.x

HP9000 series 700 = HP-UX 9.x or higher

N/A = Not applicable

<sup>‡</sup> License must be signed in order to purchase the Emulator Porting Kit (EPK).

Table 2–15. TMS320 Code Debug Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C2xx	Simulator	TMDX324X851–02	PC	DOS Win16
	Simulator	TMDX324X551–09	SPARC	OpenWin
	XDS510 Debugger	TMDX324012XX	PC	DOS Win16 OS/2
	XDS510WS Debugger	TMDX324062XX	SPARC	OpenWin
	XDS510 Board JTAG Emulator Cable	TMDS00510	PC (ISA)	N/A
	XDS510WS Box JTAG Emulator Cable	TMDS00510WS	SPARC	OpenWin
	JTAG Emulator Cable	TMDS3080002	N/A	N/A
	Emulator Porting Kit‡	TMDX324002XX	PC	DOS Win16 OS/2

† PC = MS-DOS 5.x or higher, OS/2.2x or higher

DOS Ext = DOS/4GW DOS Extender

Win16 = Windows 3.xx

Win32 = Windows NT and Windows 95

SPARC = SunOS 4.1.3 or higher or Solaris 2.x

OpenWin = Open Windows 3.x

HP9000 series 700 = HP-UX 9.x or higher

N/A = Not applicable

‡ License must be signed in order to purchase the Emulator Porting Kit (EPK).

Table 2–15. TMS320 Code Debug Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C3x	Simulator	TMDS3243851–02	PC	DOS Win16
	Simulator	TMDS3243551–09	SPARC	OpenWin
	XDS510 Debugger	TMDS3240130	PC	DOS Win16
	XDS510WS Debugger	TMDS3240630	SPARC	OpenWin
	XDS510 Board MPSD Cable	TMDS00510M	PC (ISA)	N/A
	XDS510WS Controller MPSD Cable Power Supply SCSI Cable	TMDS00510WSM	SPARC	N/A
	MPSD Cable	TMDS3080004	PC SPARC	N/A
	Emulator Porting Kit‡	TMDS3240030	PC	DOS Win16
	'C30 EVM Board Debugger Assembler/Linker	TMDS3260030	PC(ISA)	DOS Win16
	'C31 DSK Assembler/Debugger	TMDS3200031	PC(DB25)	DOS

† PC = MS-DOS 5.x or higher, OS/2.2x or higher

DOS Ext = DOS/4GW DOS Extender

Win16 = Windows 3.xx

Win32 = Windows NT and Windows 95

SPARC = SunOS 4.1.3 or higher or Solaris 2.x

OpenWin = Open Windows 3.x

HP9000 series 700 = HP-UX 9.x or higher

N/A = Not applicable

‡ License must be signed in order to purchase the Emulator Porting Kit (EPK).

Table 2–15. TMS320 Code Debug Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C4x	Simulator	TMDS3244851–02	PC	DOS Win16
	Simulator	TMDS3244551–09	SPARC	OpenWin
	XDS510 Debugger	TMDS3240140	PC	OS/2 DOS Win16
	XDS510WS Debugger	TMDS3240640	SPARC	OpenWin
	XDS510 Board JTAG Cable	TMDS00510	PC (ISA)	N/A
	XDS510WS Controller JTAG Cable Power Supply SCSI Cable	TMDS00510WS	SPARC	N/A
	JTAG Cable	TMDS3080002	PC SPARC	N/A
	Emulator Porting Kit‡	TMDX3240040	PC	OS/2 DOS Win16
	C40 PPDS Board	TMDX3261040	PC XDS510 SPARC XDS510WS	N/A

† PC = MS-DOS 5.x or higher, OS/2.2x or higher

DOS Ext = DOS/4GW DOS Extender

Win16 = Windows 3.xx

Win32 = Windows NT and Windows 95

SPARC = SunOS 4.1.3 or higher or Solaris 2.x

OpenWin = Open Windows 3.x

HP9000 series 700 = HP-UX 9.x or higher

N/A = Not applicable

‡ License must be signed in order to purchase the Emulator Porting Kit (EPK).

Table 2–15. TMS320 Code Debug Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C5x	Simulator	TMDS3245851–02	PC	DOS Win16
	Simulator	TMDS3243551–09	SPARC	OpenWin
	XDS510 Debugger	TMDS3240150	PC	DOS Win16 OS/2
	XDS510WS Debugger	TMDS3240650	SPARC	OpenWin
	XDS510 Board JTAG Emulator Cable	TMDS00510	PC (ISA)	N/A
	XDS510WS Box JTAG Emulator Cable	TMDS00510WS	SPARC	OpenWin
	JTAG Emulator Cable	TMDS3080002	N/A	N/A
	Emulator Porting Kit‡	TMDX3240050	PC	DOS Win16 OS/2
	'C50 EVM Board Debugger	TMDS3260050	PC (ISA)	DOS Win16
	'C50 DSK Assembler/Debugger	TMDS3200051	PC (UART)	DOS

† PC = MS-DOS 5.x or higher, OS/2.2x or higher  
 DOS Ext = DOS/4GW DOS Extender  
 Win16 = Windows 3.xx  
 Win32 = Windows NT and Windows 95  
 SPARC = SunOS 4.1.3 or higher or Solaris 2.x  
 OpenWin = Open Windows 3.x  
 HP9000 series 700 = HP-UX 9.x or higher  
 N/A = Not applicable

‡ License must be signed in order to purchase the Emulator Porting Kit (EPK).

Table 2–15. TMS320 Code Debug Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C54x	Simulator	TMDS324L851–02	PC	DOS Win16
	Simulator	TMDS324L551–09	SPARC	OpenWin
	XDS510 Debugger	TMDS32401L0	PC	DOS Win16 OS/2
	XDS510WS Debugger	TMDS32406L0	SPARC	OpenWin
	XDS510 Board JTAG Emulator Cable	TMDS00510	PC (ISA)	N/A
	XDS510WS Box JTAG Emulator Cable	TMDS00510WS	SPARC	OpenWin
	JTAG Emulator Cable	TMDS3080002	N/A	N/A
	Emulator Porting Kit‡	TMDX32400L0	PC	DOS Win16 OS/2
	EVM Board Debugger	TMDS3260051	PC (ISA)	DOS Win16
	'C54x DSKplus Assembler/Debugger	TMDS32000L0	PC (UART)	DOS

† PC = MS-DOS 5.x or higher, OS/2.2x or higher

DOS Ext = DOS/4GW DOS Extender

Win16 = Windows 3.xx

Win32 = Windows NT and Windows 95

SPARC = SunOS 4.1.3 or higher or Solaris 2.x

OpenWin = Open Windows 3.x

HP9000 series 700 = HP-UX 9.x or higher

N/A = Not applicable

‡ License must be signed in order to purchase the Emulator Porting Kit (EPK).

Table 2–15. TMS320 Code Debug Support Tools (Continued)

Device	Product Description	Part Number	Host	Operating System†
'C8x	Debugger Software for Emulator	TMDS3240680	SPARC	N/A
	Debugger Software for Emulator	TMDS3240180	PC	Windows NT
	Emulator Card (includes XDS510 Board and JTAG Emulator Cable)	TMDS00510	PC (ISA)	N/A
	Emulator Box (includes XDS510WS Box and JTAG Emulator Cable)	TMDS00510WS	SPARC	N/A
	JTAG Emulator Cable	TMDS3080002	—	—
	Emulator Porting Kit‡	TMDX3240080	PC SPARC	—
	Software Development Board (SDB) and Debugger (includes PCI card)	TMDX3260080	Pentium PC (PCI)	Windows NT

† PC = MS-DOS 5.x or higher, OS/2.2x or higher

DOS Ext = DOS/4GW DOS Extender

Win16 = Windows 3.xx

Win32 = Windows NT and Windows 95

SPARC = SunOS 4.1.3 or higher or Solaris 2.x

OpenWin = Open Windows 3.x

HP9000 series 700 = HP-UX 9.x or higher

N/A = Not applicable

‡ License must be signed in order to purchase the Emulator Porting Kit (EPK).



# TMS320C1x Devices

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The TMS320C1x generation of digital signal processors was the first series of DSPs developed by Texas Instruments. Its first member, the TMS320C10, was introduced in 1982. Today, the 'C1x generation consists of five members and is TI's lowest-cost DSP family.

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### 3.1 TMS320C1x Introduction

The 'C1x devices are based on a 16-bit fixed-point architecture. The Harvard architecture of these DSPs means that they have separate program and data buses for increased parallelism. Each of the devices in this generation has a unique mix of speed, on-chip memory, and peripherals that allow users to choose the one that best meets their needs. The 'C1x generation devices are all object-code compatible. These devices typically operate at 5 V.

Single-cycle multiply or arithmetic logic unit (ALU) operations provide real-time computation for DSP and control algorithms. The standard multiply time is 200 ns. A separate I/O select signal provides eight I/O ports using the 16-bit data bus. I/O ports provide a simple interface to analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), because these have a separate select signal with the standard data bus. The 16-bit barrel shifter scales data in parallel with ALU operations; data is shifted by up to 16 bits during the same cycle it is used in the ALU. The 0-, 1-, or 4-bit left shifter also operates in parallel with the ALU to support both integer and fractional math.

## 3.2 TMS320C1x Memory and Buses

The modified Harvard architecture of the 'C1x provides simultaneous access to both the data and program memory. This allows both a program fetch and data fetch to occur in parallel, so arithmetic operations execute in a single cycle. The bridge between program and data buses allows you to store coefficients in read-only memory (ROM) and transfer these coefficients into data RAM during system start-up.

On-chip program and data memory provide internal information to the CPU; external RAM or ROM can be interfaced to the 'C1x for those applications requiring off-chip program memory space.

The 'C1x offers a variety of on-chip memory, including one-time-programmable (OTP) and ROM devices with up to 8K 16-bit words of on-chip memory. Most devices have 4K 16-bit words of external program address available. For designers who need additional external memory, the 'C16 offers 64K 16-bit words of external address reach.

For a summary of device memory offerings, see Table 2–2.

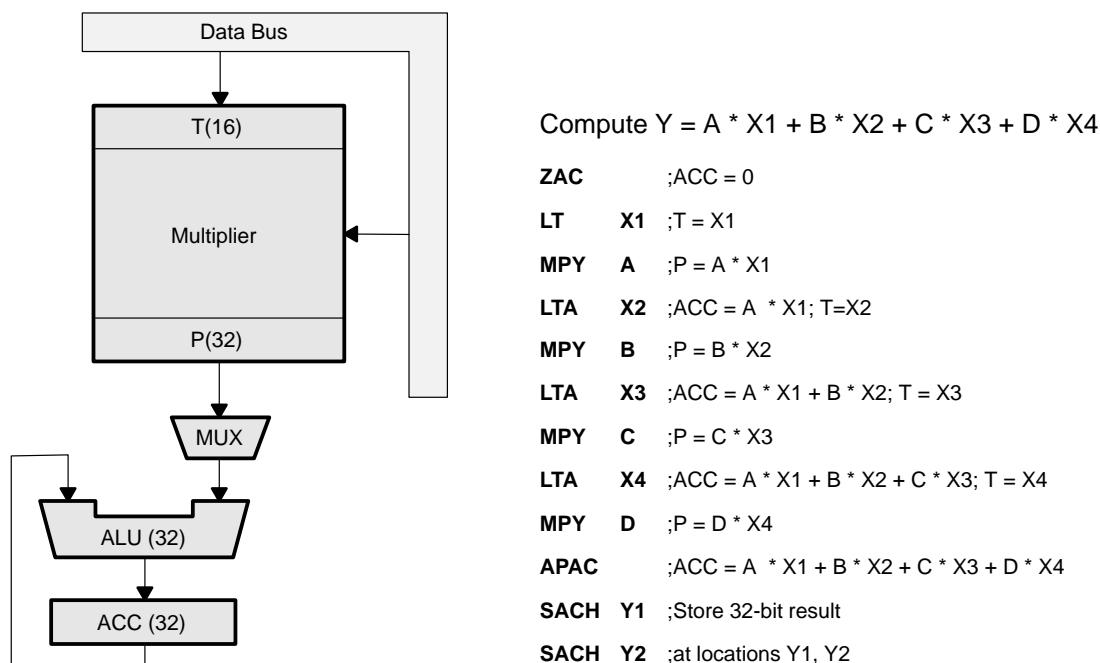
Features of the 'C1x memory and buses are:

- ☐ Single-cycle reads and writes
- ☐ Modified Harvard architecture
  - Separate program and data buses
  - "Bridge" between program and data space
- ☐ Up to 8K words of on-chip program ROM
- ☐ 4K words of one-time user-programmable memory available
- ☐ Up to 64K words of external program memory

### 3.3 Sum of Products

A sum of products is a fundamental calculation in many DSP algorithms, including FIR (finite impulse response) filters, matrix multiplication, control (transfer) functions, etc. This operation requires a fast multiply and accumulate (MAC) time. The example in Figure 3–1 shows the sum of four products, which requires the 12 program-memory locations and executes in 12 cycles. Note that the 32-bit product register and the 32-bit accumulator preserve high precision throughout the calculation.

Figure 3–1. TMS320C1x Sum of Products Example



### 3.4 TMS320C1x Key Features

Following are the key features of the 'C1x generation. When only certain devices have a particular feature, they are named in parentheses following the feature's description.

- ☐ 256-word programmable on-chip data RAM (144 words on the 'C10)
- ☐ 1.5K-word on-chip program ROM on the 'C10; 4K on the 'C14, 'C15, and 'C17; and 8K on the 'C16
- ☐ Secure 4K-word on-chip program OTP memory
- ☐ 4K-word external data reach (64K on the 'C16)
- ☐ 32-bit ALU/accumulator
- ☐ 16 x 16-bit parallel multiplier with a 32-bit product
- ☐ Single-cycle multiply
- ☐ Up to four on-chip timers for control operations
- ☐ Four-level hardware stack (eight-level in the 'C16)
- ☐ Two auxiliary registers
- ☐ Four-word input and output channels on the 'C14, 'C15, and 'C17
- ☐ 16-bit barrel shifter
- ☐ Wait states for communication with slower off-chip memories/peripherals

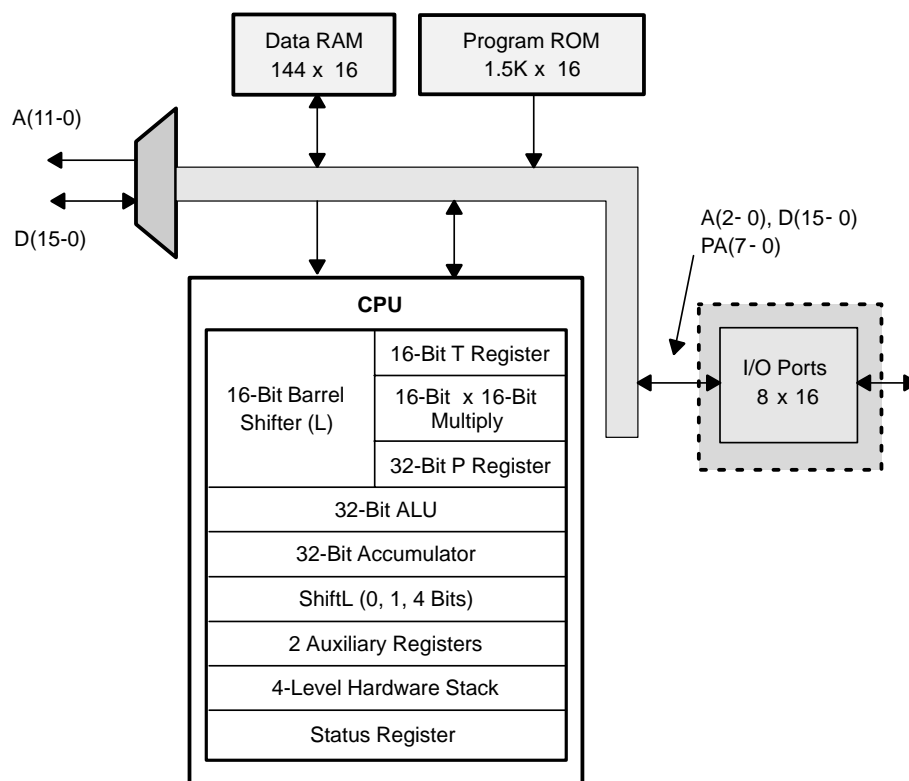
### 3.5 TMS320C10

The 'C10 (see Figure 3–2) has two speed versions that operate at instruction cycle times of 200 ns and 160 ns. This translates into 5 million instructions per second (MIPS) and 6.25 MIPS, respectively. The 'C10 has 144 words of on-chip data RAM and 1.5K words of on-chip program ROM or 4K 16-bit words of external program ROM. The 'C10 has a total program address reach of 4K words.

Additional features of the 'C10 include:

- ☐ 60 general-purpose and DSP-specific instructions
- ☐ Single-cycle multiply
- ☐ 16-bit barrel shifter
- ☐ External interrupt and polled input pins
- ☐ Eight 16-bit I/O ports
- ☐ 40-pin DIP or 44-pin PLCC package

Figure 3–2. TMS320C10 Block Diagram

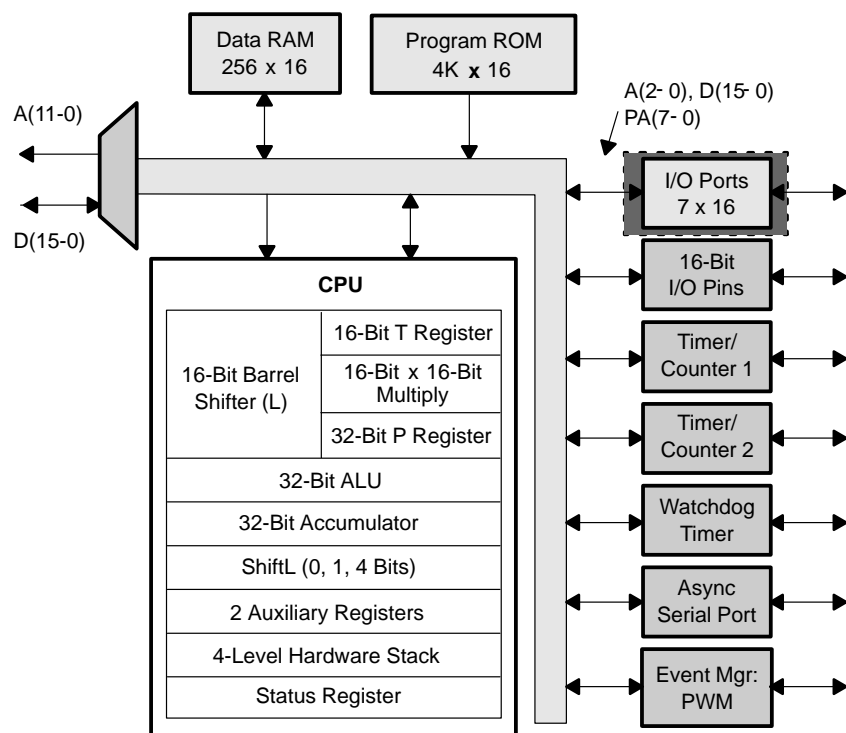


### 3.6 TMS320C14

The 'C14 (see Figure 3–3) combines the DSP core architecture with multiple control peripherals that optimize this device for single-chip control applications. These on-chip peripherals include four timer/counters; two 16-bit general-purpose timers, one serial port timer, and one watchdog timer. There are also an event manager, 16 general-purpose I/O pins, and an asynchronous serial port. The 'C14 has 256 16-bit words of on-chip RAM and 4K 16-bit words of either ROM or electrically programmable read-only memory (EPROM). It is also available in a one-time EPROM programmable version ('P14).

The 'C14 operates at an instruction cycle time of 160 ns (6.25 MIPS) and is object-code compatible with the 'C10.

Figure 3–3. TMS320C14 Block Diagram



The 'C14 peripherals (see Figure 3–4) are designed to meet the I/O requirements of control applications. They are mapped into I/O memory space and are accessed through the bank-select register (BSR) and in/out instructions. These peripherals operate without CPU intervention.

The watchdog timer is used to prevent software hang-ups. If the watchdog timer is not reset as expected, it sends an external interrupt that is commonly used to reset the processor.

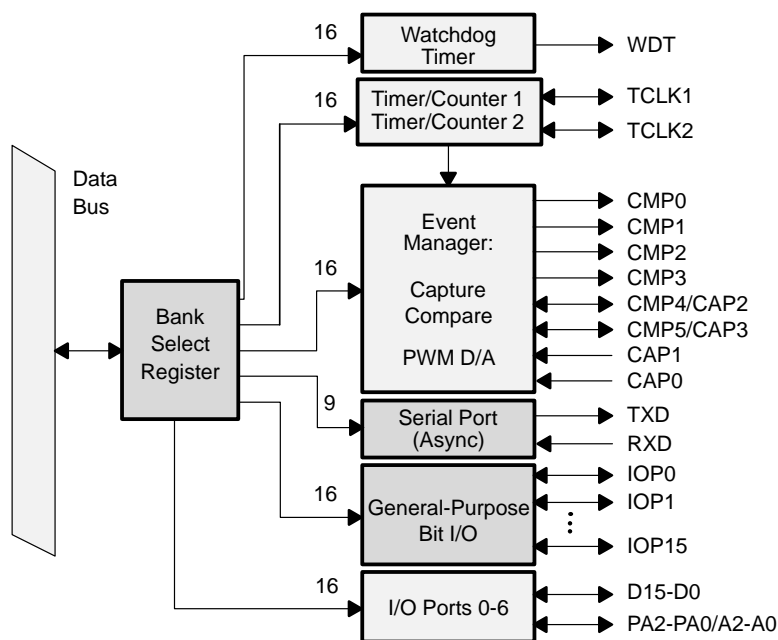
The general-purpose I/O port has 16 individual I/O pins. These I/O pins can be used to monitor and control external events within the system.

The on-chip universal asynchronous receiver/transmitter (UART) is double-buffered and operates up to 400 kbps in a full-duplex transceiver mode.

The event manager consists of compare and capture sections, which run without CPU intervention. The compare system compares each of six internal registers to either of the on-chip timers. If the contents of any compare are equal, a programmable set of actions is taken to set, reset, or toggle the associated compare output pins. Designers commonly use this system to create a pulse width modulation (PWM) output. The compare system has a special mode for PWM output, which increases the PWM resolution to 40 ns.

The capture system provides a logging function for up to four different events. When a capture pin is triggered, the content of one of the timers is saved to a 4-level-deep FIFO. An example of using the event manager is a motor spindle that triggers the 'C14's capture input on each revolution, where the 'C14 uses the captured timer data to determine the spindle speed and correct the speed by adjusting the PWM output from the compare system.

Figure 3–4. TMS320C14 Peripherals





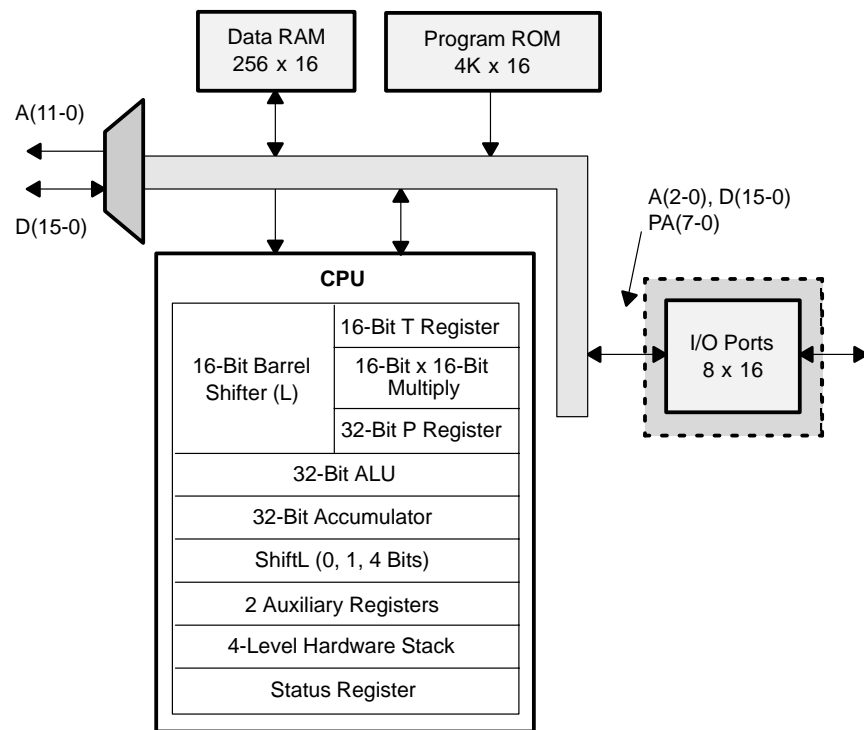
### 3.7 TMS320C15

The 'C15 (see Figure 3–5) offers 256 16-bit words of on-chip RAM and 4K 16-bit words of on-chip ROM or EPROM. It has instruction cycle times of 160 ns and 200 ns (4 MIPS). The 'C15 is both object-code and pin compatible with the 'C10.

Additional features of the 'C15 include:

- ☐ Single-cycle multiply
- ☐ 16-bit barrel shifter
- ☐ External interrupt and polled input pins
- ☐ Eight 16-bit I/O ports
- ☐ 40-pin DIP or 44-pin PLCC package
- ☐ OTP version (P15)

Figure 3–5. TMS320C15 Block Diagram



### 3.8 TMS320C16

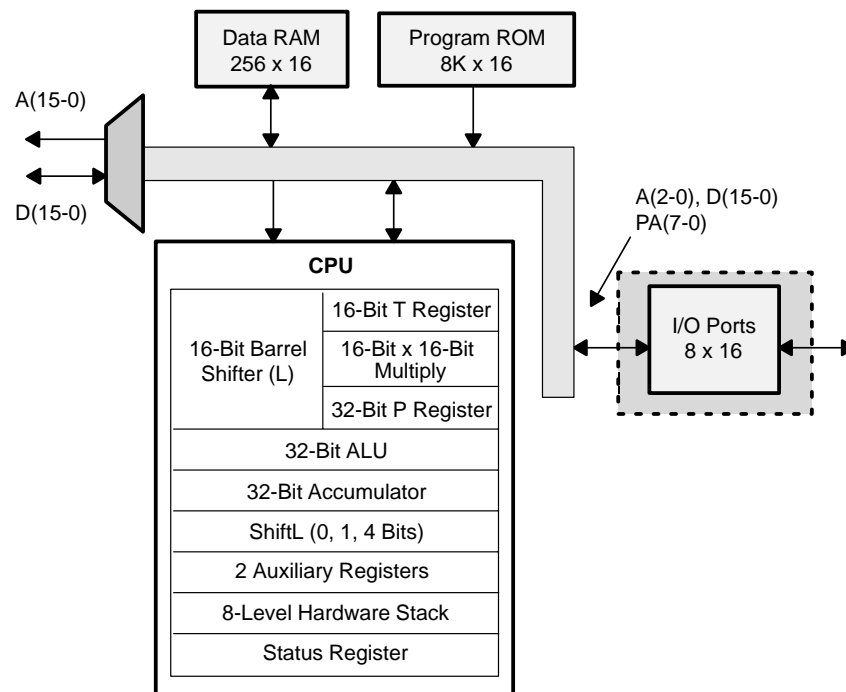
The 'C16 (see Figure 3–6) offers 256 16-bit words of on-chip RAM and 8K 16-bit words of on-chip ROM. It also has an external address reach of 64K 16-bit words (the largest of the 'C1x-generation devices) to accommodate larger programs. Another advantage is an eight-level hardware stack, up from the four levels in other members of this generation.

The 'C16 is the fastest 'C1x-generation device, performing at 8.7 MIPS (114-ns instruction cycle time). It is object-code and pin compatible with the 'C10.

Additional features of the 'C16 include:

- ☐ Single-cycle multiply
- ☐ 16-bit barrel shifter
- ☐ External interrupt and polled input pins
- ☐ Eight 16-bit I/O ports
- ☐ 64-pin PQFP package

Figure 3–6. TMS320C16 Block Diagram



### 3.9 TMS320C17

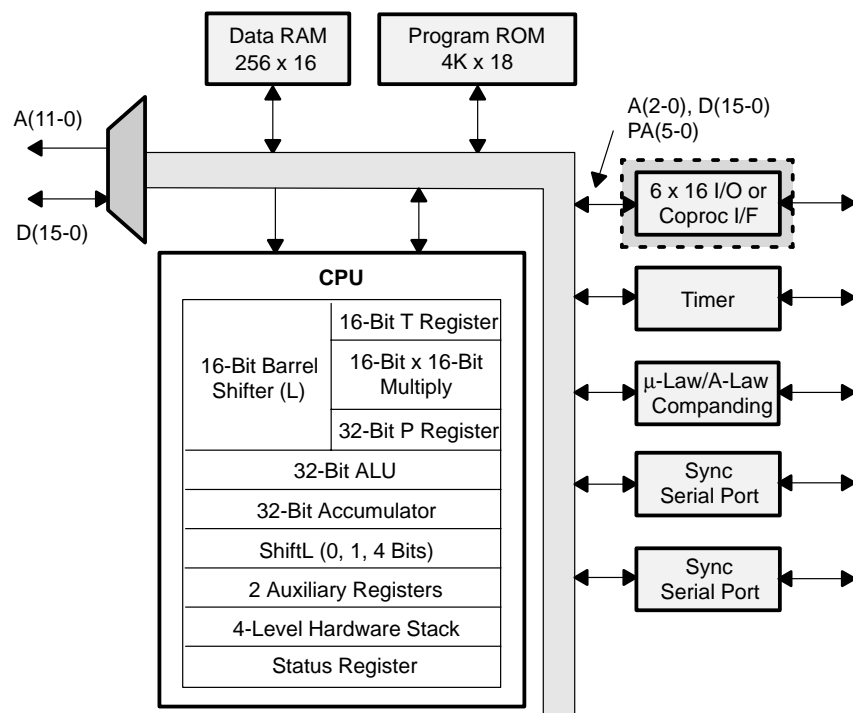
The 'C17 (see Figure 3–7) features a dual-channel serial interface, on-chip companding hardware ( $\mu$ -law/A-law), a serial-port timer, and a 16-bit latched coprocessor port for direct microprocessor I/O interface. The 'C17 has 256 16-bit words of on-chip RAM and either 4K 16-bit words of internal ROM or 4K 16-bit words of external program ROM. It is also available in an OTP version ('P17).

The 'C17 operates at instruction cycle times of 160 ns and 200 ns (3.6 MIPS).

Additional features of the 'C17 include:

- ☐ Programmable times
- ☐ Microcomputer mode only
- ☐ 40-pin DIP and 44-pin PLCC packages

Figure 3–7. TMS320C17 Block Diagram



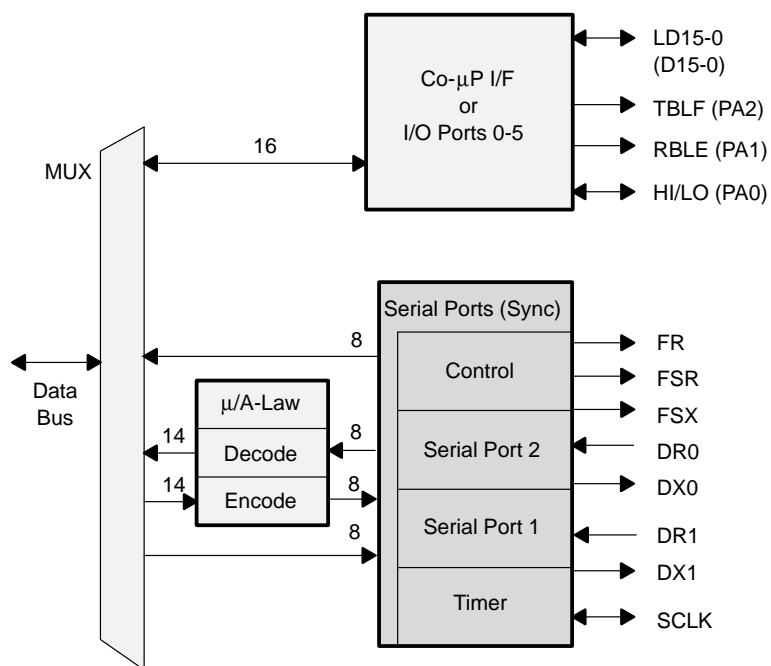
The 'C17 integrates peripherals for single-chip telecommunications applications. These peripherals are mapped into I/O memory space and are accessed through in/out instructions (see Figure 3–8).

The coprocessor interface provides a direct connection to most microcontrollers. This is an asynchronous connection that can be configured for 8- or 16-bit transfers. Optionally, the coprocessor port can be used as a 16-bit I/O port.

The on-chip companding hardware enables the 'C17 to compress and expand data in either  $\mu$ -law format with either sign magnitude or 2s-complement numbers. The companding hardware converts between 8-bit log-PCM samples and linear PCM. This saves both time and board space for systems interfacing to standard codecs such as the TCM29C18 and TCM29C19.

The 'C17 has two serial ports, each with independent transmit and receive capability. These serial ports easily interface to common codecs and operate up to 2.5 Mbps.

Figure 3–8. TMS320C17 Peripherals



### **3.10 Tools for TMS320C1x**

For information about the code generation and debugging tools available for the 'C1x devices, refer to Chapter 15, Code Generation Tools, and Chapter 16, System Integration and Debugging Tools. Table 2–14 and Table 2–15 in Chapter 2, Selection Guide, provide part numbers and host system information.

# **TMS320C2x Devices**

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The TMS320C25 and TMS320C26 devices make up the 'C2x generation. The 'C2x is an expanded version of the 'C1x architecture (16-bit fixed-point Harvard architecture).

For designers who require greater performance than that of a 'C1x DSP, the TMS320C2x offers code compatibility with several enhancements. These added features offer more flexibility in performance, more on-chip memory, and more power. There is also an ANSI C compiler designed for the 'C2x, which translates the widely used ANSI C language directly into assembly language for the 'C2x.

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<b>4.3 TMS320C2x Multiplier/ALU .....</b>	<b>4-4</b>
<b>4.4 TMS320C2x Interface to Off-Chip Devices .....</b>	<b>4-5</b>
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## 4.1 TMS320C2x Introduction

The 'C2x DSP performs 10-12.5 million instructions per second (MIPS). The 'C2x offers four times the performance of the 'C1x generation, and accepts source code from 'C1x devices.

The 'C2x is capable of an instruction cycle time of 80 ns. Enhanced features such as 74 additional instructions (134 total instructions), eight auxiliary registers, an 8-level hardware stack, more on-chip memory, and simultaneous single-cycle multiply/ALU operations contribute to this high performance. The 'C2x implements bit-reversed addressing for fast fourier transforms (FFTs) through hardware, eliminating lengthy software solutions and further increasing performance.

Another 'C2x feature is a hardware wait-state generator for communication to slower off-chip memories.

An optimizing ANSI C compiler is offered for the 'C2x. This enables you to develop and debug code in ANSI C, without learning a new assembly language. This also shortens the development cycle, reducing time to market.

## 4.2 TMS320C2x Key Features

Following are the key features of the TMS320C2x generation. When only certain devices have a particular feature, they are named in parentheses following the feature's description.

- ☐ 544-word programmable on-chip data RAM (including 256-word program/data RAM)
- ☐ 1568-word configurable program/data RAM ('C26)
- ☐ 4K-word on-chip program ROM ('C25)
- ☐ Secure 4K-word on-chip program OTP ROM
- ☐ 128K-word total data/program memory space
- ☐ 32-bit ALU/accumulator
- ☐ 16 x 16-bit parallel multiplier with a 32-bit product
- ☐ Single-cycle multiply/accumulate instructions
- ☐ Repeat instructions for efficient use of program space and enhanced execution
- ☐ Block moves for data/program management
- ☐ On-chip timer for control operations
- ☐ Up to eight auxiliary registers with dedicated arithmetic unit



### 4.3 TMS320C2x Multiplier/ALU

The performance and parallelism of the 'C2x-generation architecture become evident with study of the multiplier and accumulator section of the device (see Figure 4–1).

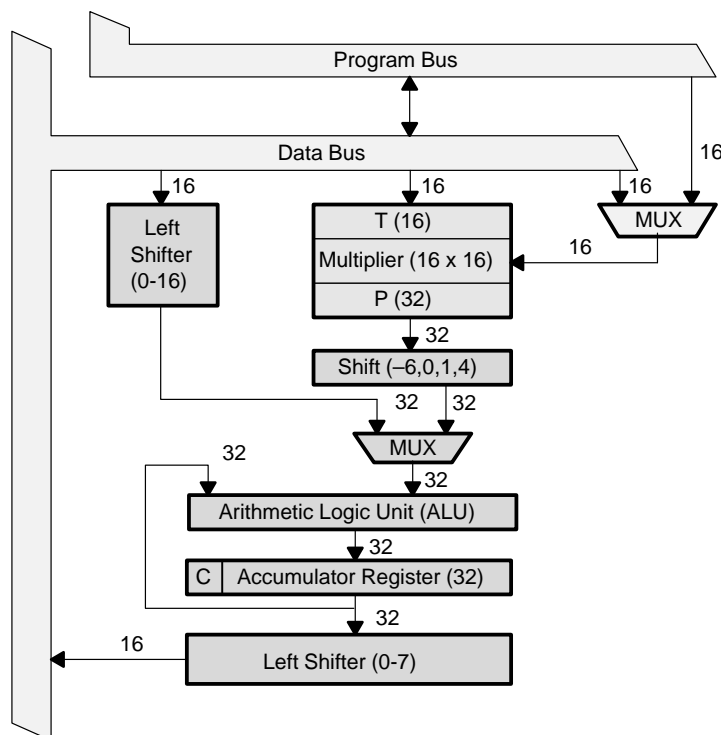
In a manner similar to that of the 'C1x generation, the on-chip multiplier performs a 16 x 16-bit multiply with a 32-bit product in a single cycle. However, to double the performance, the 'C2x-generation devices can fetch two data operands when executing the multiply and accumulate (MAC).

The 16-bit barrel shifter scales data in parallel with ALU operations; data is shifted up to 16 bits during the same cycle it is used in the ALU. The 0-, 1-, 4-, or 6-bit left shifter also operates in parallel with the ALU to support both integer and fractional math.

Features of the 'C2x multiplier/ALU include:

- ☐ A single-cycle 16-bit x 16-bit multiply that yields a 32-bit product
- ☐ Support for simultaneous acquisition of the program and two data operands
- ☐ Support for simultaneous ALU and multiplier operations
- ☐ 0- to 16-bit left post-shifter

Figure 4–1. TMS320C2x Multiplier/ALU



## 4.4 TMS320C2x Interface to Off-Chip Devices

Internally, the 'C2x generation uses a modified Harvard architecture to perform program and data fetches in parallel. Externally, these buses are multiplexed together to reduce package size and cost. Most applications place either program or data in on-chip memory, with the other residing in off-chip memory to minimize external bus conflicts and maximize performance (see Figure 4–2).

The proper strobe is selected by the processor based on whether a program fetch or I/O command is being executed. These signals ease the interface to external memory and peripherals.

The READY line supports the addition of wait states for accessing external memory. This is useful for low-cost systems that use slow external memory to reduce cost yet maintain high performance through on-chip memory.

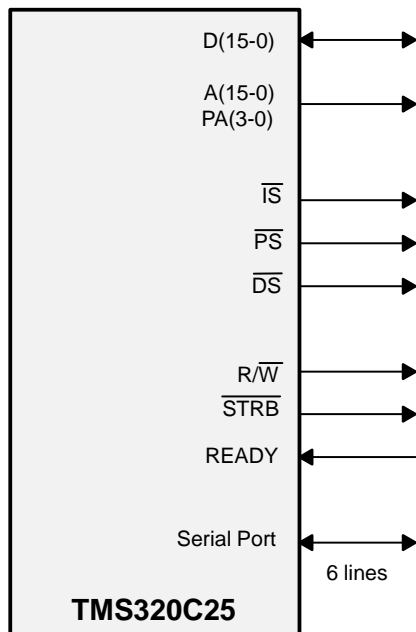
The  $\overline{\text{HOLD}}$  (hold) and  $\overline{\text{HOLDA}}$  (hold acknowledge) signals allow an external processor to stop execution, directly access the 'C25's external memory, and resume execution. This is quite useful in either designs with multiple 'C25s or systems that have a host processor. A separate I/O select signal provides 16 I/O ports using the 16-bit data bus. The I/O ports provide an easy interface to ADCs and DACs, because the I/O ports have a separate select signal in addition to the standard data bus interface signals.

The serial port provides a glueless interface to analog interface circuits (AICs) such as the 'C44. The serial port is double-buffered with separate transmit and receive circuitry, providing serial transmission rates of up to 6.25 Mbps.

Features of the 'C2x interface to off-chip devices include:

- ☐ Microprocessor-like 16-bit interface over a single bus
- ☐ Wait states for communication with slow memories or peripherals
- ☐ 16 input/output channels capable of single-cycle I/O accesses
- ☐ Serial port

Figure 4–2. TMS320 Interface to Off-Chip Devices



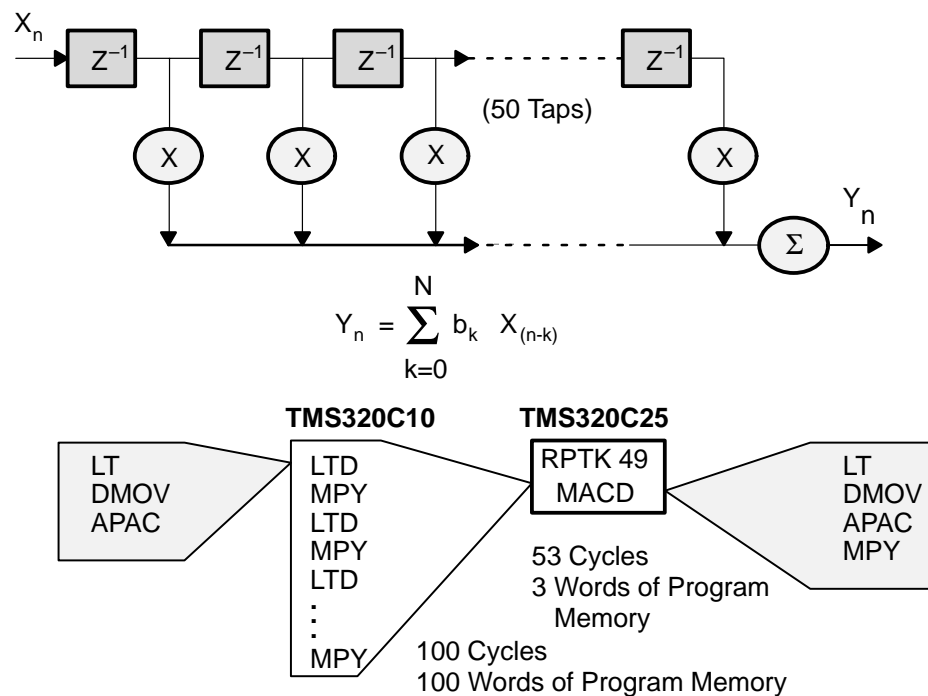
## 4.5 TMS320C25 Sum of Products Example

The example shown in Figure 4–3 is an implementation of a 50-tap FIR filter, which is a sum of products. This operation requires four functions for each tap in the filter. First, the temporary register (TR) contents must be loaded into the multiplier using the LT command.

Second, a data move (DMOV) is executed. DMOV is a method to address "aging" data sets for common DSP algorithms. For example, after the first set of calculations is performed on an FIR filter data set, a new data value must be brought in and the oldest value discarded. DMOV allows this by treating data in a circular fashion, with the oldest and newest values located side by side. At the end of each calculation, a new data value is placed in memory at the location of the oldest value. Third, the result of the previous multiply is accumulated (APAC), and finally the multiply (MPY) is performed.

On a 'C1x, you could perform the first three functions in parallel using the LTD instruction, with the multiply taking a second cycle. The 'C25 takes this a step further by executing all four functions in a single cycle with the MACD (multiply, accumulate, and data move) instruction. Using the MACD instruction in combination with the repeat (RPTK) instruction allows a significant reduction in program space and doubles the performance.

Figure 4–3. TMS320C25 Sum of Products Example



## 4.6 TMS320C25

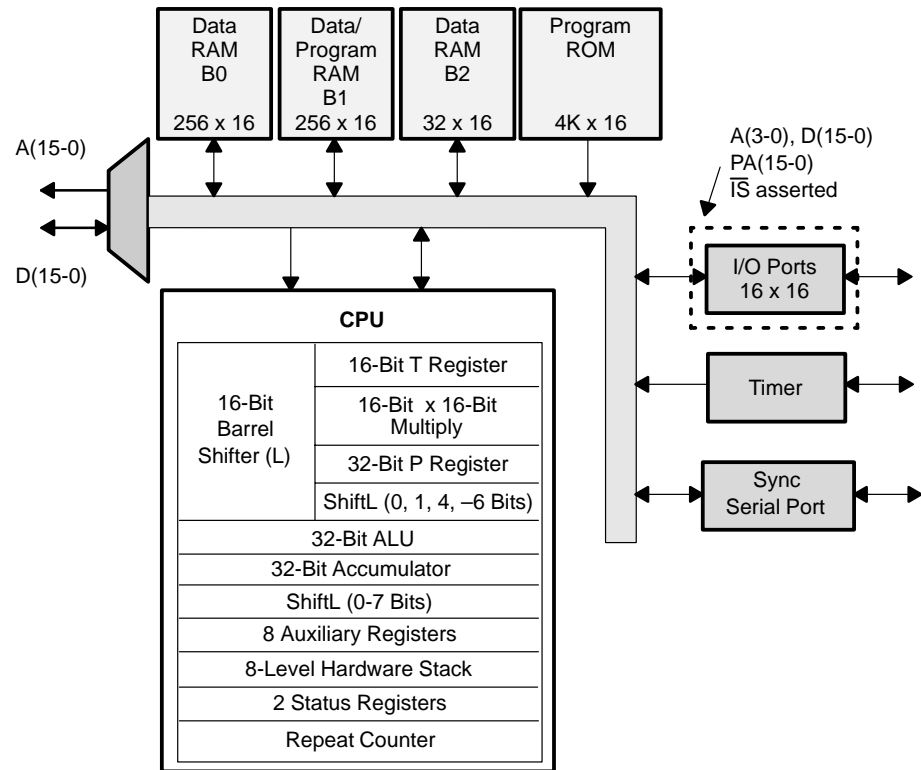
The 'C25 (see Figure 4–4) includes an instruction set with 134 general-purpose and DSP instructions, eight auxiliary registers, an 8-level hardware stack, 4K 16-bit words of on-chip program ROM and 544 16-bit words of on-chip RAM that can be configured as data or data/program, an external address reach of 64K words for both data and program, a serial port, and 16 I/O ports. The 'C25 operates at 80 ns, 100 ns, and 120 ns, which translates to 12.5 MIPS, 10 MIPS, and 8.25 MIPS, respectively. The 'C25 comes in 68-pin PLCC and 80-pin PQFP OTP ('P25) package versions.

The OTP version replaces the 4K program ROM with OTP ROM for prototypes prior to ROM code release. This benefits production on medium-volume designs that need small space or power. It also makes a DSP system easy to implement.

Additional features of the 'C25 include:

- ☐ Single-cycle multiply and accumulate (MAC)
- ☐ Repeat instruction for increased execution efficiency
- ☐ 32-bit ALU accumulator
- ☐ Eight auxiliary registers with dedicated ALU
- ☐ 16 x 16 bit parallel multiplier with 32-bit product
- ☐ 0- to 16-bit parallel shifter
- ☐ Accepts source code from the 'C1x generation
- ☐ Multiprocessor features
- ☐ Microprocessor features
- ☐ On-chip memory-mapped peripherals
- ☐ ANSI C compiler

Figure 4–4. TMS320C25 Block Diagram



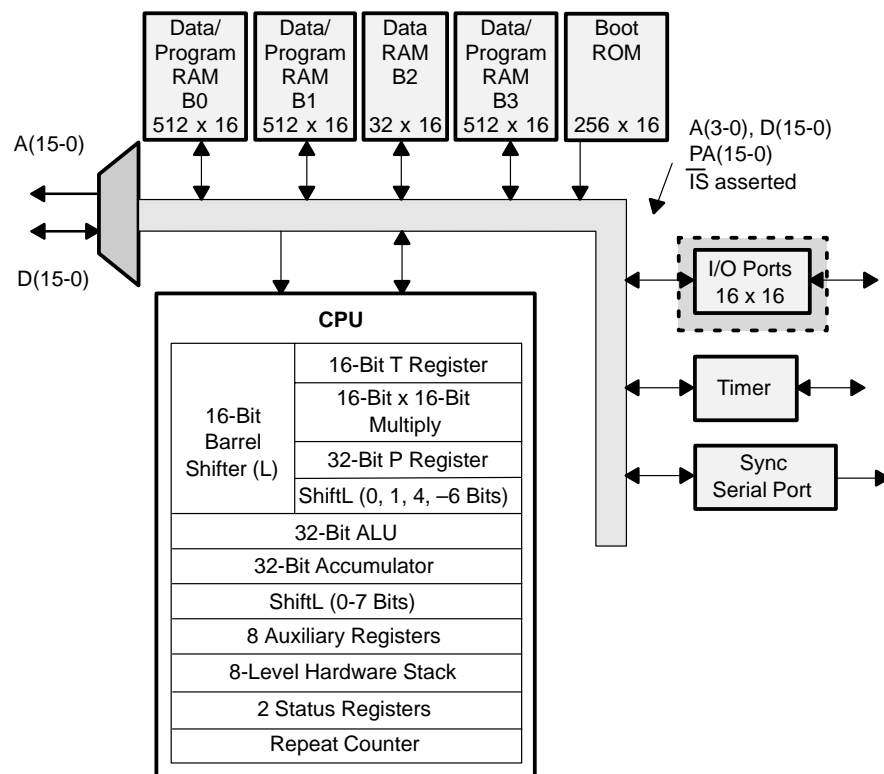
## 4.7 TMS320C26

The 'C26 (see Figure 4–5) is object-code and pin compatible with the 'C25. The on-chip memory of the 'C26 has been configured for RAM-based systems. The device has a boot ROM and 1.5K 16-bit words of RAM, which can be configured as data or program.

Features of the 'C26 include:

- ☐ 100-ns instruction cycle time
- ☐ Accepts source code from the 'C1x generation
- ☐ 128K-word extended address reach
- ☐ Single-cycle multiply and accumulate (MAC)
- ☐ 134 general-purpose and DSP instructions
- ☐ Multiprocessor features
- ☐ Microprocessor features
- ☐ On-chip memory-mapped peripherals
- ☐ ANSI C compiler
- ☐ 68-pin PLCC package

Figure 4–5. TMS320C26 Block Diagram



## **4.8 Tools for TMS320C2x**

For information about the code generation and debugging tools available for the 'C2x devices, refer to Chapter 15, Code Generation Tools, and Chapter 16, System Integration and Debugging Tools. Table 2–14 and Table 2–15 in Chapter 2, Selection Guide, provide part numbers and host system information.



# TMS320C2xx Devices

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The TMS320C2xx generation combines strong performance with low cost. The 'C2xx generation is a 16-bit fixed-point, Harvard architecture family that offers performance up to 40 MIPS and power dissipation of as little as 1.1 mW/MIPS.

<b>Topic</b>	<b>Page</b>
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5.6 TMS320C2xx Memory Bus .....	5-8
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## 5.1 TMS320C2xx Introduction

The 'C2xx devices are fully static, are offered in 3-V versions, have a full CPU shutdown idle mode, and can use on-chip phase-locked loop (PLL) options. These features all contribute to reductions in system power requirements.

The 'C2xx devices are source-code compatible with the 'C2x generation and are upwardly compatible with the 'C5x generation. The 'C5x assembler accepts 'C2xx instructions as well as 'C5x instructions. The 'C2xx instruction set incorporates all the 'C2x instructions and adds 11 new ones.

The core CPU of the 'C2xx features 544 words of dual-access RAM. The external address reach of the 'C2xx is 224K words; 64K words of data, program, and I/O, and 32K words of global memory for multiprocessor operation.

The 'C2xx generation is supported by a full suite of development tools that make designing with these devices easy. Texas Instruments offers a C compiler/assembler/linker, simulator, evaluation module, and an emulator/debugger that supports nonintrusive IEEE Standard 1149.1-compliant (JTAG) scan-based emulation. Numerous third-party companies also provide development tools for the 'C2xx generation.

All 'C2xx devices are available in speeds of 40 MHz, 57 MHz, and 80 MHz except for the 'C209, which is available in 40 MHz and 57 MHz. These speeds translate into cycle time and MIPS as shown in Table 5–1.

*Table 5–1. 'C2xx Clock Speed and MIPS*

<b>Clock Speed (MHz)</b>	<b>Instruction Cycle Time (ns)</b>	<b>MIPS</b>
40	50	20
57	35	28.5
80	25	40

The 'C2xx generation also features the first TI DSPs with on-chip flash memory. The 'F206 has 32K words of flash memory and 4.5K words of RAM, enabling designers to eliminate costly off-chip memory.

## 5.2 TMS320C2xx Key Features

Following are the key features of the TMS320C2xx generation. When only certain devices have a particular feature, they are named in parentheses following the feature's description.

- ☐ Up to 4.5K data/program RAM on chip
- ☐ 32K words of flash memory on-chip ('F206)
- ☐ 32-bit ALU/accumulator
- ☐ 16 x 16-bit parallel multiplier with a 32-bit product
- ☐ Repeat instructions for efficient use of program space and enhanced execution
- ☐ 16-bit on-chip timer
- ☐ 16-bit barrel shifter
- ☐ Eight-level hardware stack
- ☐ Built-in power-down mode
- ☐ Software wait-state generator
- ☐ 80- or 100-pin TQFP packages
- ☐ Various PLL options for reduced electromagnetic interference (EMI) and system power dissipation

### 5.3 TMS320C2xx Synchronous Serial Port

The 'C2xx offers a full-duplex framed synchronous serial port with up to 20-Mbps throughput (at a 25-ns instruction cycle time). The transfer rate is one-half the device clockout rate. This bidirectional synchronous serial port provides direct communication with serial devices such as codecs, serial ADCs, and other serial systems. The serial port can be used for intercommunication between processors in multiprocessing applications.

Both the receive and transmit sides of the serial port have a 4-level-deep buffer or FIFO, allowing the CPU to accept an interrupt at either 1, 2, 3, or 4 levels deep. This capability means less intervention from the CPU, as well as increased flexibility and efficiency with respect to data transfers.

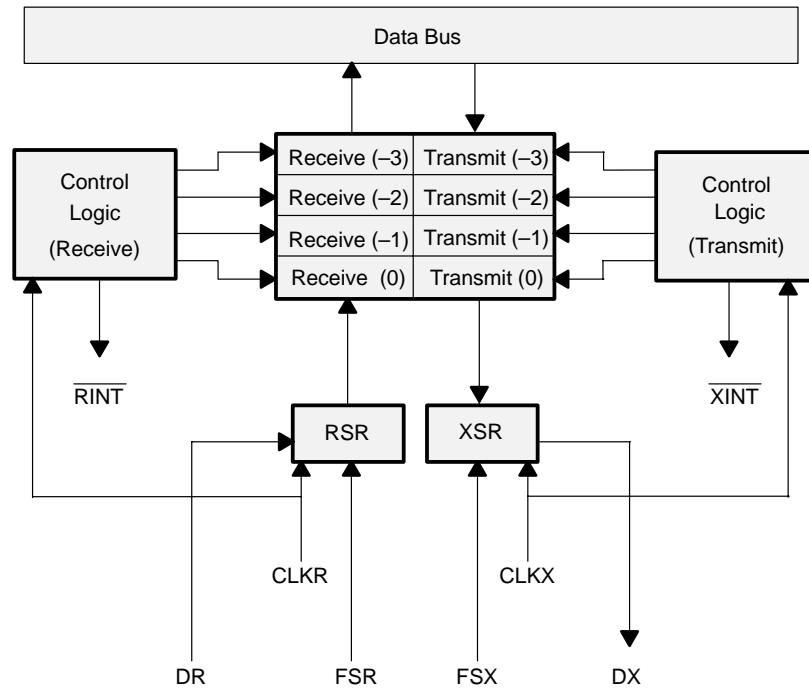
The 'C2xx synchronous serial port features:

- ☐ Full-duplex framed synchronous serial port
- ☐ 4-word x 16-bit buffer to reduce interrupt service routine (ISR) overhead
- ☐ Serial port performance
  - 20 Mbps at 25 ns
  - 14.28 Mbps at 35 ns
  - 10 Mbps at 50 ns
- ☐ Transfer rate one-half that of the CPU rate

All 'C2xx devices, except the 'C209, feature this serial port.

Figure 5–1 shows a block diagram of the synchronous serial port.

Figure 5–1. TMS320C2xx Synchronous Serial Port



## 5.4 TMS320C2xx Asynchronous Serial Port

The 'C2xx offers an asynchronous serial port that is full-duplex and double-buffered. It accepts 8-bit data and can be programmed through a register to accept baud rates of up to 2.5 Mbps. The asynchronous serial port can be used to communicate with other devices such as microcontrollers or for RS-232 connections supporting data transfers of up to 115.2 kbps.

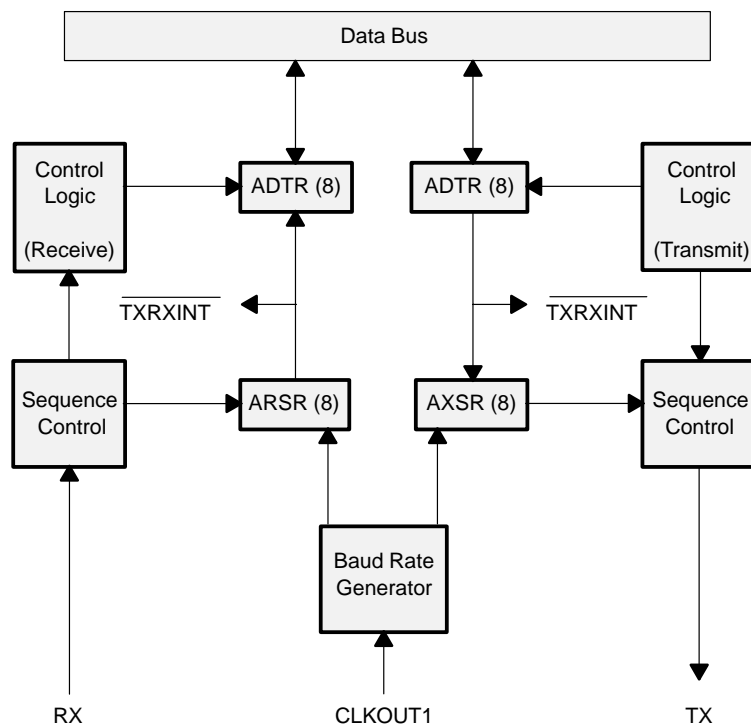
Features included with the 'C2xx asynchronous serial port are:

- ☐ Full duplex
- ☐ Double buffered
- ☐ 8-bit data transfers
- ☐ 16-bit register for baud-rate generation
- ☐ Baud rates up to 2.5 Mbps (at a 25-ns instruction cycle time)

All 'C2xx devices, except the 'C209, feature this asynchronous serial port.

Figure 5–2 shows a block diagram of the asynchronous serial port.

Figure 5–2. TMS320C2xx Asynchronous Serial Port



## 5.5 TMS320C2xx Boot Loader

Some of the 'C2xx devices have an on-chip hard-coded boot loader, which allows you to load code from an 8-bit external EPROM into internal or external RAM. The EPROM is mapped into global data memory. Once the boot loading operation begins, 8-bit data is read by the device and reassembled into 16-bit words to a user-specified destination. When complete, control of the device is passed to the start of the program.

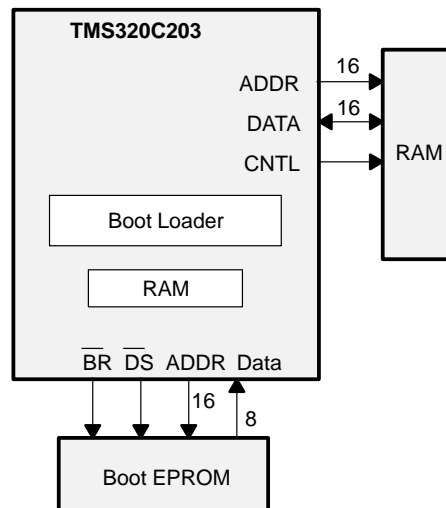
Features of the 'C2xx boot loader are:

- ☐ Load from 8-bit external EPROM into internal/external RAM
- ☐ EPROM is mapped into global data memory space
- ☐ Dedicated boot loader pin
- ☐ Boot loader operation:
  - Reads 8-bit data
  - Reassembles into 16-bit words
  - Loads to user-specified destination
  - When complete, control passes to start of program

The 'C203 features this boot loader.

Figure 5–3 shows a block diagram of the boot loader.

Figure 5–3. TMS320C2xx Boot Loader



## **5.6 TMS320C2xx Memory Bus**

The 'C2xx advanced Harvard-type architecture maximizes processing power by maintaining two separate memory bus structures, program and data, for full-speed execution. This multiple bus structure allows reading both data and instructions simultaneously. Instructions support data transfers between the two spaces. This architecture lets you store coefficients in program memory to be read in RAM, eliminating the need for a separate coefficient ROM. This, coupled with a four-level-deep pipeline, allows the 'C2xx to execute most instructions in a single cycle.

The 'C2xx dual-access RAM (DARAM) allows writes to and reads from the RAM in the same cycle without the address restrictions of single-access RAM (SARAM). The DARAM is configured in three blocks: block B0, block B1, and block B2. Block B0 is a 256-word block that can be configured as data or program memory. Block B1 is 256 words in data memory and block B2 is 32 words in data memory.

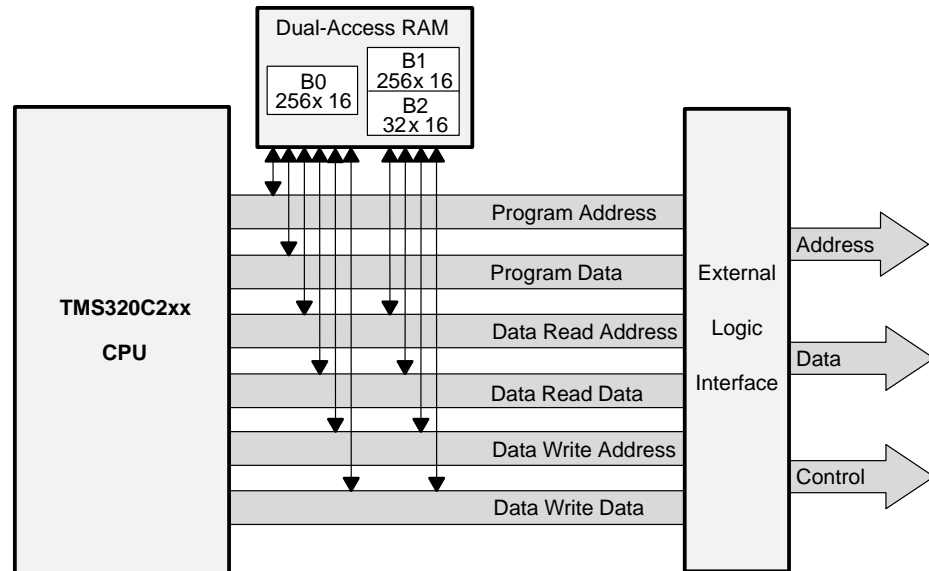
Some 'C2xx devices also have SARAM and/or ROM. Also, the 'F206 includes 32K words of flash memory. Flash memory offers an excellent alternative to RAM because of its lower cost and nonvolatile storage and is an alternative to ROM due to its reprogrammability.

The ability of the DARAM to perform two accesses in one cycle, coupled with the parallel nature of the 'C2xx architecture, enables the 'C2xx devices to perform three concurrent memory accesses in any given machine cycle.

Figure 5–4 shows a block diagram of the memory bus.



Figure 5–4. TMS320C2xx Memory Bus



## 5.7 TMS320C203

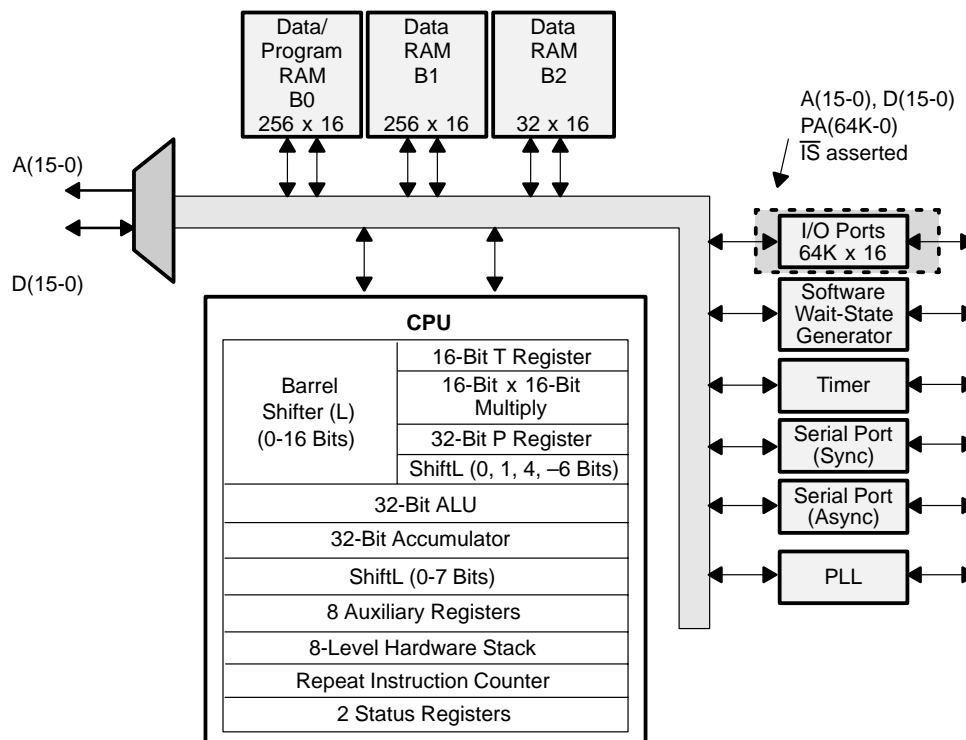
The 'C203 incorporates all the features of the 'C2xx core and adds two high-performance serial ports for enhanced communication with peripheral devices. There is one synchronous serial port with a four-level-deep FIFO, which results in less intervention from the CPU, but at a low cost. One full-duplex asynchronous serial port, a programmable wait-state generator, and a 16-bit timer are also included. The serial ports, timer, and wait-state generator are mapped into I/O space. The 'C203 is packaged in a 100-pin TQFP.

Features of the 'C203 include:

- ☐ 25-, 35-, and 50-ns instruction cycle times
- ☐ 192K-word external address reach
- ☐ Accepts source code from the TMS320C1x/'C2x generations
- ☐ ANSI C compiler
- ☐ +2, x1, x2, and x4 PLL options
- ☐ IEEE 1149.1-standard (JTAG) emulator control
- ☐ Boot ROM option
- ☐ Full-duplex synchronous serial port with four-level-deep FIFO
- ☐ Full-duplex asynchronous serial port (UART)
- ☐ 100-pin TQFP package

Figure 5–5 shows a block diagram of the 'C203.

Figure 5–5. TMS320C203 Block Diagram



The synchronous serial port has full-duplex, framed operation at up to 20 Mbps throughput. The transfer rate is one-half the device clockout rate. Both the receive and transmit sides of the serial port have a first-in first-out (FIFO) allowing the CPU to accept an interrupt at levels 1, 2, 3, or 4. This capability means less intervention from the CPU as well as increased flexibility and efficiency with respect to data transfers.

The asynchronous serial port is a universal asynchronous receive/transmit (UART) device. It offers full-duplex and double-buffered operation. It accepts 8-bit data and can be programmed via a register to accept baud rates up to 2.5 Mbps. The asynchronous serial port can be used to communicate with other devices, such as microcontrollers or for RS-232 connections supporting data transfers of up to 115.2K bps.

## 5.8 TMS320C204

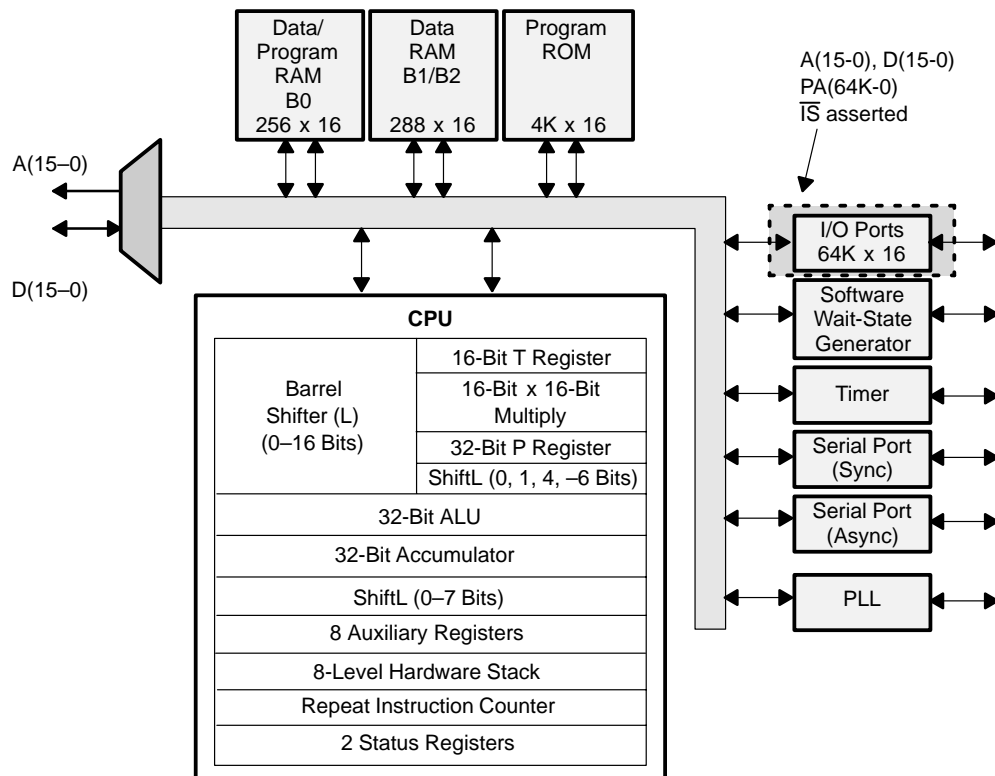
The 'C204 is based on the same core as the 'C203 and offers the same performance and peripherals as the 'C203. The 'C204 adds 4K words of masked ROM for low-cost, on-chip program storage. The 'C204 is packaged in a 100-pin TQFP and is pin-compatible with the 'C203.

Features of the 'C204 include:

- ☐ 25-, 35-, and 50-ns instruction cycle times
- ☐ 192K-word external address reach
- ☐ Accepts source code from the 'C1x/C2x generations
- ☐ ANSI C compiler
- ☐  $\div 2$ , x1, x2, and x4 PLL options
- ☐ IEEE 1149.1-standard (JTAG) emulator control
- ☐ Full-duplex synchronous serial port with four-level-deep FIFO
- ☐ Full-duplex asynchronous serial port (UART)
- ☐ 100-pin TQFP package

Figure 5–6 shows a block diagram of the 'C204.

Figure 5–6. TMS320C204 Block Diagram



## 5.9 TMS320F206

The 'F206 is the first digital signal processor from Texas Instruments with on-chip flash memory. The 'F206 Flash DSP has 32K words of flash integrated into program memory. Flash memory is attractive for program memory because it has a lower cost than SRAM and more flexibility than ROM. The flash memory on the 'F206 can be programmed through the 'C2xx emulator for easy changes in the program during prototyping. The reprogrammability of the flash allows quick changes to the product to adapt to new standards and to add new features to the end equipment.

In addition to the flash, the 'F206 also has a total of 4.5K of on-chip RAM. This level of memory integration allows a true one-chip solution for many systems.

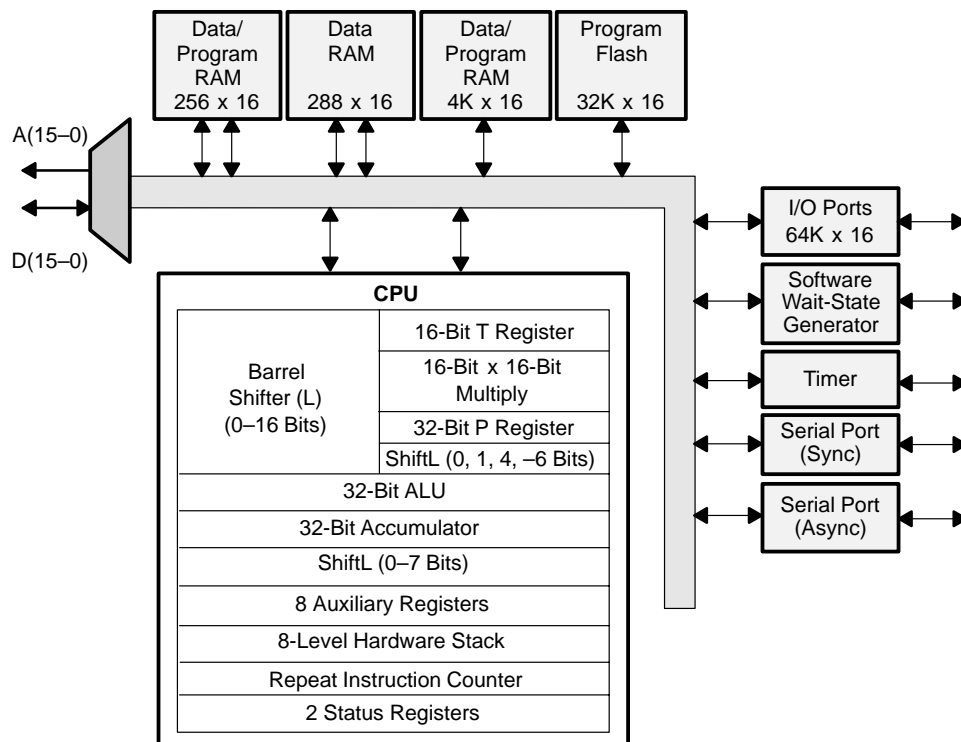
The 'F206 is based on the same 'C2xx core as other members of this generation and incorporates the same serial ports as the 'C203. The 'F206 comes in a 100-pin TQFP package and is footprint-compatible with the 'C203 and 'C204.

Features of the 'F206 Flash DSP include:

- ☐ 25-, 35-, and 50-ns instruction cycle times
- ☐ 192K-word external address reach
- ☐ Accepts source code from the 'C1x/C2x generations
- ☐ ANSI C compiler
- ☐ Divide-by-two, multiply-by-one, -two, and -four PLL options
- ☐ IEEE 1149.1-standard (JTAG) emulator control
- ☐ Full-duplex synchronous serial port with four-level-deep FIFO
- ☐ Full-duplex asynchronous serial port (UART)
- ☐ 100-pin TQFP package

Figure 5–7 shows a block diagram of the 'F206.

Figure 5–7. TMS320F206 Block Diagram



## 5.10 TMS320C209

The 'C209 was the first member of the 'C2xx generation. It takes the 'C2xx core and adds 4K words of ROM and an additional 4K words of RAM (total of 4.5K words). The large on-chip memory, small packaging, and low cost make this device attractive for space-constrained applications such as small form factor hard-disk drives.

The 'C209 does not include the serial ports of the 'C203. It has performance ratings of 20 MIPS and 28.5 MIPS and comes in an 80-pin TQFP.

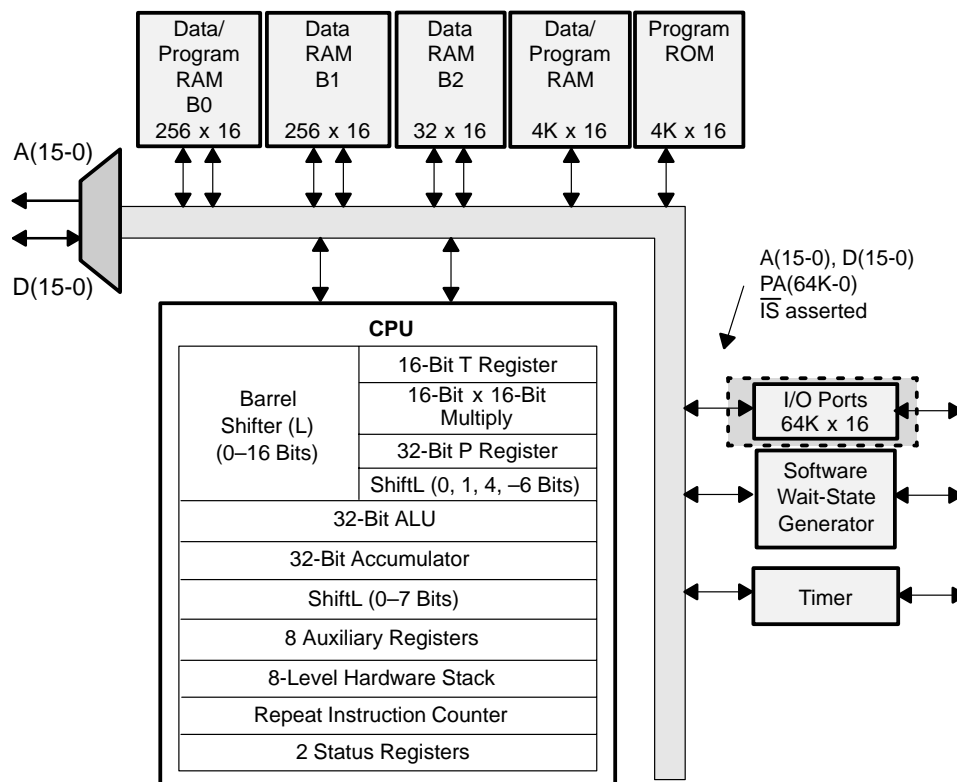
The TMS320C209 features:

- ☐ 35- and 50-ns instruction cycle times
- ☐ 4K 16-bit words of RAM
- ☐ Accepts source code from the 'C1x/C2x generations
- ☐ ANSI C compiler
- ☐  $\div 2$ ,  $\times 2$  PLL option
- ☐ IEEE 1149.1-standard (JTAG) emulator control
- ☐ 80-pin TQFP package

Figure 5–8 shows a block diagram of the 'C209.



Figure 5–8. TMS320C209 Block Diagram



## **5.11 Tools for TMS320C2xx**

For information about the code generation and debugging tools available for the 'C2xx devices, refer to Chapter 15, Code Generation Tools, and Chapter 16, System Integration and Debugging Tools. Table 2–14 and Table 2–15 in Chapter 2, Selection Guide, provide part numbers and host system information.

# TMS320C24x DSP Controllers

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The 'C24x devices are an optimized set of digital motor-control processors that include event managers specifically designed to enable the types of robust and energy-efficient motor-control designs required for the future. These products are particularly well-suited for variable-speed control of brushless motors, including dc permanent magnet, ac induction, and switched reluctance motors.

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## 6.1 TMS320C24x DSP Controllers Introduction

The TMS320C24x DSP controllers are motor-control-optimized members of Texas Instruments TMS320C2xx DSP generation. They have been specifically designed for control system applications, and they combine all of the necessary integration for single-chip controller implementations, providing the high performance of a DSP core with the on-chip peripherals of a microcontroller. This approach yields a high-performance DSP controller that is an affordable alternative to both slower MCUs and expensive ASIC or multichip designs. At 50 ns instruction cycle times, the 'C24x offers 10 to 20 times the speed of traditional 16-bit microcontrollers and microprocessors.

The 16-bit, fixed-point core that is the DSP engine for the 'C24x devices provides analog designers a digital solution that does not sacrifice the precision and performance of their systems. In fact, system performance can be enhanced through the use of advanced control algorithms for techniques such as adaptive control, Kalman filtering, and state control. The TMS320 DSP controllers offer reliability and programmability. Analog control systems, on the other hand, are hard-wired solutions and can experience performance degradation due to aging and other environmental factors.

The high-speed central processing unit (CPU) of the TMS320 DSP controllers allows the digital designer to process algorithms in real time rather than approximate results through look-up tables. The instruction set of these DSP controllers, which incorporates both signal-processing instructions and general-purpose functions, coupled with the extensive development support available for the TMS320 DSP family, reduces development time and provides the same ease of use as traditional 8- and 16-bit microcontrollers.

The 'C24x DSP controllers leverage a set of peripheral functions that allows TI to configure various family members for different price/performance points or application optimization. This library of both digital and mixed-signal peripherals includes:

- ☐ Timers
- ☐ Serial communication ports
- ☐ Data converters
- ☐ Event managers

## 6.2 TMS320C24x Architecture

The architectural design of the 'C24x is based on the 'C2xx DSP core. The operational flexibility and speed of the 'C24x is a result of an advanced, modified Harvard architecture (which has separate buses for program and data memory), a multilevel pipeline, on-chip peripherals, on-chip memory, and a highly specialized instruction set. The 'C24x performs up to 40 MIPS.

The 'C24x devices are source-code compatible with the 'C2x generation and are upwardly compatible with the 'C5x generation. The 'C5x assembler accepts 'C24x instructions as well as 'C5x instructions. The 'C24x instruction set incorporates all the 'C2x instructions and adds 11 new ones.

The core CPU of the 'C24x features 544 words of dual-access RAM. The external address reach of the 'C24x is 224K words; 64K words of data, program, and I/O, and 32K words of global memory for multiprocessor operation.

The 'C24x series is supported by a full suite of development tools that make designing with these devices easy. Texas Instruments offers a C compiler/assembler/linker, a simulator, and an emulator/debugger that supports non-intrusive IEEE Standard 1149.1-compliant (JTAG) scan-based emulation. Numerous third-party companies also provide development tools for the 'C24x generation.

The 'C24x generation also features a DSP controller with on-chip flash memory. The TMS320F240 includes 16K words of flash memory, enabling designers to eliminate costly off-chip memory.

## 6.3 TMS320C24x Key Features

Following are the key features of the 'C24x series:

- ☐ Processing hardware
  - 32-bit arithmetic logic unit (CALU)
  - 32-bit accumulator
  - 16-bit  $\times$  16-bit parallel multiplier with a 32-bit product capability
  - Three scaling shifters
  - Eight 16-bit auxiliary registers with a dedicated arithmetic unit for indirect addressing of data memory
- ☐ Memory
  - 224K words  $\times$  16-bit maximum addressable memory space (64K words program, 64K words data, and 64K words I/O, and 32K words global)
  - On-chip dual-access RAM (DARAM) on-chip
  - On-chip ROM or flash EPROM
  - External memory interface module with software wait state, 16-bit address lines, and 16-bit data lines
  - Support of hardware wait states
- ☐ Program control:
  - Four-level pipeline operation
  - Eight-level hardware stack
  - User-maskable interrupts
- ☐ Instruction set
  - Single-instruction repeat operation
  - Single-cycle multiply/accumulate instructions
  - Memory block move instructions for program/data management
  - Indexed-addressing capability
  - Bit-reversed indexed-addressing capability for radix-2 FFTs

- ❑ Power:
  - Static CMOS technology
  - Four power-down modes to reduce power consumption
- ❑ Emulation: IEEE Standard 1149.1 boundary-scan logic interfaced to on-chip scan-based emulation logic
- ❑ Speed: 50-ns instruction cycle time, with most instructions single cycle
- ❑ Code compatibility with TMS320 fixed-point devices:
  - Source code compatible with the 'C25 and 'C2xx devices, and upwardly compatible with the 'C5x generations of DSPs
- ❑ On-chip peripherals: See Table 6–1 and Figure 6–1.

Figure 6–2 shows a block diagram of the 'C240 DSP controllers.

*Table 6–1. Device Configurations*

Features	'F240/'C240
On-chip ROM/flash memory (words)	16K flash/ROM
On-chip dual-access RAM (words)	544
Total memory-address range (words)	64K program 64K data 64K I/O 32K global
Timers	3 general-purpose with compares 1 watchdog
Serial communications interface (SCI)	1
Serial peripheral interface (SPI)	1
Compare outputs	9 total
Capture inputs	4 total 2 quadrature encoder pulse (QEP)
I/O functions	28
Analog-to-digital convertors (ADCs)	2 10-bit ADCs with 16 total inputs and 10 $\mu$ s conversion
Pulse-width modulation (PWM) outputs	12 total
Package	132-pin PQFP

Figure 6–1. TMS320C240/F240 Peripheral Overview

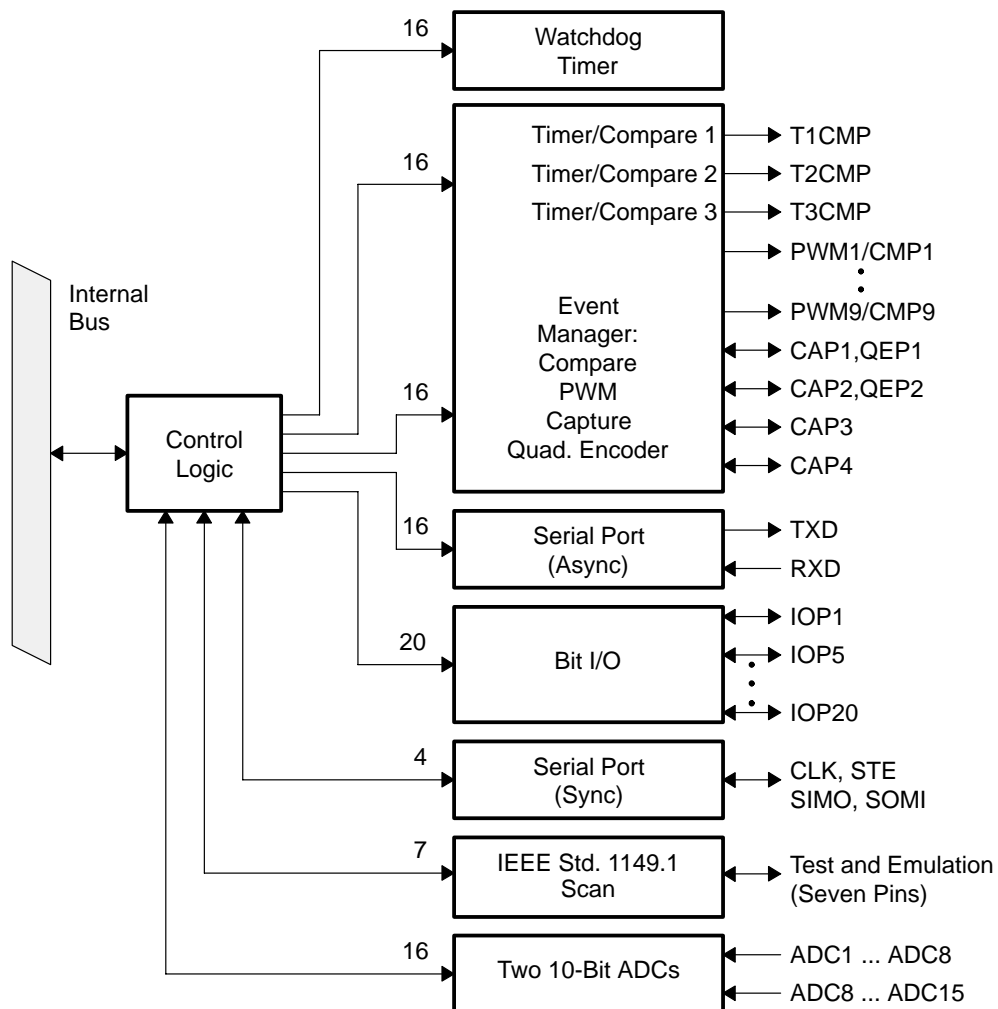
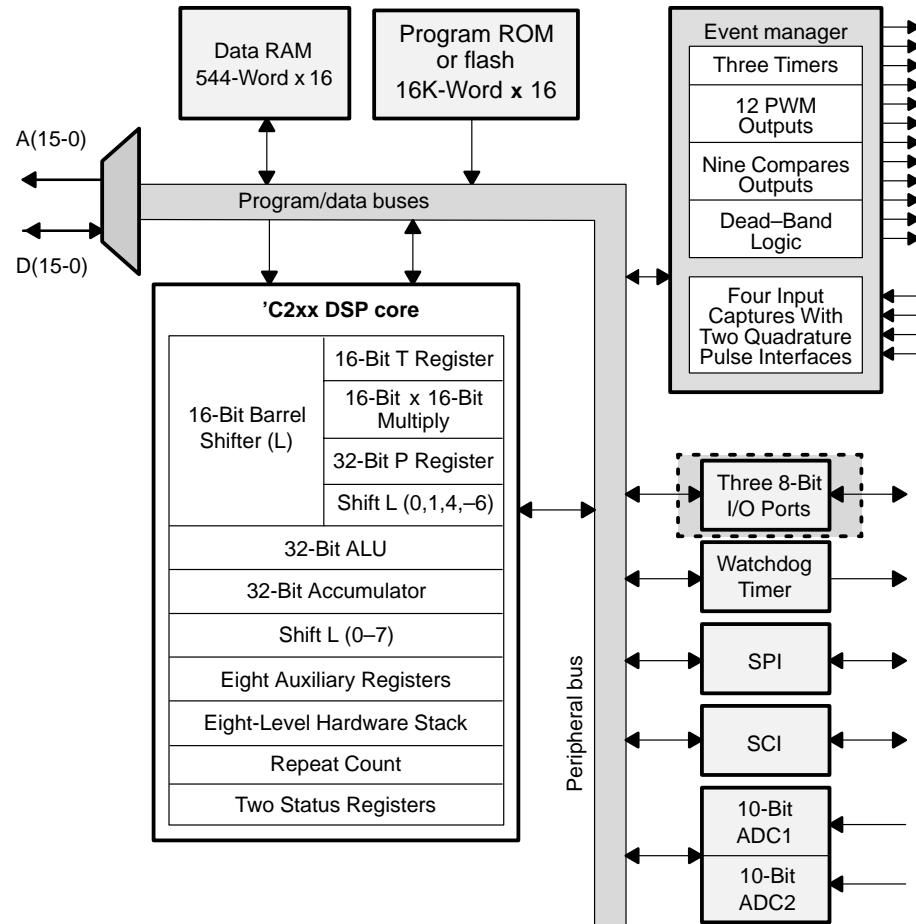




Figure 6–2. TMS320C240/F240 Block Diagram



## 6.4 TMS320C24x Memory Bus

The 'C2xx advanced Harvard-type architecture maximizes processing power by maintaining two separate memory bus structures, program and data, for full-speed execution. This multiple bus structure allows reading both data and instructions simultaneously. Instructions support data transfers between the two spaces. This architecture lets you store coefficients in program memory to be read in RAM, eliminating the need for a separate coefficient ROM. This, coupled with a four-level-deep pipeline, allows the 'C2xx to execute most instructions in a single cycle.

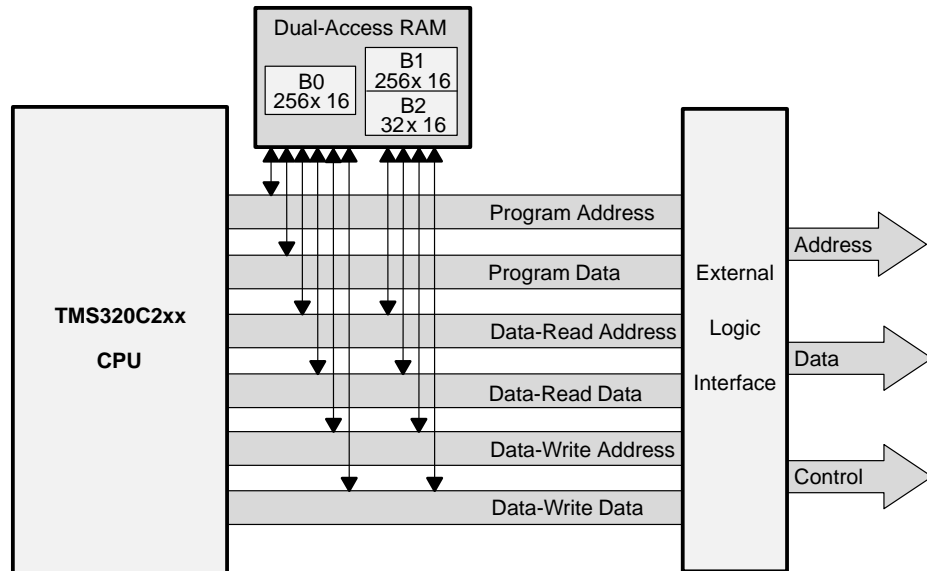
The 'C2xx DARAM allows writes to and reads from the RAM in the same cycle without the address restrictions of single-access RAM (SARAM). The DARAM is configured in three blocks: block B0, block B1, and block B2. Block B0 is a 256-word block that can be configured as data or program memory. Block B1 is 256 words in data memory and block B2 is 32 words in data memory.

The 'C240 includes 16K words of ROM. The 'F240 includes 16K words of flash memory. Flash memory offers an excellent alternative to RAM because of its lower cost and nonvolatile storage and is an alternative to ROM due to its reprogrammability.

The ability of the DARAM to perform two accesses in one cycle, coupled with the parallel nature of the 'C2xx architecture, enables the 'C2xx devices to perform three concurrent memory accesses in any given machine cycle.

Figure 6–3 shows a block diagram of the memory bus.

Figure 6–3. TMS320C24x Memory Bus



## 6.5 TMS320C240/F240 Event Manager (EV) Module

The 'C240/'F240 event manager module consists of timers, compare units, simple compares, a capture unit, and a quadrature encoder pulse (QEP) circuit. These items are discussed in the following subsections. Figure 6–4 shows a block diagram of the 'C240 Event Manager.

### 6.5.1 General-Purpose (GP) Timers

There are three GP timers on the TMS320C240. The GP timer includes:

- ☐ A 16-bit timer up-, up/down-counter
- ☐ A 16-bit timer compare register (with shadow register)
- ☐ A 16-bit timer period register (with shadow register)
- ☐ A 16-bit timer control register
- ☐ Selectable internal or external input clocks
- ☐ A programmable prescaler for either internal or external counter input clocks
- ☐ Control logic and four maskable interrupts and interrupt flags: underflow, overflow, timer compare, and period interrupts
- ☐ A timer compare output pin with configurable low- and high- active states
- ☐ A selectable direction (DIR) input pin (to count up or down when the directional up/down count mode is selected)

The GP timers can be operated independently or in synchronization. A 32-bit GP timer can be configured using GP timer2 and timer3. The compare register associated with each GP timer can be used for compare function and PWM waveform generation. There are two single and three continuous modes of operation for each GP timer in up- or up/down-counting operations. Internal or external input clocks with a prescaler are used for each GP timer. The state of each GP timer/compare output is configurable by the general-purpose timer control register (GPTCON). GP timers also provide a timebase for the 'C240 peripherals; GP timer1 for all the compares and PWM circuits, GP timer1 or timer2 for the simple compares to generate additional compare or PWMs, GP timer2 or timer3 for the capture units and the QEP counting operations.

## 6.5.2 Compare Units

There are three full compare units on the 'C240. These compare units use GP timer1 as the timebase and generate six outputs for compare and high-precision PWM waveforms generation using the programmable deadband circuit. The states of the six outputs are configurable independently.

### 6.5.2.1 Simple Compares

The 'C240 is equipped with three simple compares that can be used to generate three additional independent compare or high-precision PWM waveforms. GP timer1 or timer2 can be selected as the timebase for the three simple compares. The states of the outputs of the three simple compares are configurable as low-active, high-active, or forced low or high independently.

### 6.5.2.2 Compare/PWM Waveform Generation

Up to 12 compare and/or high-precision PWM waveforms (outputs) can be generated by the 'C240; three independent pairs (six outputs) by the three compare units with *programmable deadbands*, three independent compare or PWMs (three outputs) by the simple compares, and three independent compare and PWMs (three outputs) by the GP timer compares.

### 6.5.2.3 Compare/PWMs Characteristics

The characteristics of the compare/PWM waveforms include:

- ☐ 16-bit, 50-ns resolutions
- ☐ Programmable deadband for the PWM output pairs, from zero to 102  $\mu$ s
- ☐ Minimum deadband width of 50 ns
- ☐ On-the-fly change of the PWM carrier frequency, the PWM frequency wobbling
- ☐ On-the-fly change of the PWM pulse widths within and after each PWM period
- ☐ External maskable power and drive protection interrupts
- ☐ Pulse pattern generator circuit (Figure 6–4), for programmable generation of asymmetric, symmetric, and four-space vector PWM waveforms
- ☐ Minimized CPU overhead using auto-reload of the compare and period registers

### 6.5.3 Capture Unit

The capture unit provides a logging function for different events or transitions. The values of the GP timer2 counter and/or GP timer3 counter are captured and stored in the two-level FIFO stacks when selected transitions are detected on capture input pins. The capture unit of the 'C240 consists of four capture circuits.

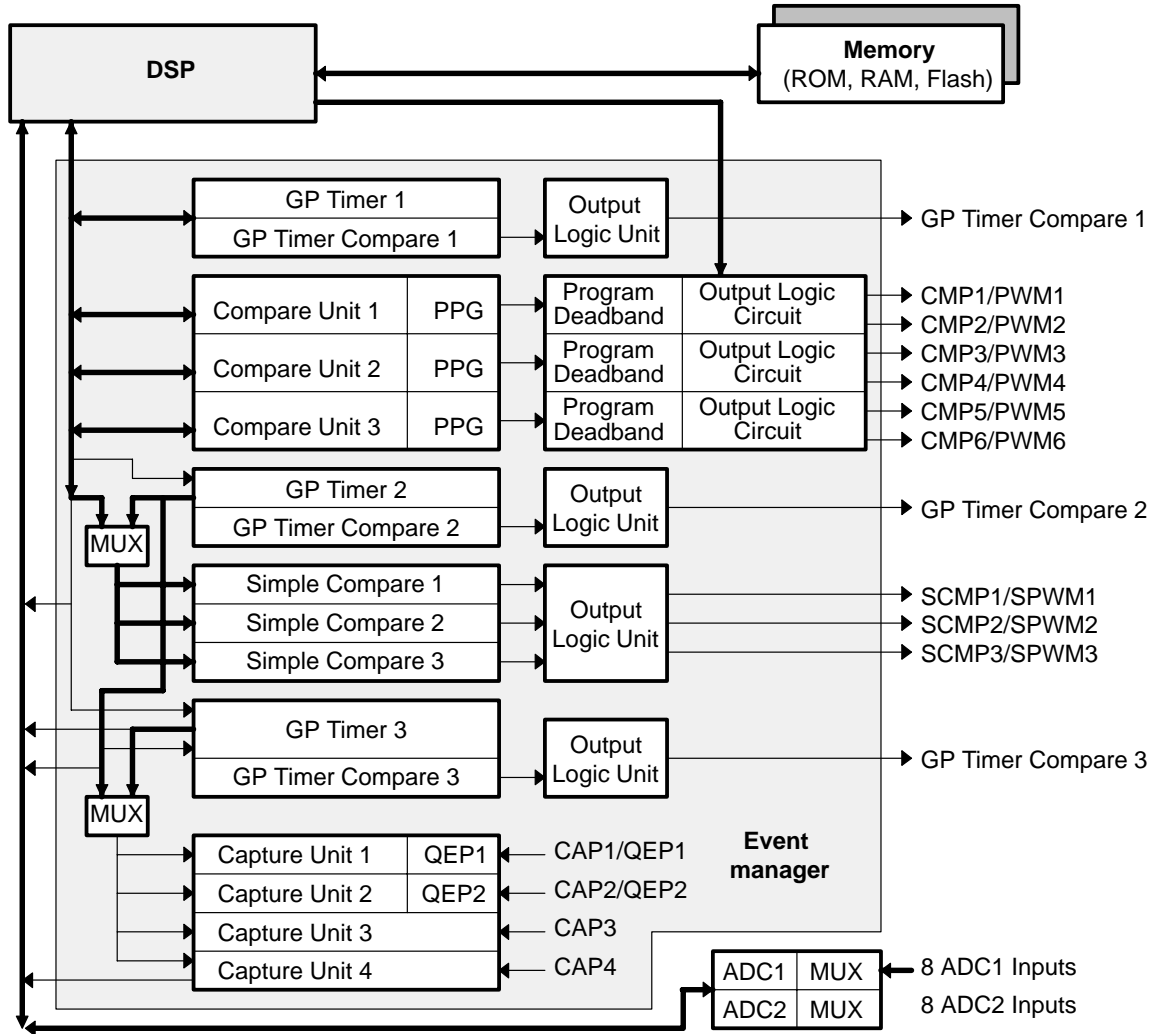
The capture unit includes the following features:

- ☐ One 16-bit capture control register
- ☐ One 16-bit capture FIFO status register
- ☐ Optional selection of GP timer2 and/or GP timer3 through two 16-bit multiplexers (MUXs)
- ☐ Four 16-bit by two FIFO stack registers
- ☐ Four possible Schmitt-triggered capture input pins
- ☐ User-specified edge-detection mode at the input pins
- ☐ Four maskable interrupts/flags

### 6.5.4 Quadrature Encoder Pulse (QEP) Circuit

Two capture inputs can be used to interface the on-chip QEP circuit with the quadrature pulses generated from an optical encoder. Full synchronization of these inputs is done on the chip. Direction or leading quadrature pulse sequence is detected.

Figure 6–4. TMS320C240 Event Manager Block Diagram/Functions



## 6.6 Analog-to Digital-Converter (ADC) Module

The ADC module consists of two 10-bit analog-to-digital converters with two built-in sample and hold circuits. A total of 16 analog input channels are available on the 'C240:

Features of the 'C240 include:

- ☐ Two input channels (one for each ADC unit) can be sampled and converted simultaneously
- ☐ Each ADC unit can perform single or continuous sample/hold and conversion operations.
- ☐ Two 2-level-deep FIFO result registers for ADC units 1 and 2
- ☐ ADC module (both A/D converters) can start operation by software instruction, by external signal transition on a device pin, or by the event manager events on each of the GP timer/compare outputs and the capture 4.
- ☐ The ADC control register is double buffered (with shadow register) and can be written to at any time. A new conversion of ADC can start either immediately or when the previous conversion process is completed according to the control-register bits.
- ☐ At the end of each conversion, an interrupt flag is set and an interrupt is generated if it is unmasked/enabled.
- ☐ The result of previous conversions stored in data register 1 for ADC1, and in data register 2 for ADC2, are lost when new results are generated.

Figure 6–5 shows a block diagram of the 'C240 ADC Module.





## 6.7 Watchdog and Real-Time Interrupt (RTI) Module

The 'C240 device includes a watchdog timer and a real-time interrupt module. The watchdog (WD) function of this module monitors software and hardware operation by generating a system reset if it is not periodically serviced by software, by having the correct key written. The real-time interrupt (RTI) function provides interrupts at programmable intervals. The WD/RTI module features include:

☐ WD timer:

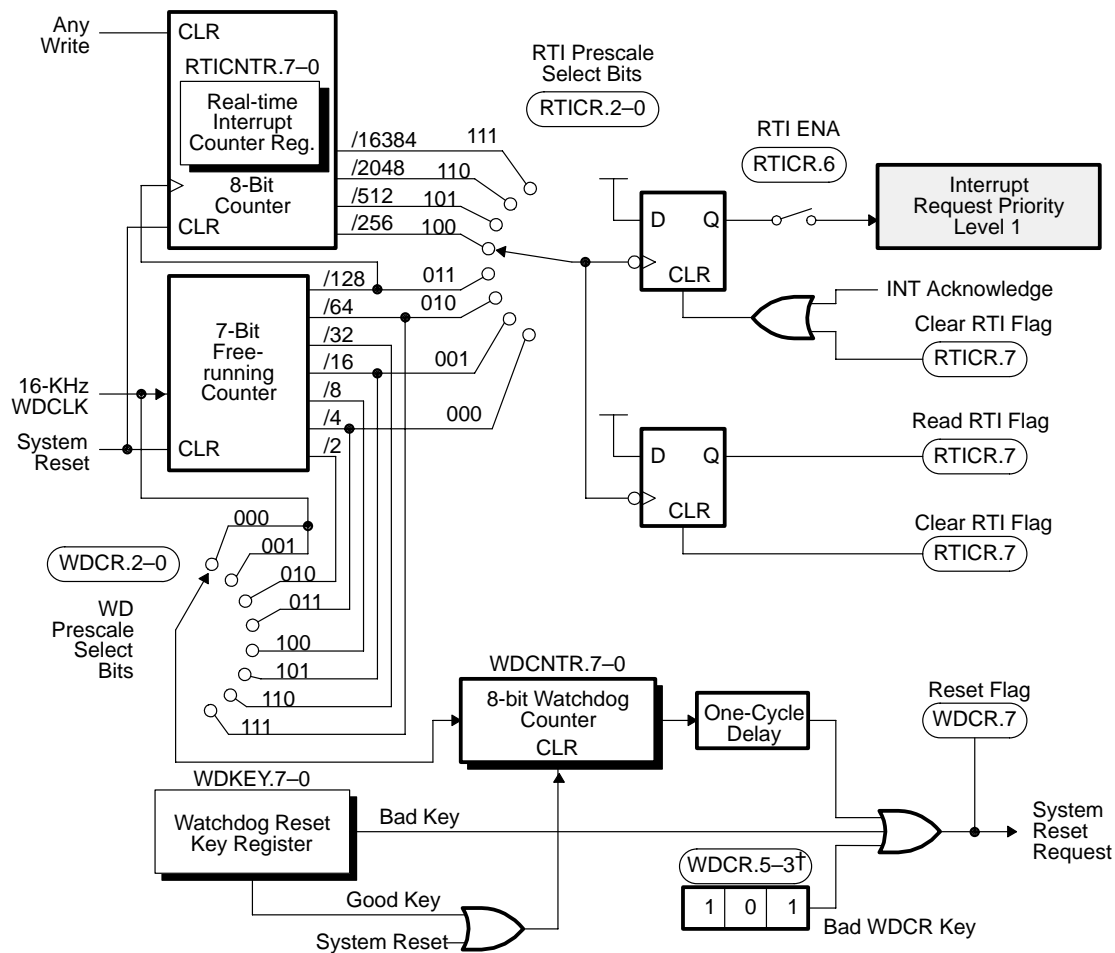
- Seven different WD timer overflow rates ranging from 15.63 ms to 1 s
- A WD reset key (WDKEY) register that clears the WD counter when a correct value is written and generates a system reset if an incorrect value is written to the register
- A WD flag (WDFLAG) that indicates whether the WD timer initiated a system reset
- WD check bits that initiate a system reset if an incorrect value is written to the watchdog-control register (WDCR)
- Automatic activation of the WD timer, once system reset is released
- Three WD control registers located in the control register frame beginning at address 7020h

☐ Real-time interrupt (RTI):

- Interrupt generation at a programmable frequency from 1 to 4096 interrupts per second
- Interrupt or polled operation
- Two RTI control registers located in the control register frame beginning at address 7020h.

Figure 6–6 shows a block diagram of the WD/RTI module.

Figure 6–6. WD/RTI Module Block Diagram



† Writing to bits WDCR.5–3 with anything but the correct pattern (101) generates a system reset.

## 6.8 Serial Peripheral Interface (SPI) Module

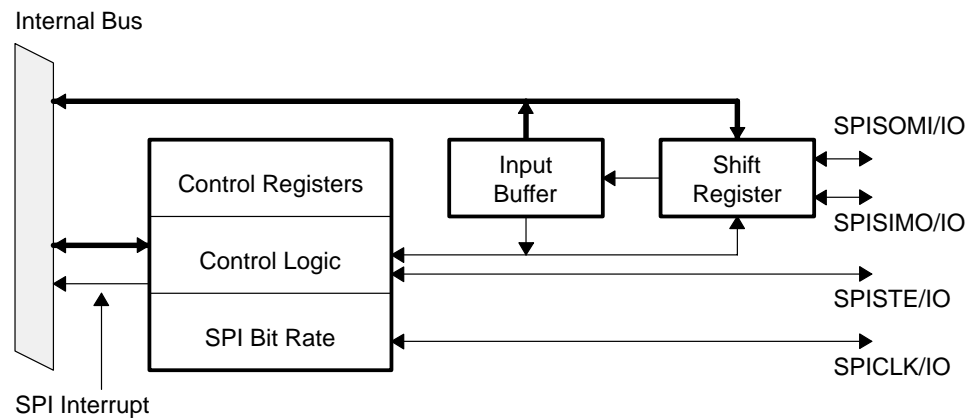
The 'C240 device includes the four-pin SPI module. The SPI is a high-speed, synchronous serial I/O port that allows a serial bit stream of programmed length (one to eight bits) to be shifted into and out of the device at a programmable bit-transfer rate. The SPI normally is used for communications between the microcontroller and external peripherals or another microcontroller. Typical applications include external I/O or peripheral expansion through devices such as shift registers, display drivers, and ADCs. Multidevice communications are supported by the master/slave operation of the SPI. The SPI module features include:

- ☐ Four external pins:
  - SPISOMI: SPI slave output/master input pin, or general-purpose bidirectional I/O pin
  - SPISIMO: SPI slave input/master output pin, or general-purpose bidirectional I/O pin
  - SPISTB: SPI slave enable strobe pin, or general-purpose bidirectional I/O pin
  - SPICLK: SPI serial clock pin, or general-purpose bidirectional I/O pin
- ☐ Two operational modes: master and slave
- ☐ Baud rate: 128 different programmable rates/2.5 Mbps at 10 MHz SYSCLK
- ☐ Data-word format: one to eight data bits
- ☐ Four clocking schemes controlled by the clock polarity and clock phase bits:
  - Falling edge without phase delay: SPICLK inactive high. SPI transmits data on the falling edge of the SPICLK and receives data on the rising edge of the SPICLK signal.
  - Falling edge with phase delay: SPICLK inactive high. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK and receives data on the falling edge of the SPICLK signal.
  - Rising edge without phase delay: SPICLK inactive low. SPI transmits data on the rising edge of the SPICLK and receives data on the falling edge of the SPICLK signal.
  - Rising edge with phase delay: SPICLK inactive low. SPI transmits data one half-cycle ahead of the falling edge of the SPICLK and receives data on the rising edge of the SPICLK signal.

- Simultaneous receive and transmit operation (transmit function can be disabled in software)
- Transmitter and receiver operations are accomplished through either interrupt driven or polled algorithms.
- Ten SPI module control registers located in the control register frame beginning at address 7040h

Figure 6–7 shows a block diagram of the SPI module.

*Figure 6–7. Four-Pin Serial Peripheral Interface (SPI) Module Block Diagram*



## 6.9 Serial Communications Interface (SCI) Module

The 'C240 device includes an SCI module. The SCI module supports digital communications between the CPU and other asynchronous peripherals that use the standard NRZ format. The SCI's receiver and transmitter are double-buffered and each has its own separate enable and interrupt bits. Both may be operated independently or simultaneously in the full-duplex mode. To ensure data integrity, the SCI checks received data for break detection, parity, overrun, and framing errors. The speed of bit rate (baud) is programmable to over 65,000 different speeds through a 16-bit baud-select register.

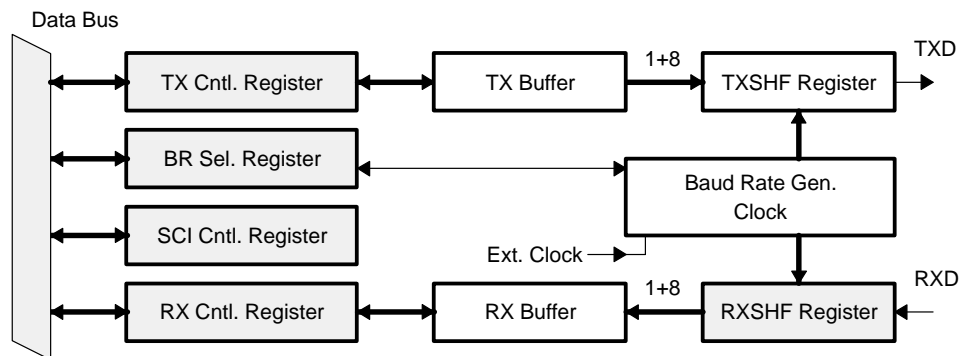
Features of the SCI module include:

- ☐ Three external pins:
  - SCITXD: SCI transmit output pin or general-purpose bidirectional I/O pin
  - SCIRXD: SCI receive input pin or general-purpose bidirectional I/O pin
  - SCICLK: SCI bidirectional serial clock pin or general-purpose bidirectional I/O pin
- ☐ Two communications modes: asynchronous and isosynchronous
- ☐ Baud rate: 64K different programmable rates
  - Asynchronous mode: 312 Kbps at 10-MHz SYSCLK
  - Isosynchronous mode: 5 Mbps at 10-MHz SYSCLK
- ☐ Data word format:
  - One start bit
  - Data word length programmable from one to eight bits
  - Optional even/odd/no parity bit
  - One or two stop bits
- ☐ Four error-detection flags: parity, overrun, framing, and break-detection
- ☐ Two wake-up multiprocessor modes: idle-line and address bit
- ☐ Half- or full-duplex operation
- ☐ Double-buffered receive and transmit functions

- Transmitter and receiver operations can be accomplished through either interrupt-driven or polled algorithms with status flags:
  - Transmitter: TXRDY flag (transmitter buffer register is ready to receive another character) and TX EMPTY flag (transmitter shift register is empty)
  - Receiver: RXRDY flag (receive buffer register ready to receive another character), BRKDT flag (break condition occurred), and RX ERROR (monitoring four interrupt conditions)
  - Separate enable bits for transmitter and receiver interrupts (except BRKDT)
  - Non-return-to-zero (NRZ) format
  - Twelve SCI module control registers located in the control register frame beginning at address 7050h

Figure 6–8 shows the SCI module block diagram.

Figure 6–8. TMS320C24x Serial Communication Interface (SCI)



## 6.10 Tools for TMS320C24x

For information about the code generation and debugging tools available for the 'C24x devices, refer to Chapter 15, *Code Generation Tools*, and Chapter 16, *System Integration and Debugging Tools*. Table 2–14 and Table 2–15 in Chapter 2, *Selection Guide*, provide part numbers and host system information.



# TMS320C3x Devices

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The TMS320C3x generation is the first of TI's floating-point digital signal processors. The 'C3x devices provide an easy-to-use, high-performance architecture, which allows users to develop breakthrough products quickly.

'C3x devices can be used in a wide variety of areas including automotive applications, digital audio, industrial automation and control, data communications, and office equipment such as multifunction peripherals, copiers, and laser printers.

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## 7.1 TMS320C3x Introduction

The 'C3x has a von Neumann architecture, which provides a unified data and program space. To further enhance performance, the 'C3x devices have four internal data buses and at least one external data bus. The base architecture is enhanced with numerous on-chip peripherals.

The CPU has an independent multiplier and ALU to offer up to 60 million floating-point operations per second (MFLOPS) and up to 30 MIPS.

The DMA controller has its own data bus and operates in parallel with the CPU. The DMA controller is programmed to input and output data sets, freeing the CPU for arithmetic operations. The DMA controller can reach anywhere in the memory map, including on-chip, off-chip, and memory-mapped peripheral registers.

The total memory space of the 'C3x is 16M 32-bit words. Having the data, program, and I/O space contained in this 16M word address range maximizes memory usage and allows you to allocate the memory space as desired. Both 1K-word, 32-bit RAM blocks can support two CPU accesses in a single cycle. The separate program, data, and DMA buses allow parallel program fetches, data reads/writes, and DMA operations. To maintain high performance when using slower external memory, the 'C3x contains a 64-word on-chip cache.

Development tools available from TI for the 'C3x family include the software simulator, C compiler/linker/assembler, hardware emulator, evaluation module, and a DSP Starter Kit. Additionally, there are hundreds of software algorithms and scores of application and development tools available through TI's extensive third-party network.

## 7.2 TMS320C3x Key Features

Key features of the 'C3x generation are listed in paragraphs that follow. When only certain devices have a particular feature, they are named in parentheses following the feature's description.

### □ CPU

- 33-ns single-cycle instruction execution time with 60-MHz clock on all devices ('C31, 'C32)
  - 60-MHz clock
  - 60 MFLOPS
  - 30 MIPS
- 40-ns single-cycle instruction execution time with 50-MHz clock on all devices
  - 50-MHz clock
  - 50 MFLOPS
  - 25 MIPS
- 50-ns single-cycle instruction execution time
  - 40-MHz clock
  - 40 MFLOPS
  - 20 MIPS
- 60-ns single-cycle instruction execution time ('C30, 'C31)
  - 33-MHz clock
  - 33.3 MFLOPS
  - 16.7 MIPS
- 32-bit instruction words, 32-bit data words, and 24-bit addresses
- 24/32-bit integer, 32/40-bit floating-point, and 32-bit logical operations
- Two- and three-operand instructions
- Parallel ALU and multiplier instructions in a single cycle
- Block repeat capability
- Zero-overhead loops and single-cycle branches
- Conditional calls and returns
- Interlocked instructions for multiprocessing support
- Two address generators with eight auxiliary registers and two auxiliary register arithmetic units
- Eight 40-bit, extended-precision registers
- 32-bit barrel shifter

- ☐ **Peripherals**
  - On-chip memory-mapped DMA controller for concurrent CPU and I/O operations
  - Two channels configurable priority ('C32)
  - Memory-mapped serial ports to support 8-, 16-, 24-, or 32-bit full-duplex transfers
    - One serial port ('C31/C32)
    - Two serial ports ('C30)
  - Two memory-mapped 32-bit timers
  - Two general-purpose external flags and four external interrupts
  - Scan logic for test and evaluation
- ☐ **Memory**
  - 64 × 32-bit instruction cache
  - One 4K 32-bit-word single-cycle dual-access on-chip ROM block ('C30)
  - Two 1K 32-bit-word single-cycle dual-access on-chip RAM blocks ('C30/C31)
  - Two 256 32-bit-word RAM blocks ('C32)
  - 16M word addressing space
  - Preprogrammed bootloader ('C31/C32)
- ☐ **Memory interfaces**
  - Two memory/I/O expansion buses ('C30)
  - One external memory bus ('C31/C32)
  - Flexible 8-, 16-, or 32-bit data size in 8-, 16-, or 32-bit memory ('C32)
- ☐ **Low power (3.3 V) ('C31/C32) with two power-down modes: 2-MHz operation and idle**
- ☐ **CMOS technology**
- ☐ **Packages**
  - 181-pin PGA ('C30)
  - 208-pin PQFP ('C30)
  - 132-pin PQFP ('C31/LC31)
  - 144-pin PQFP/TQFP ('C32)

### 7.3 TMS320C3x CPU

The TMS320 CPU has an independent multiplier and accumulator and achieves up to 60 MFLOPS. Results are stored in any one of eight extended-precision registers. These are 40-bit registers that store values with a 32-bit mantissa and an 8-bit exponent. These registers can serve as both the source and destination for any arithmetic operation. The extended-precision registers are an extremely valuable resource for programming in assembly or C. These registers allow you to maintain intermediate results without storing data in memory. This results in higher-performance assembly code and a more efficient C compiler.

To sustain 60 MFLOPS, the CPU has two independent auxiliary register arithmetic units (ARAUs). The two ARAUs generate 24-bit addresses that are accessed through the eight auxiliary registers. The ARAUs can perform any of these functions:

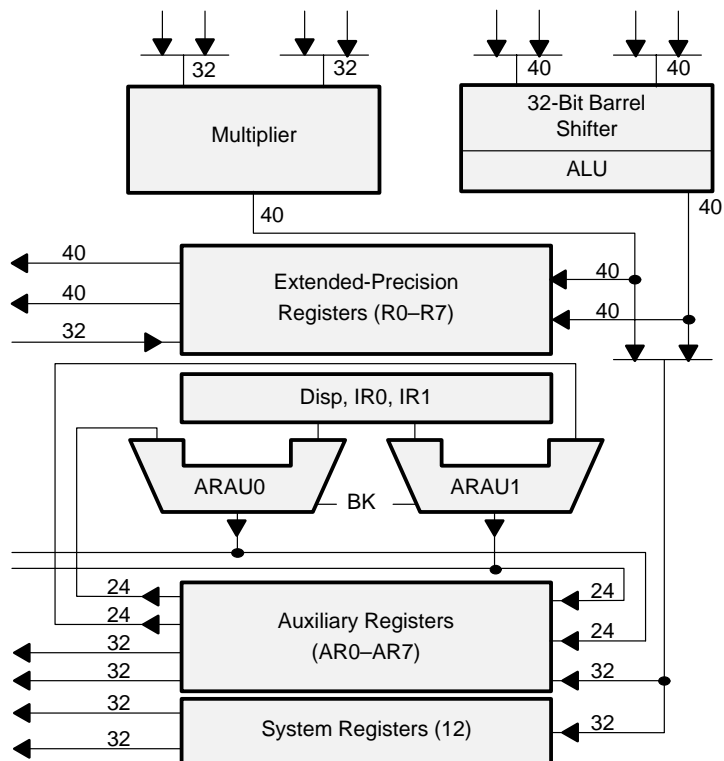
- ☐ Pre- or post-increment or decrement
- ☐ Index offset for increment and decrement values other than 1
- ☐ Circular addressing to support circular buffers
- ☐ Bit-reversed addressing for FFTs

Features of the TMS320C3x CPU include:

- ☐ 60-MFLOP CPU
- ☐ Register-based CPU
- ☐ 32 or 40 floating-point/integer multiplier
- ☐ 32 or 40 floating-point/integer ALU
- ☐ 32-bit barrel shifter
- ☐ Eight 40-bit extended-precision registers
- ☐ Two address generators
- ☐ Two index registers
- ☐ Eight indirect-address registers

Figure 7–1 shows a block diagram of the 'C3x CPU.

Figure 7–1. TMS320C3x CPU



## 7.4 TMS320C3x Memory

To realize the full performance of the 'C3x CPU, it is important to have a bus and memory architecture that can keep pace. The 'C3x fetches up to four words per cycle. These consist of a program opcode, two CPU data operands, and a DMA data transfer. The internal buses can transfer all four words in parallel, relying on seven memory sources for data.

The 'C3x uses seven internal buses to access on-chip resources:

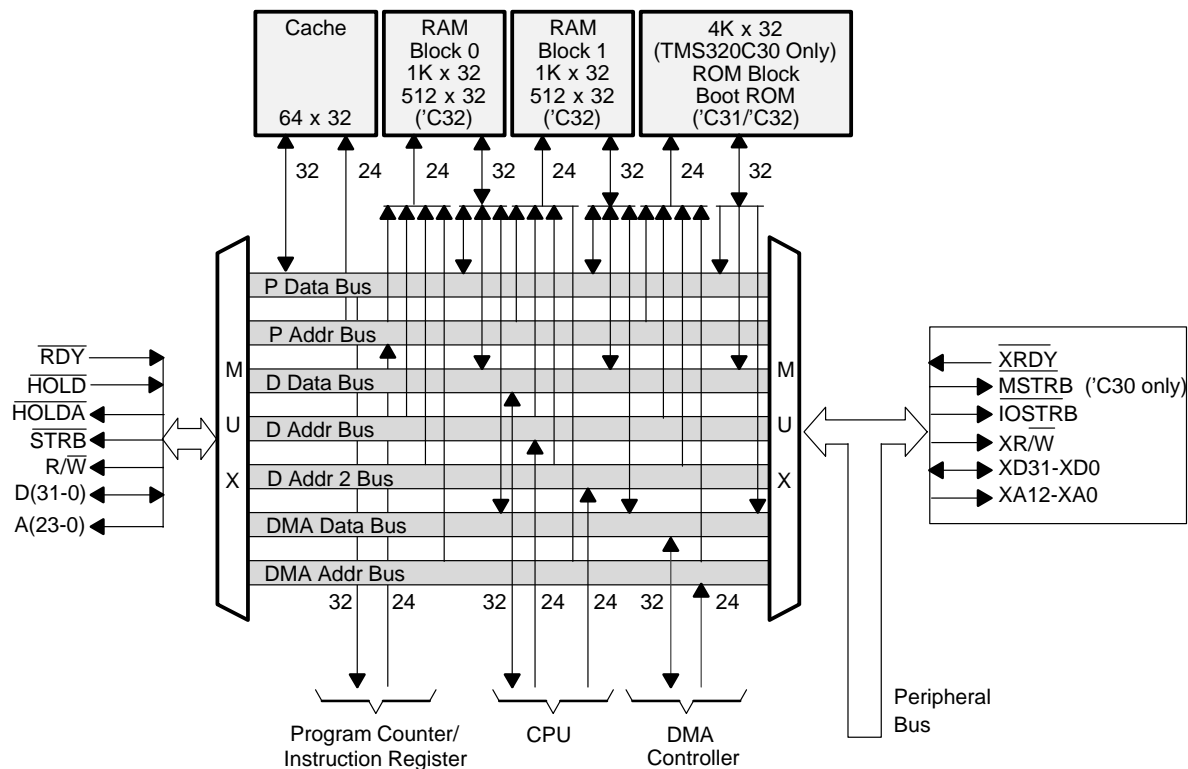
- ☐ Program address/data: The CPU uses these buses to maintain instruction fetches every cycle.
- ☐ Data address/data: In any cycle, the CPU can fetch two data operands, because it has two data address buses and one data bus that can be accessed twice in a single cycle.
- ☐ DMA address/data: The DMA uses these buses to perform DMA transfers in parallel with CPU operation.

With the internal buses in place to feed the DMA and CPU, the 'C3x devices can use both internal and external data and program memory. The 'C30 and 'C31 have two 1K 32-bit word blocks of dual-access RAM, while the 'C32 has two 256 32-bit words of on-chip RAM. This memory provides up to four words of program or data in a single cycle. All 'C3x devices feature an on-chip cache to boost system performance. The primary bus for each device has 16M words of address reach. The 'C30 features an expansion bus that has an 8K-word address reach, which is often used to interface to peripherals.

The 'C32 offers the ability to access 8-, 16-, and 32-bit data stored in 8-, 16-, and 32-bit wide external memory giving the flexibility of nine memory interface options. This feature can significantly affect total system cost savings. Additionally, the 'C32 memory interface allows for storage of the 32-bit instruction word in either 16- or 32-bit-wide external memory.

Figure 7–2 shows a block diagram of the 'C3x memory.

Figure 7-2. TMS320C3x Memory





## 7.5 TMS320C3x DMA Controller

The DMA controller transfers data between memory resources. The serial ports and timers on the 'C3x are memory-mapped, allowing DMA transfers to and from these peripherals. To perform a transfer, the DMA reads a memory location pointed to by the source address register and then writes to the memory location pointed to by the destination address register. The source and destination addresses are incremented or decremented after each transfer, depending on the value of the global control register. The DMA controller performs continuous transfers over the DMA bus until the value in the transfer counter register reaches 0, and a programmable interrupt is sent to the CPU.

For example, an application might use the DMA to transfer 512 words from slow external memory to the on-chip RAM. At the completion of the transfer, an interrupt is sent to the CPU to process and output results while the DMA transfers a new set of 512 words to on-chip RAM. By off-loading data input, the DMA controller allows sustained CPU performance for arithmetic calculations. In this case, the CPU always has zero-wait-state access to data, even though the external memory requires one or more wait states.

The 'C32 offers the programmer the flexibility of designating priority on the bus. There are three options:

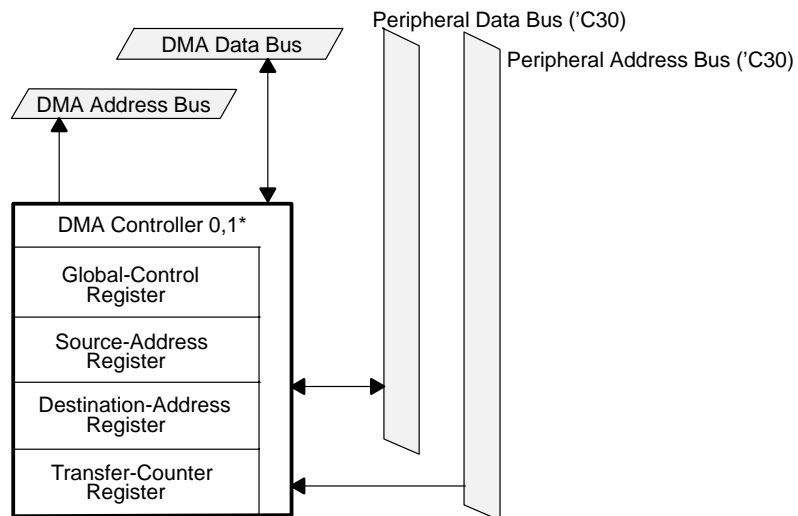
- 1) The CPU has priority over the DMA at all times ('C30 and 'C31).
- 2) The DMA controller has priority over the CPU.
- 3) The CPU and DMA share a rotating priority with the CPU having first access.

Features of the DMA controller include:

- ☐ Increased CPU-sustained performance by virtually eliminating CPU I/O
- ☐ Memory-to-memory transfers
- ☐ Two-channel configurable priority ('C32 only)
- ☐ Programmable increment or decrement of addresses

Figure 7–3 shows a block diagram of the DMA controller.

Figure 7–3. TMS320C3x DMA Controller



\* DMA1 is available only on the 'C32

## 7.6 TMS320C3x Sum of Products Example

The following code for a sum of products is typical of DSP algorithms and demonstrates the power of the 'C3x architecture. First, note that the repeat single instruction (RPTS) is used for a zero-overhead loop. The parallel bars next to the ADDF instruction indicate that the addition is executed in parallel with the multiplication. Auxiliary registers 0 and 1 are used to fetch the two data operands with a post-increment of one. The multiplier results are placed in one of the eight extended-precision registers. The extended-precision register set is further used as the input and output for the addition. Finally, the DMA can transfer the next set of data for the CPU to process in parallel with the multiply and accumulate. All of these operations take place in a single cycle, illustrating the parallelism in the 'C3x architecture.

Figure 7–4 shows an example of a sum of products function.

Figure 7–4. TMS320C3x Sum of Products Example

$$y = a1 * x1 + a2 * x2 + \dots + an * xn$$

```

MPY    *AR0++, *AR1++, R0
MPY    *AR0++, *AR1++, R2

RPTS   n-3
MPYF   *AR0++, *AR1++, R0
| | ADDF  R0 , R2 , R2

ADDF   R0 , R2

```

## 7.7 TMS320C30

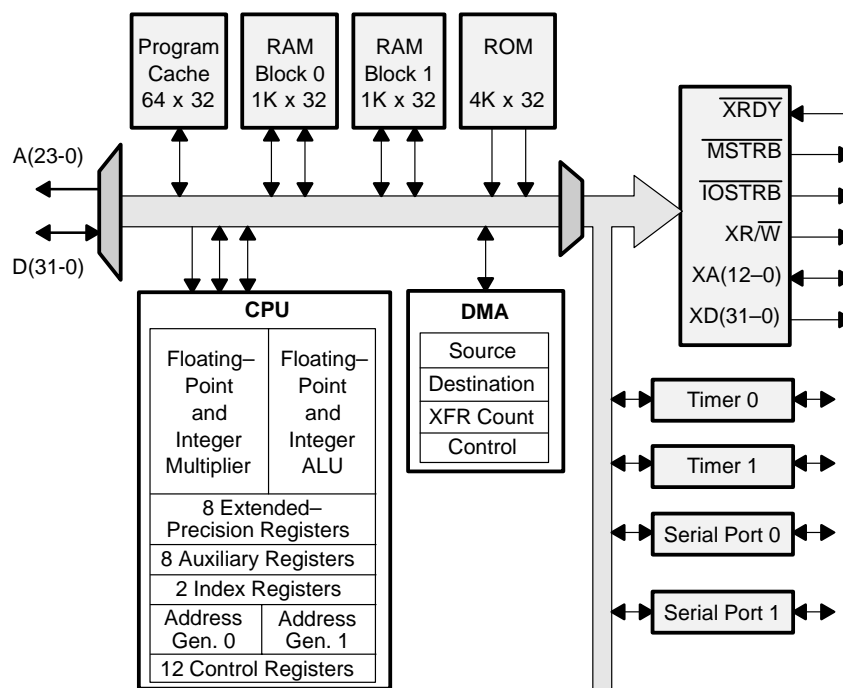
The 'C30 features a second external data bus, two timers, and two serial ports. The expansion bus has a 13-bit address bus and a 32-bit data bus. Each serial port has independent double-buffered transmit and receive sections with a maximum data rate of 15 Mbps with a 60-MHz input clock.

Features of the TMS320C30 include:

- ☐ 40-, 50-, and 60-ns instruction cycle times
- ☐ 16M-word external-address reach
- ☐ Single-cycle multiply and accumulate (MAC) operation
- ☐ Two serial ports
- ☐ Two timers
- ☐ 4K-words on-chip ROM
- ☐ Optimizing ANSI C compiler
- ☐ On-chip DMA
- ☐ Packaging:
  - ☒ 181-pin PGA
  - ☒ 208-pin PQFP

Figure 7–5 shows a block diagram of the 'C30.

Figure 7–5. TMS320C30 Block Diagram



## 7.8 TMS320C31

The 'C31 is the second member of the 'C3x generation and is object-code compatible with the 'C30. The 'C31 has the same fast CPU as all other members of the 'C3x generation, but offers a different mix of peripherals to achieve a unique price/performance point.

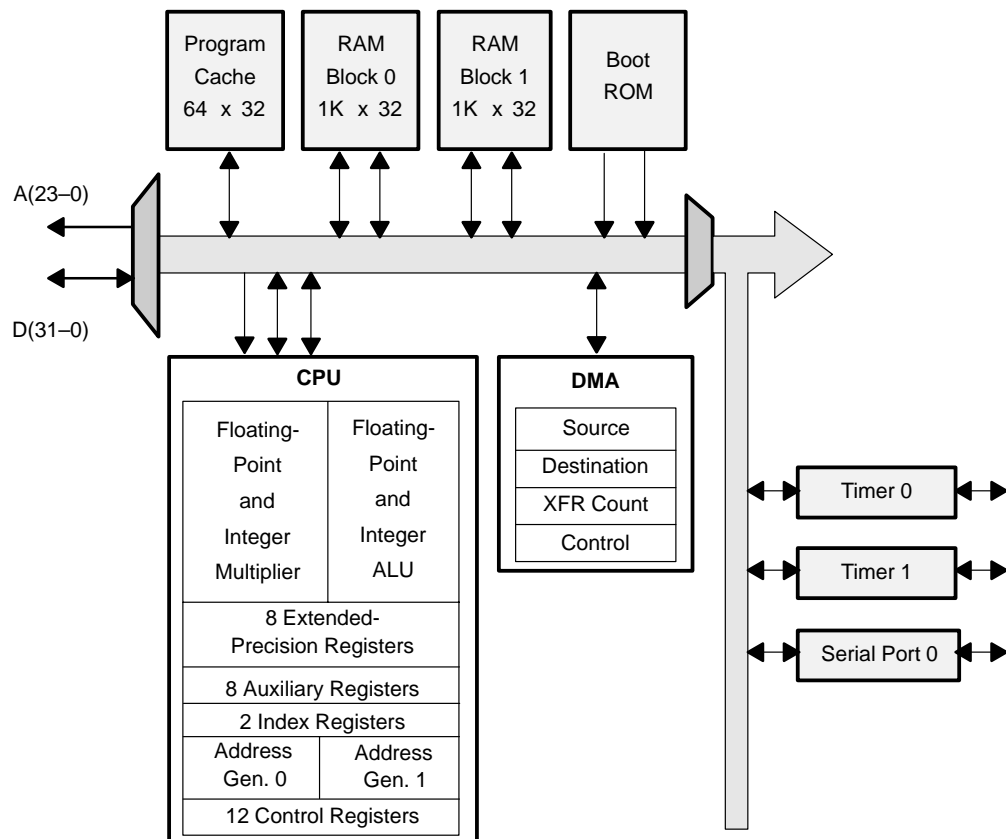
The 'C31 offers a lower cost than the 'C30 by removing the expansion bus and one of the serial ports and replacing the 4K 32-bit words of internal ROM with a boot ROM. A low-power version of the 'C31 is available at 33 or 40 MHz at 3.3 V, which significantly reduces power consumption. The 'C31 comes in a 132-pin PQFP.

The TMS320C31 features:

- ☐ 33-, 40-, 50-, and 60-ns instruction cycle times
- ☐ 16M word external address reach
- ☐ Single-cycle multiply and accumulate (MAC) operation
- ☐ Optimizing ANSI C compiler
- ☐ On-chip DMA
- ☐ Boot ROM
- ☐ 3.3-V version up to 40 MHz
- ☐ Two low-power modes
- ☐ Two 32-bit timers
- ☐ Serial port
- ☐ 64-word cache
- ☐ 132-pin PQFP

Figure 7–6 shows a block diagram of the 'C31.

Figure 7–6. TMS320C31 Block Diagram



## 7.9 TMS320C32

The 'C32 is the lowest-cost floating-point device TI offers. The 'C32 is object-code compatible with the 'C30 and 'C31. The 'C32 has a flexible memory interface that supports 8-, 16-, or 32-bit data types in 8-, 16-, or 32-bit memory. Additionally, it supports program storage in 16- or 32-bit memory. This can lead to considerable savings in system cost.

There are also two low-power modes on the 'C32. One reduces the clock rate of the device but continues execution, while the other suspends instruction execution and puts the device on hold. These are valuable features in power-critical applications.

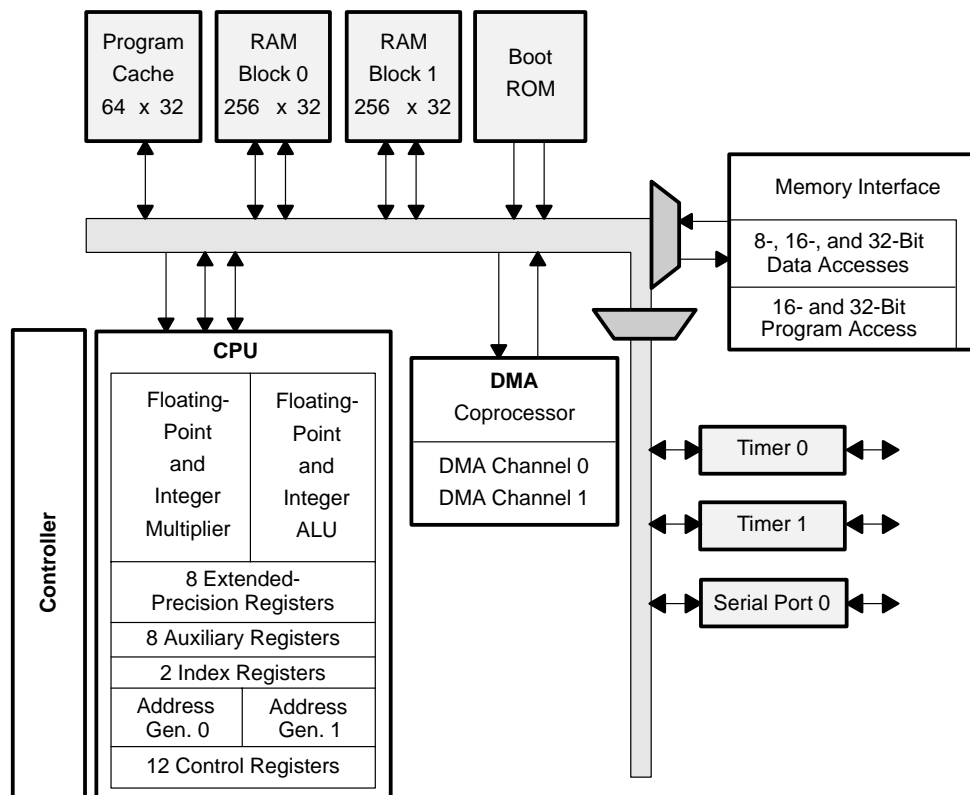
The 'C32 features the same boot ROM as the 'C31, has two 256-word, 32-bit blocks of on-chip RAM, and comes in a 144-pin PQFP or TQFP.

Features of the TMS320C32 include:

- ☐ 33-, 40-, and 50-ns instruction cycle times
- ☐ Object-code compatibility with the 'C30/C31
- ☐ 16M-word external-address reach
- ☐ Flexible memory interface (8, 16, or 32 bits)
- ☐ Two-channel DMA with configurable priorities
- ☐ Low-power modes
- ☐ 64-word program cache
- ☐ Two 32-bit timers
- ☐ 144-pin PQFP or TQFP

Figure 7–7 shows a block diagram of the 'C32.

Figure 7–7. TMS320C32 Block Diagram





## 7.10 Tools for TMS320C3x

For information about the code generation and debugging tools available for the 'C3x devices, refer to Chapter 15, *Code Generation Tools*, and Chapter 16, *System Integration and Debugging Tools*. Table 2–14 and Table 2–15 in Chapter 2, *Selection Guide*, provide part numbers and host system information.

# TMS320C4x Devices

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The TMS320C4x devices are 32-bit floating-point DSPs optimized for parallel processing. The 'C4x family combines a high-performance CPU and DMA controller with up to six communication ports to meet the needs of multiprocessor and I/O-intensive applications.

Key applications of the 'C4x family include three-dimensional graphics, image processing, networking, and telecommunications base stations.

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## 8.1 TMS320C4x Introduction

All 'C4x devices are compatible with TI's multichip development environment. Each device contains an on-chip analysis module which supports hardware breakpoints for parallel-processing development and debugging. The 'C4x family accepts source code from the TMS320C3x family of floating-point DSPs.

## 8.2 TMS320C4x Key Features

Key features of the TMS320C4x generation are as follows.

- ☐ Up to 30-MIPS and 60-MFLOPS performance with 384 Mbytes/s of I/O capability
  - IEEE floating-point conversion for ease of use
  - Register-based CPU
  - Single-cycle byte and half-word manipulation capabilities
  - Divide and square root support for improved performance
- ☐ On-chip memory includes 2K words of RAM, 128 words of program cache, and a bootloader
- ☐ Two external buses providing an address reach of up to 4G words
- ☐ Two memory-mapped 32-bit timers
- ☐ 6- and 12-channel DMA
- ☐ Up to six communication ports for multiprocessor communication
- ☐ Idle mode for reduced power consumption
- ☐ Optimizing ANSI C compiler

### 8.3 TMS320C4x CPU

The 'C4x has an independent multiplier and accumulator and achieves up to 60 MFLOPS. Results are stored in any one of 12 extended-precision registers. These are 40-bit registers that store values with a 32-bit mantissa and an 8-bit exponent. These registers can serve as both the source and destination for any arithmetic operation. The extended-precision registers are an extremely valuable resource for programming in assembly or C. These registers allow maintenance of intermediate results without storing data in memory. This results in higher performance assembly code and a more efficient C compiler.

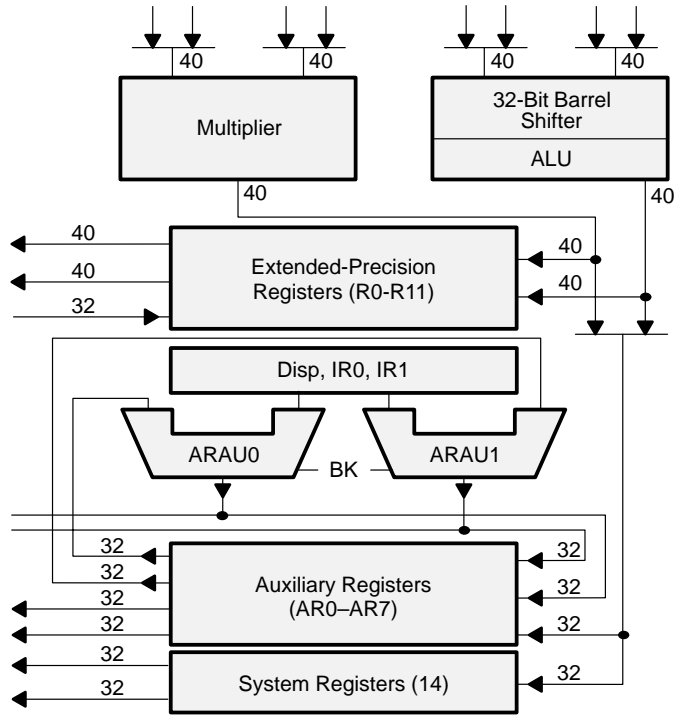
To sustain 60 MFLOPS, the CPU has two independent auxiliary register arithmetic units (ARAUs), which can generate two addresses in a single cycle. The two ARAUs operate in parallel with the multiplier and ALU. They support addressing with displacements, addressing with index registers (IR0 and IR1), circular addressing, and bit-reversed addressing.

Features of the 'C4x CPU are:

- ☐ High-speed internal parallelism: eight operations per cycle for maximum sustained performance
  - Floating-point/integer multiply
  - Floating-point/integer addition
  - Two data accesses
  - Zero-overhead branch and loop counter update
- ☐ IEEE floating-point conversion
- ☐ Divide and square root support for improved performance
- ☐ Single-cycle byte and halfword manipulation capabilities
- ☐ Register-based CPU

Figure 8–1 shows a block diagram of the 'C4x CPU.

Figure 8–1. TMS320C4x CPU



## 8.4 TMS320C4x Memory and Bus Structure

To realize the full performance of the 'C4x CPU, it is important to have a bus and memory architecture that can keep pace. The 'C4x fetches up to four 32-bit words each cycle: a program opcode, two CPU data operands, and a DMA data transfer. The internal buses can transfer all four words in parallel, relying on seven memory sources for data.

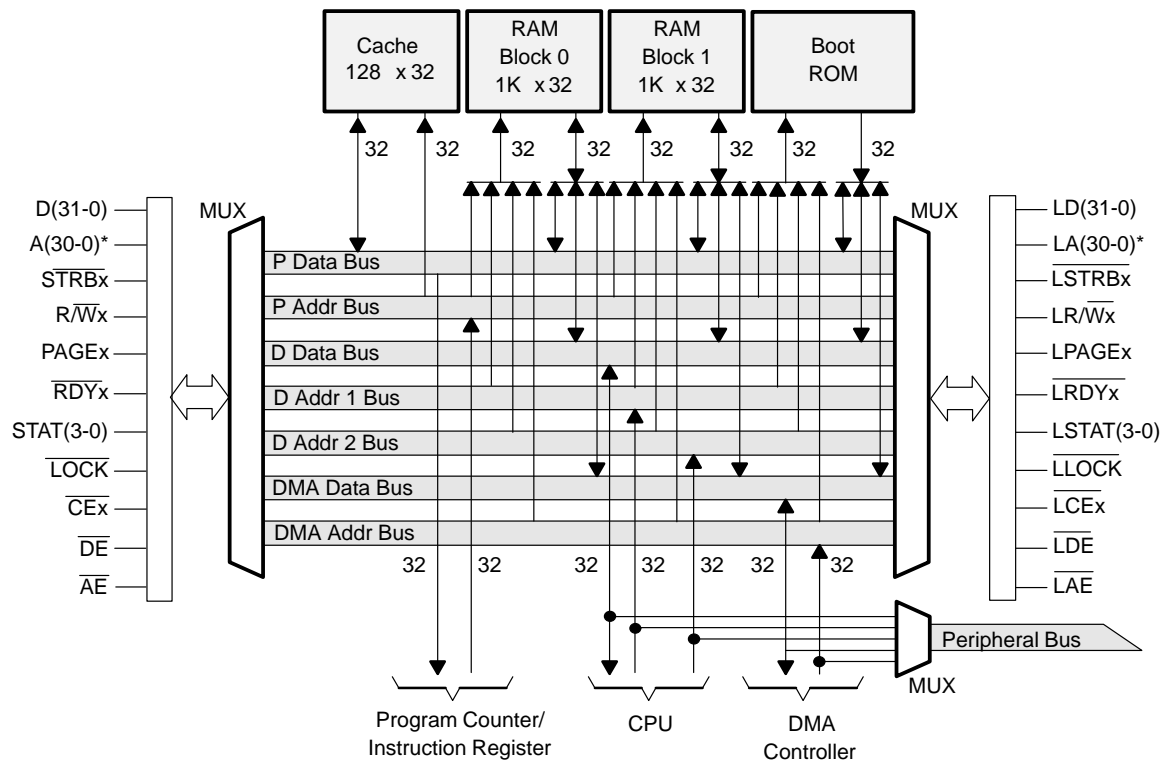
The 'C4x uses seven internal buses to access on-chip resources.

- ☐ Program address/data: The CPU uses these buses to maintain instruction fetches every cycle.
- ☐ Data address/data: In any cycle, the CPU can fetch two data operands, because it has two data address buses and one data bus that can be accessed twice in a single cycle.
- ☐ DMA address/data: The DMA uses these buses to perform DMA transfers in parallel with CPU operation.

With the internal buses in place to feed the DMA and CPU, the 'C4x devices can use both internal and external data and program memory. Internally, the 'C4x has two 1K by 32-bit-word blocks of dual-access RAM, providing up to four words of program or data in a single cycle. For external memory, the 'C40 has two identical 32-bit buses, which address up to 2G words of memory each. The 'C44 has two 24-bit external address buses, which address up to 16M words each. Each device has an on-chip instruction cache to boost performance when using slower external memory.

Figure 8–2 shows a block diagram of the 'C4x memory and bus structure.

Figure 8–2. TMS320C4x Memory and Bus Structure



\* 24-bit address bus in TMS320C44

## 8.5 TMS320C4x Communication Ports

The communication ports on the 'C4x generation transfer up to 24 Mbytes/s each for asynchronous interprocessor communications or for servicing intensive I/O needs. The 'C40 has six ports, and the 'C44 has four. Each port has four control pins and eight data pins. These 12 pins provide a glueless interface to another 'C4x. The control pins combined with the control logic arbitrate with another device to determine data transfer timing and direction. Because the communication ports have built-in arbitration and control circuitry, you simply need to read data from and write data to the memory-mapped input and output FIFOs.

In a typical transfer, the DMA coprocessor or the CPU first writes to the output FIFO. Next, the communication port sends a request signal to the destination processor, which responds with an acknowledge. The communication port then transfers the word as four successive bytes. The destination processor receives the word in its input FIFO, where the destination DMA or CPU can read the contents. Note that the input and output FIFOs provide a 16-word x 32-bit buffer between the communication ports.

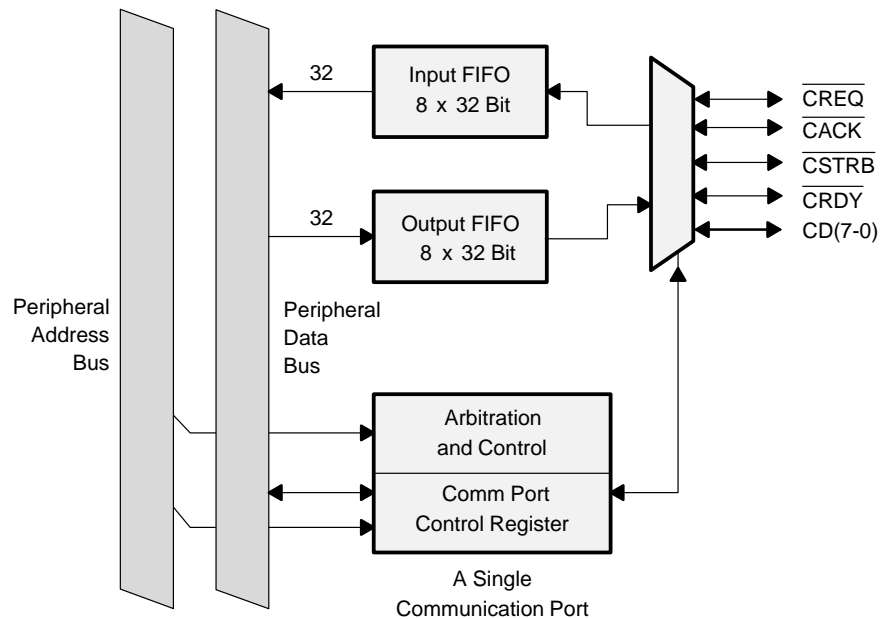
Features of the 'C4x communication ports include:

- ☐ Up to 24 Mbytes/s bidirectional interface on each communication port for high-speed and low-cost parallel-processor interface
- ☐ Eight-word-deep input FIFO and eight-word-deep output FIFO buffer
- ☐ Automatic arbitration and handshaking for direct processor-to-processor connection

Figure 8–3 shows a block diagram of the 'C4x communication ports.



Figure 8–3. TMS320C4x Communication Ports



## 8.6 TMS320C4x DMA Coprocessor

With as many as six communication ports and two external buses, the 'C4x has an I/O capability or as much as 384 Mbytes/s. To service this tremendous speed, the 'C4x has a 6- or 12-channel DMA. The DMA operates independently of the CPU and has dedicated address and data buses to avoid bus conflicts.

The DMA is programmed to transfer data from any memory location to any other memory location (communication ports are memory-mapped). The DMA can begin a task based on CPU or external interrupts and can interrupt the CPU at the completion of a task. The DMA also includes a link pointer register that allows the DMA to program its next task without CPU intervention.

Since each communication port has transmit and receive capability, 12 DMA channels are needed if all six communication ports are being used in a bidirectional mode. The DMA has a split-mode operation dedicated to this function, allowing the DMA to service the 12 input and output FIFOs in the communication ports.

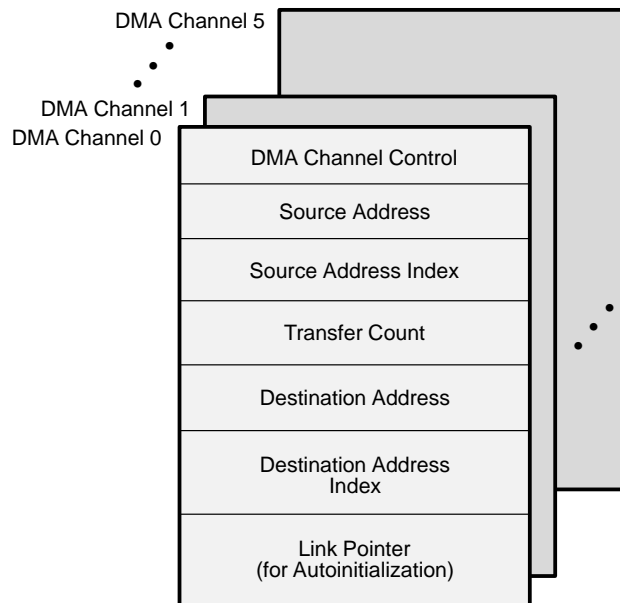
In the event that both the CPU and DMA are accessing the same resource, priorities can be assigned to resolve the conflict. Priority can be assigned to the CPU, the DMA, or mixed, where the CPU gets the first access followed by the DMA.

The 'C4x DMA coprocessor features:

- ☐ Concurrent I/O to maximize sustained CPU performance
- ☐ Autoinitialization
- ☐ Up to 6 or 12 DMA channels for parallel data transfers
  - Data transfers to and from anywhere in memory
  - Three operations per cycle
    - 32-bit data transfer
    - Address register update
    - Transfer counter update
  - Performance of 90 MOPS

Figure 8–4 shows a block diagram of the 'C4x DMA coprocessor.

Figure 8–4. TMS320C4x DMA Coprocessor



## 8.7 TMS320C40

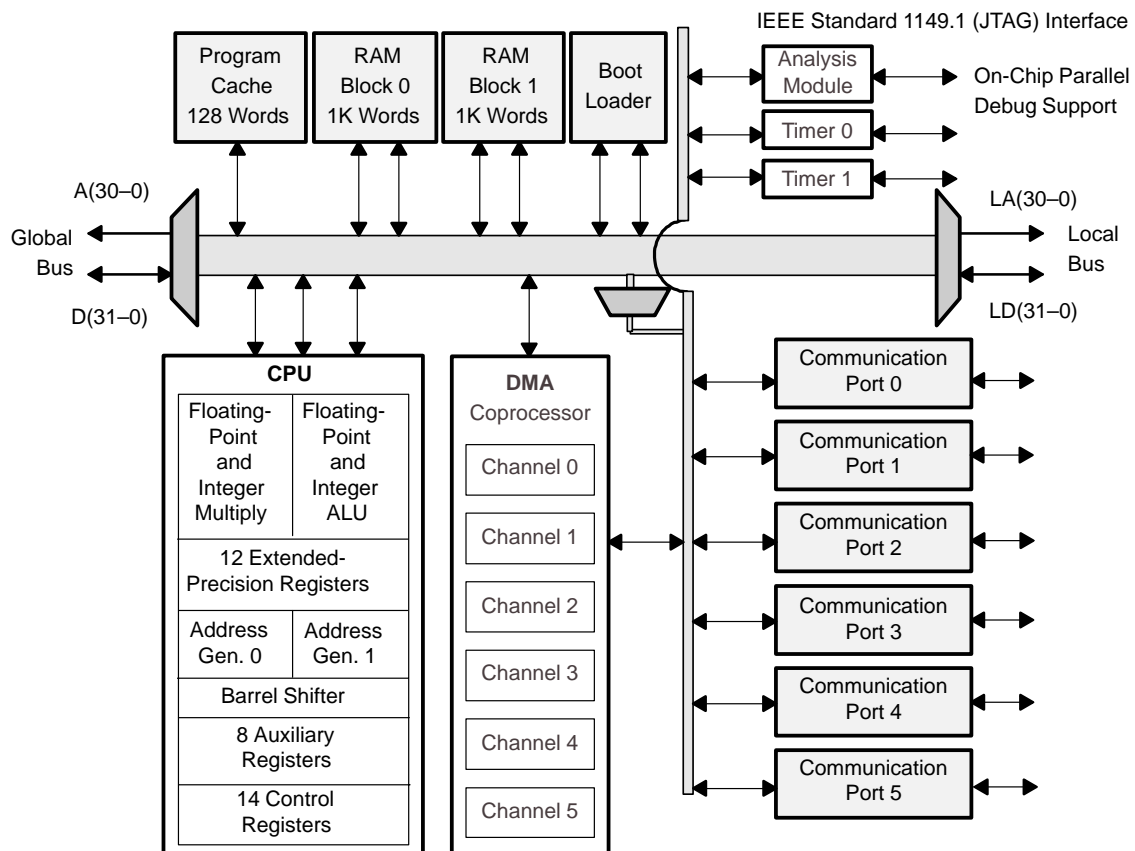
The 'C40 is the original member of the 'C4x family. It features a CPU that can deliver up to 30 MIPS and 60 MFLOPS with a maximum I/O bandwidth of 384 Mbytes/s. The 'C40 has 2K words of on-chip RAM, 128 words of program cache, and a bootloader. Two external buses provide an address reach of 4G of unified memory space. The 'C40 is available in a 325-pin PGA.

Features of the 'C40 include:

- ☐ 33-, 40-, and 50-ns instruction cycle times
- ☐ 4G-word external address reach
- ☐ Optimizing ANSI C compiler
- ☐ IEEE floating-point conversion for ease of use
- ☐ 6- or 12-channel on-chip DMA
- ☐ Six communication ports
- ☐ Accepts source code from 'C3x

Figure 8–5 shows a block diagram of the 'C40.

Figure 8–5. TMS320C40 Block Diagram



## 8.8 TMS320C44

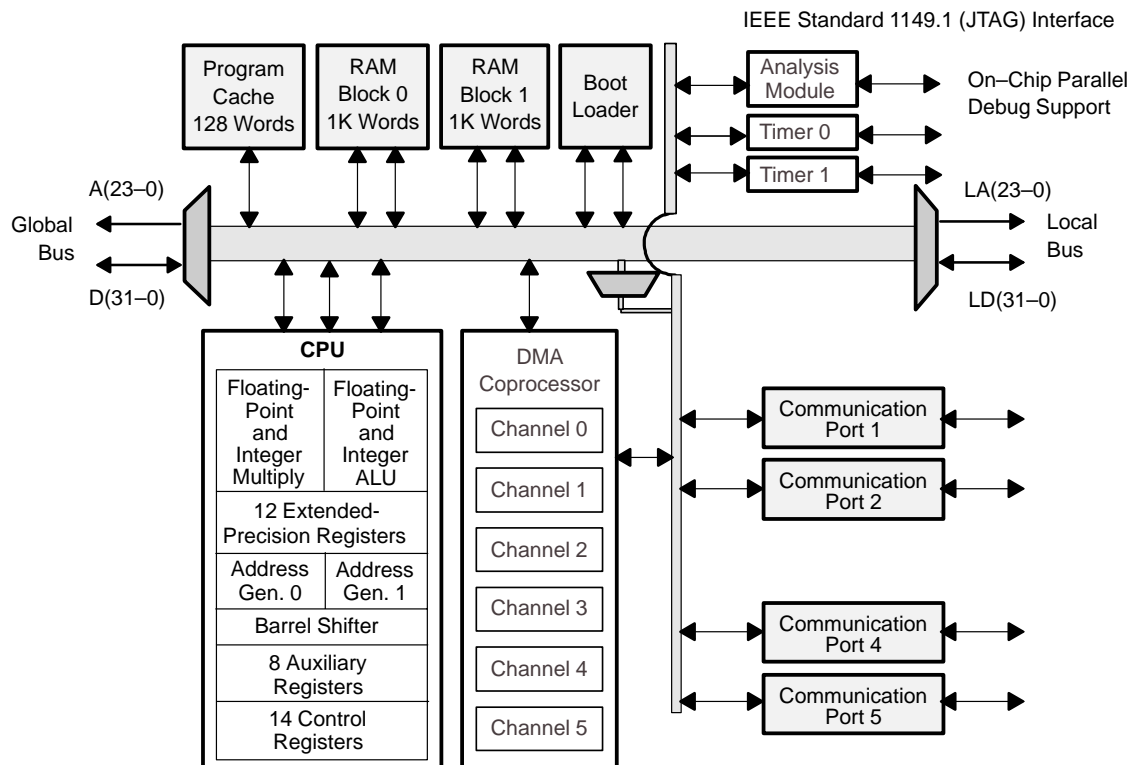
The 'C44 is a lower-cost version of the 'C40, for parallel-processing applications that are more price-sensitive. The 'C44 features four communication ports and has an external address reach of 32M words over two external buses. To further reduce cost, the 'C44 comes in a 304-pin PQFP. The TMS320C44 can deliver up to 30-MIPS/60-MFLOPS performance with a maximum I/O bandwidth of 336 Mbytes/s. The 'C44 is source-code compatible with the 'C40.

Features of the 'C44 include:

- ☐ 33- and 40-ns instruction cycle times
- ☐ Idle mode for reduced power consumption
- ☐ Optimizing ANSI C compiler
- ☐ IEEE floating-point conversion for ease of use
- ☐ 6- or 12-channel on-chip DMA
- ☐ 304-pin PQFP/388 BGA
- ☐ 32M word external address reach
- ☐ Four communication ports

Figure 8–6 shows a block diagram of the 'C44.

Figure 8–6. TMS320C44 Block Diagram



## 8.9 Tools for TMS320C4x

For information about the code generation and debugging tools available for the 'C4x devices, refer to Chapter 15, *Code Generation Tools*, and Chapter 16, *System Integration and Debugging Tools*. Table 2–14 and Table 2–15 in Chapter 2, *Selection Guide*, provide part numbers and host system information.



# TMS320C5x Devices

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The TMS320C5x generation is TI's most widely used fixed-point DSP. The 'C5x devices offer performance of 20-50 MIPS with power consumption reduced to 2.35 mA/MIPS for typical applications. The 3-V versions maintain 40-MIPS performance and reduce power consumption to 1.15 mA/MIPS.

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## 9.1 TMS320C5x Introduction

A programmable software wait-state generator has been added to the 'C5x allowing interfaces with up to seven wait states. Wait states are programmed on 8K-word boundaries allowing the designer to optimize memory configuration for performance and cost.

The standard serial port operates at up to 12.5 Mbps. This is a synchronous double-buffered serial port with independent transmit and receive sections.

The time division multiplexed (TDM) serial port has all the same features as the standard serial port with the addition of time division multiplexing, making it well suited for interprocessor communication in multiprocessor DSP systems.

The buffered serial port (BSP) comprises a full-duplex, double-buffered serial port interface and an auto-buffering unit. The BSP operates at up to 40 Mbps with no CPU intervention. The serial port interface block of the BSP is an enhanced version of the standard serial port interface.

The host port interface (HPI) is an 8-bit parallel port used to interface a host device to the 'C5x. HPI memory is a  $2K \times 16$ -bit single-access RAM (SARAM) block that can also be used as general-purpose on-chip or program SARAM.

Multiple on-chip phase-locked-loop (PLL) options are available, depending on which 'C5x is chosen. The PLL allows designers to maintain CPU speed but use a slower external clock frequency. This reduces power and electromagnetic emissions.

For systems requiring significant off-chip resources, the 'C5x family addresses  $64K \times 16$ -bit externally in program, data, and I/O spaces, each with its own select pin.

## 9.2 TMS320C5x Key Features

Following are the key features of the TMS320C5x generation. When only certain devices have a particular feature, they are named in parentheses following the feature's description.

### ☐ CPU

- 20-ns, single-cycle instruction execution time, 50 MIPS
- 25-ns, single-cycle instruction execution time, 40 MIPS
- 35-ns, single-cycle instruction execution time, 28.6 MIPS
- 50-ns, single-cycle instruction execution time, 20 MIPS
- Single-cycle multiply/accumulate (MAC) for program code
- Single-cycle/single-word repeats and block repeats for program code
- Block memory moves for better program/data management
- Four-level-deep executable pipeline to handle delayed branch, call, and return instructions
- Indexed addressing mode
- Bit-reversed/indexed addressing mode to facilitate Fast Fourier Transforms (FFTs)
- Power-down modes
- 32-bit ALU, 32-bit accumulator, and 32-bit accumulator buffer
- Eight auxiliary registers with a dedicated ALU for indirect addressing
- 16-bit parallel logic unit (PLU) for fast bit manipulation
- $16 \times 16$ -bit parallel multiplier with a 32-bit product capacity
- 0- to 16-bit right and left barrel shifters
- 64-bit incremental data shifter
- Two indirectly addressed circular data buffers for circular addressing

### ☐ Peripherals

- Eight-level hardware stack
- 11 context-switch registers to shadow the contents of strategic, CPU-controlled registers during interrupts
- Full-duplex, synchronous serial port, which directly interfaces to the codec
- Time-division-multiplexed (TDM) serial port ('C50/C51/C53)
- Buffered serial port (BSP) ('LC56, 'LC57, 'BC57S, 'C57S, 'LC57S)
- Interval timer with period and control registers for software stops, starts, and resets
- Concurrent external DMA performance, using extended holds
- On-chip clock generator
- Various phase-locked-loop (PLL) options for reduced EMI and system power dissipation

- PLL clock generator ( $\times 1, \times 2, \times 3, \times 4, \times 5, \times 9$ ) ('LC56, 'LC57, 'BC57S, 'C57S)
- IEEE 1149.1-standard (JTAG) scan-path test bus for system test and emulation
- Host-port interface ('LC57, 'BC57S)
- ☐ Memory
  - 10K 16-bit words of on-chip program/data RAM ('C50)
  - 2K 16-bit words of on-chip program/data RAM ('C51)
  - 1K 16-bit words of on-chip program/data RAM ('C52)
  - 4K 16-bit words of on-chip program/data RAM ('C53, 'C53S)
  - 7K 16-bit words of on-chip program/data RAM ('LC56, 'LC57, 'BC57S)
  - 2K 16-bit words of single-cycle on-chip boot ROM ('C50, 'BC57S)
  - 8K 16-bit words of single-cycle on-chip program ROM ('C51)
  - 4K 16-bit words of on-chip program ROM ('C52)
  - 16K 16-bit words of on-chip program ROM ('C53, 'C53S)
  - 32K 16 ROM ('LC56, 'LC57)
  - Bit words of on-chip program ROM
- ☐ Memory interfaces
  - 16 programmable software wait-state generators for program, data, and I/O memories
  - 224K-word 16-bit maximum addressable external memory space (64K-word program, 64K-word data, 64K-word I/O, and 32K-word global)
- ☐ Source code upward compatible with all 'C1x, 'C2x, and 'C2xx devices
- ☐ Single 5-V or 3.3-V supply
- ☐ Static CMOS technology
- ☐ Packaging:
  - 100-pin TQFP ('C51, 'C52, 'C53S, 'LC56)
  - 132-pin QFP ('C50, 'C51, 'C53)
  - 100-pin QFP ('C52)
  - 144-pin QFP ('BC57S)
  - 128-pin TQFP ('LC57)

### 9.3 TMS320LC57/BC57S Host Port Interface

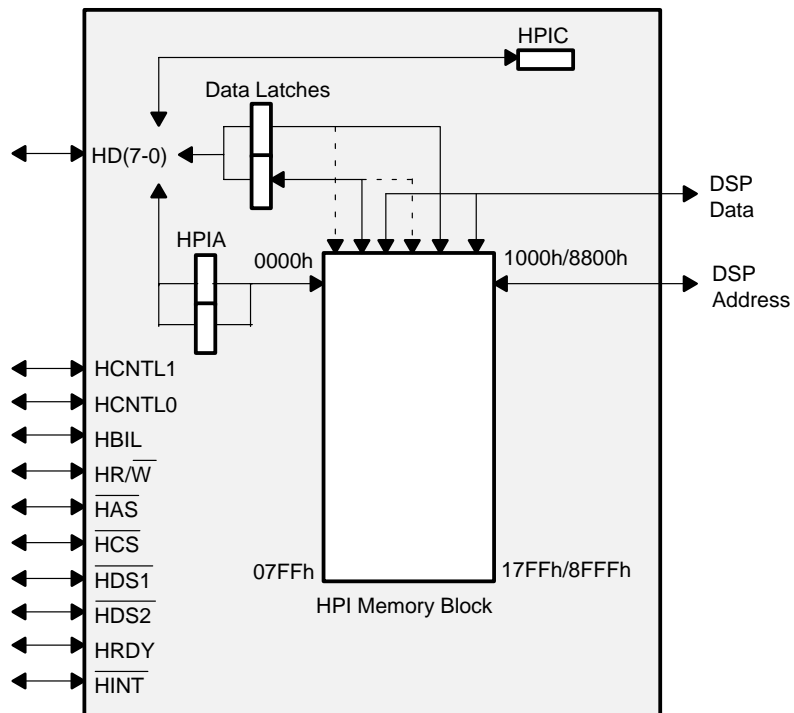
The host port interface (HPI) is an 8-bit parallel port available on the 'LC57 and the 'BC57S. The HPI provides a glueless interface to standard microprocessors as well as to other TI devices. The HPI appears as a 2K-word block of shared memory that is available in either a FIFO or standard random-access configuration. Most importantly, the HPI has the ability to maintain its high level of functionality as the interface between an external CPU and the 'C57, even while the 'C57 is idle or in reset. This significantly reduces system power consumption by offloading standard I/O tasks from the DSP.

Features of the HPI include:

- ☐ Byte-wide register addressability
- ☐ 8-bit parallel port
- ☐ High-speed back-to-back accesses
- ☐ Dedicated bus to 2K 16-bit words of SARAM
- ☐ Shared-access mode (SAM)
  - Normal mode of operation
  - Allows DSP and host to have HPI memory access
  - Asynchronous host accesses resynchronized internally
  - 45.7 Mbps at 57 MHz
  - 64.0 Mbps at 80 MHz
- ☐ Host-only mode (HOM)
  - Allows host to access HPI memory while 'C57 is in IDLE2 or in reset mode
  - 5- $\mu$ A power dissipation (IDLE2)
  - 160 Mbps, independent of clock

Figure 9–1 shows a block diagram of the 'LC57/BC57S HPI.

Figure 9–1. TMS320LC57/BC57S Host Port Interface

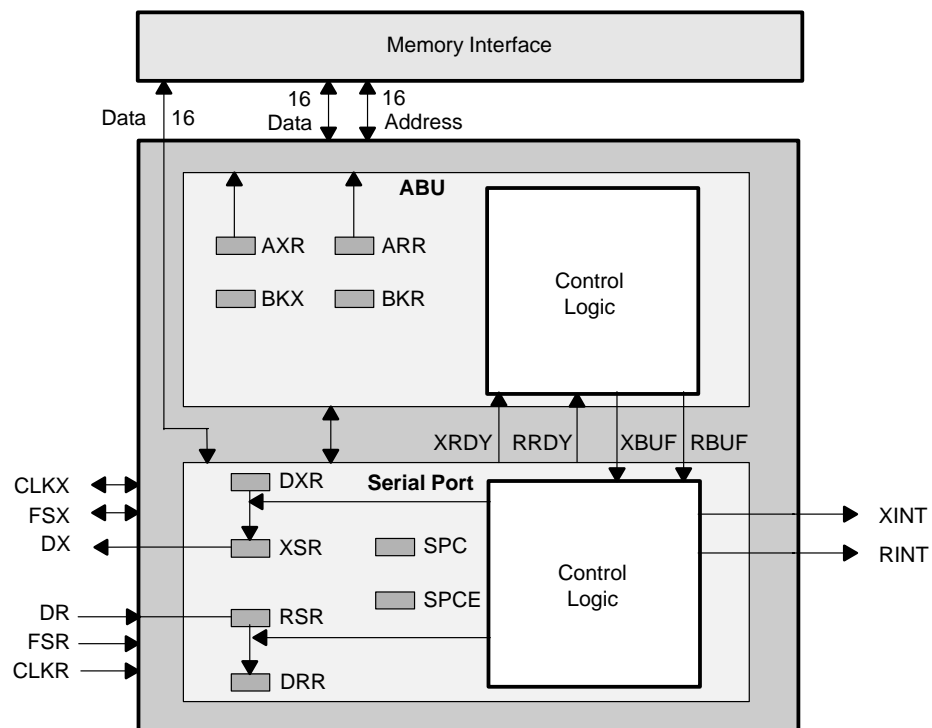


## 9.4 TMS320LC56/LC57/BC57S Buffered Serial Port

The buffered serial port (BSP) provides a no-overhead mechanism to interface serially with codecs, ADCs, and other peripherals. The BSP supports 8-, 10-, 12-, and 16-bit serial data packets and uses a 2K-byte buffer to hold input or output data. Downward code compatible with the standard serial ports, the BSP is designed to be completely flexible and programmable. The BSP has the ability to simultaneously receive data from and transmit data to a programmable on-chip buffer through a dedicated memory bus, freeing the CPU to execute other tasks without memory bus contention.

Figure 9–2 shows a block diagram of the BSP.

Figure 9–2. TMS320LC56/LC57/BC57S Buffered Serial Port



## 9.5 TMS320C5x Multiplier/ALU Features

The performance and parallelism of the 'C5x architecture become evident by studying the multiplier and accumulator sections of the device. The on-chip multiplier performs a 16-bit x 16-bit multiply with a 32-bit product in a single cycle.

To double the performance, the 'C5x devices can fetch two data operands when executing the multiply and accumulate (MAC) instruction. Scaling and fractional math shifts occur in parallel with all arithmetic operations.

The 'C5x devices are the first to include an accumulator buffer. The accumulator buffer provides quick comparisons to the accumulator contents to determine the minimum or maximum in a table of values, a common operation for both general-purpose and DSP algorithms. This is very useful in implementing Viterbi-decoding algorithms. Additionally, the accumulator buffer allows quick temporary storage of a commonly referenced value, eliminating the extra cycles it takes to store the value in memory. It also allows up to 65 bit shifts among accumulator, accumulator buffer, and carry.

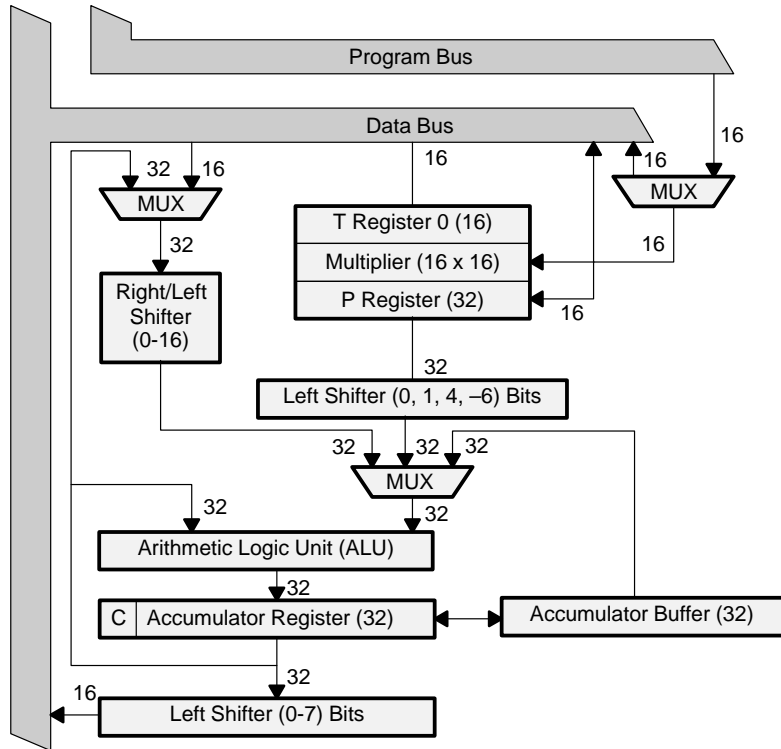
Features of the 'C5x multiplier/ALU include:

- ☐ Single-cycle 16-bit x 16-bit multiply, yielding a 32-bit product
- ☐ Ability to access program and two data operands simultaneously
- ☐ Simultaneous ALU and multiplier operations performed by the CPU
- ☐ Zero-overhead shift registers
- ☐ Accumulator buffer with path back into ALU

Figure 9–3 shows a block diagram of the 'C5x multiplier/ALU.



Figure 9–3. TMS320C5x Multiplier/ALU Features



## 9.6 TMS320C5x Parallel Logic Unit

The parallel logic unit (PLU) performs logical operations without corrupting the ALU contents. This allows data to be checked and decisions made without the overhead of storing and restoring the ALU content.

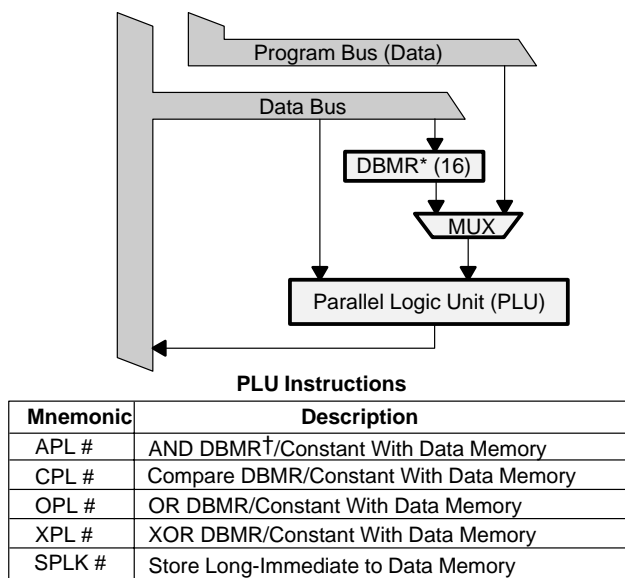
The PLU supports AND, OR, XOR, and compare functions. These functions are commonly used to set, clear, and toggle bits within a data-memory location. To make these functions easy to use, dedicated instructions perform them, using either immediate or register data to compare with the data-memory location.

Features of the 'C5x PLU are:

- ☐ Performs logical operations without disturbing arithmetic registers in ALU
- ☐ Sets, clears, and toggles any number or combinations of bits in data memory
- ☐ Compares bits individually or collectively
- ☐ Supports long-immediate and register values

Figure 9–4 shows a block diagram of the 'C5x PLU.

Figure 9–4. TMS320C5x Parallel Logic Unit



<sup>†</sup> \*DBMR: Dynamic Bit-Manipulation Register

## 9.7 TMS320C5x Interrupts

The 'C5x supports four external interrupts, two serial port interrupts, one timer interrupt, and a trap instruction.

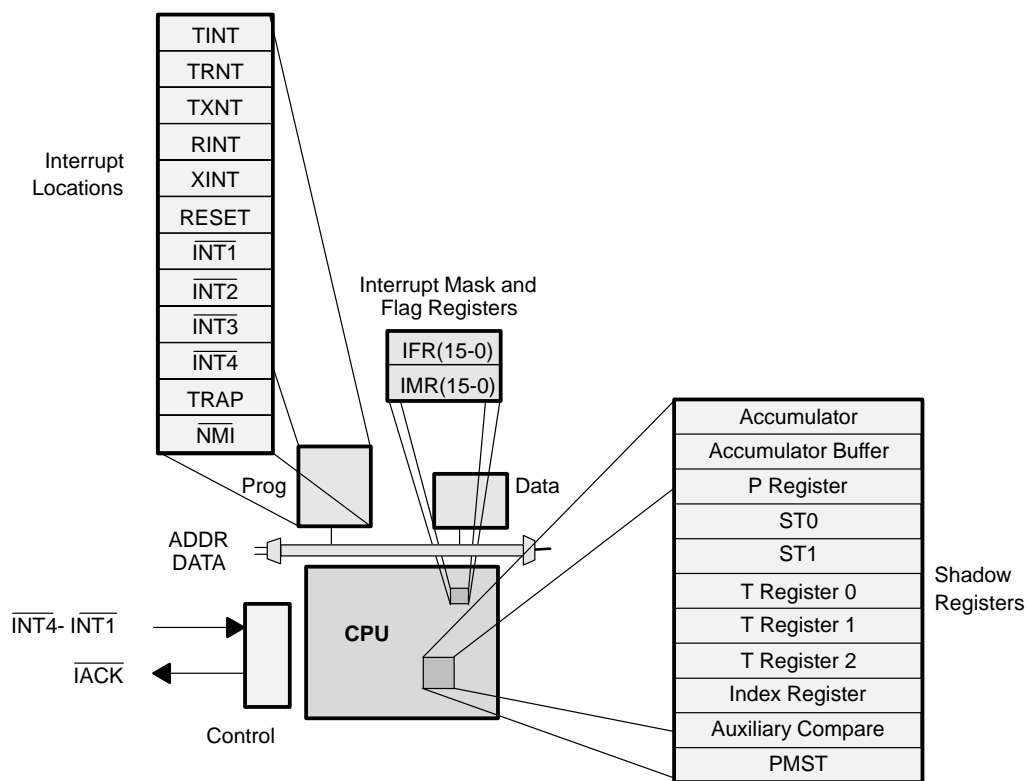
To speed up interrupt service routines (ISRs), the key registers are shadowed with a 1-level-deep stack and are saved in a single cycle. This saves 22 cycles when an interrupt occurs by eliminating the need to push and pop these 11 registers.

The 'C5x interrupt features include:

- ☐ Interrupt sources: four external, two serial port, one timer, one trap
- ☐ One-level-deep stack on strategic registers for zero-overhead context switching
- ☐ Program-accessible interrupt flag register (IFR) for software interrupt polling
- ☐ Automatic global interrupt enable on return from interrupt service routine
- ☐ Relocatable interrupt vectors

Figure 9–5 shows a block diagram of the 'C5x interrupts.

Figure 9–5. TMS320C5x Interrupts



## 9.8 TMS320C5x Circular Addressing

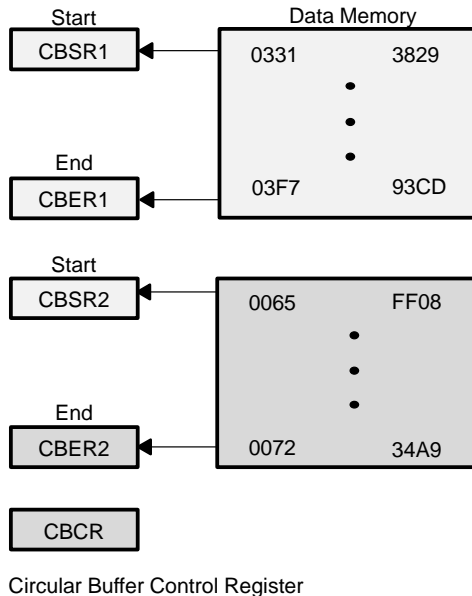
Circular addressing is a method to address "aging" data sets for common DSP algorithms. For example, after performing the first set of calculations on a finite impulse response (FIR) filter data set, a new data value must be brought in and the oldest value discarded. Data move (DMOV) allows you to do this by treating data in a circular fashion, with the oldest and newest values located side by side. At the end of each calculation, a new data value is placed in memory at the location of the oldest value. You update the circular buffer start address to correspond to the newest value and the circular buffer end address to correspond to the oldest value.

Circular addressing features are:

- ☐ Two circular-addressing data buffers
- ☐ Memory-mapped auxiliary registers to indirectly address each circular buffer
- ☐ Effective use of data-memory space while increasing performance

Figure 9–6 shows a block diagram of the 'C5x circular addressing.

Figure 9–6. TMS320C5x Circular Addressing

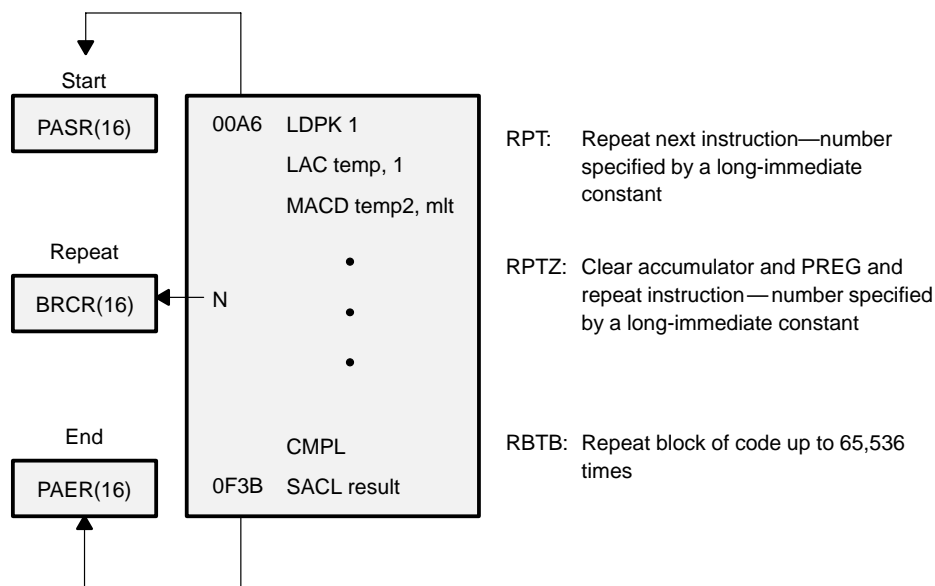


## 9.9 Repeat and Block Instructions

The 'C25 was the first device to offer a zero-overhead looping instruction, the RPT instruction. The 'C5x expands this capability with the RPTZ and RPTB instructions. The RPTZ command is a logical extension of the RPT command that also clears the accumulator and product registers. This saves two cycles in typical routines. The repeat block instruction (RPTB) allows you to repeat a block of code up to 64K times without any overhead required to branch to the beginning of the code segment. This allows you to benefit from a faster instruction cycle (due to the pipeline) without paying a penalty for program discontinuity.

Figure 9–7 shows a block diagram of the repeat and block instructions.

Figure 9–7. Repeat and Block Instructions



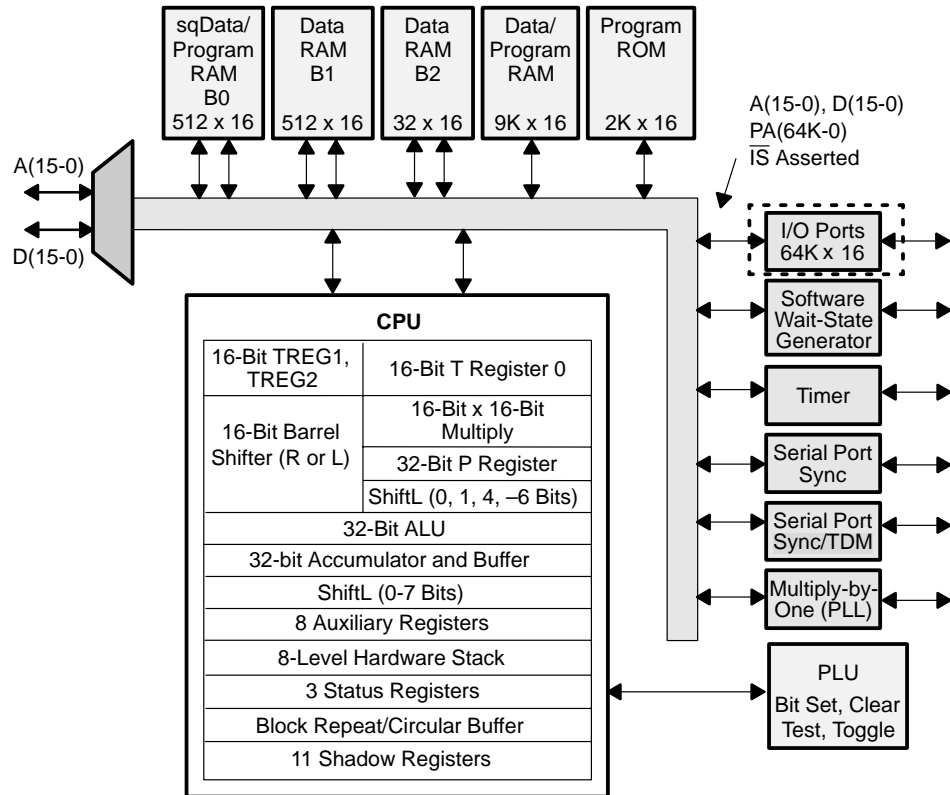
## 9.10 TMS320C50 and TMS320LC50

The 'C50 and 'LC50 feature large, on-chip RAM blocks, which are ideal for form-function emulation. The 'LC50 is the low-voltage (3.3 V) version of the 'C50 device and significantly reduces power consumption. The 'C50 is a highly integrated DSP, offering a complete system on a single chip. With a boot ROM and 10K 16-bit words of on-chip RAM, an entire DSP can be integrated into a 132-pin QFP. By integrating the memory on-chip, you reduce both power and board space. Integrating the off-chip memory can be especially important in high-performance systems to eliminate expensive high-speed static RAM (SRAM).

The 'C50 offers 25-, 35-, and 50-ns instruction cycle times and accepts source code from the 'C1x, 'C2x, and 'C2xx generations. It has a full-duplex synchronous serial port, time division multiplexed (TDM) communication port, and pre-programmed ROM bootloader. Other features of the 'C50 include a 192K-word external address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control.

Figure 9–8 shows a block diagram of the 'C50/LC50.

Figure 9–8. TMS320C50/LC50 Block Diagram



## 9.11 TMS320C51 and TMS320LC51

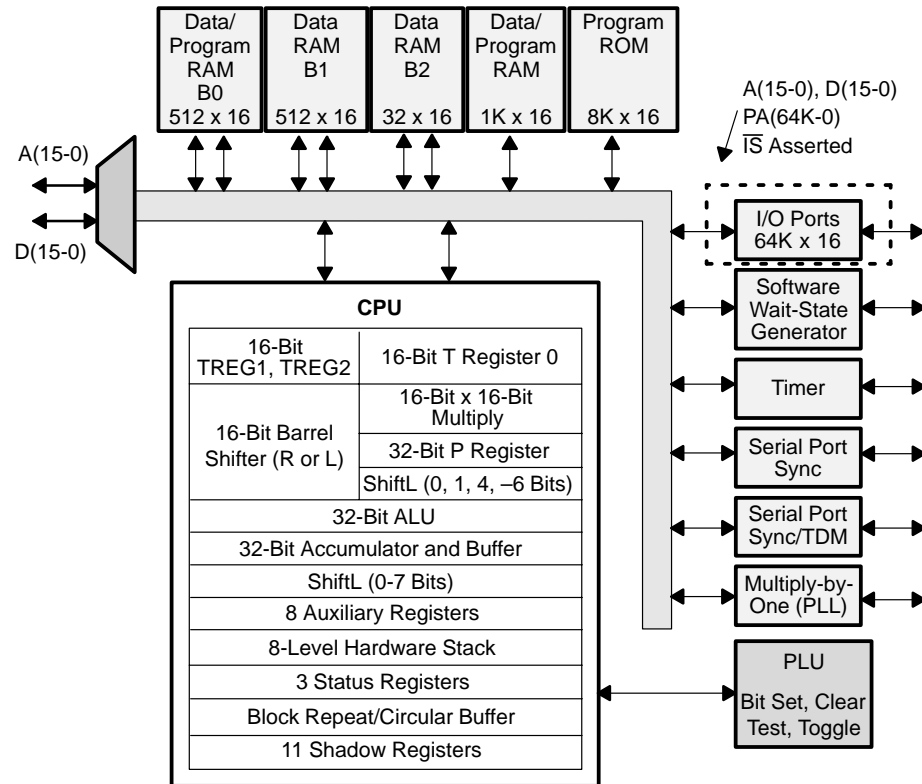
The 'C51 features a user-maskable ROM for implementing information that was preprogrammed by TI. It is object-code and pin compatible with the 'C50 device. The 'LC51 is the low-voltage version of the 'C51. In the 'C51, the 'C50's 9K-word block of RAM is replaced by 8K 16-bit words of on-chip ROM. This provides a considerable advantage in cost and performance for users who require large amounts of on-chip program space. With this ROM and 2K 16-bit words of RAM, sophisticated DSP algorithms can fit on a single device. This device is available in a 132-pin QFP and a 100-pin TQFP measuring only  $14 \times 14 \times 1.4$  mm for designs that require both small board area and reduced height. The 'C51 is available in 3.3 V or 5 V and 50-, 35-, 25-, or 20-ns cycle times, has communication ports similar to those of the 'C50, and has an optional preprogrammed ROM bootloader.

The 'C51 accepts source code from the 'C1x, 'C2x, and 'C2xx generations. It also has a full-duplex synchronous serial port and a TDM serial port. Other features of the 'C51 include a 192K-word external-address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control.

Figure 9–9 shows a block diagram of the 'C51/LC51.



Figure 9–9. TMS320C51/LC51 Block Diagram



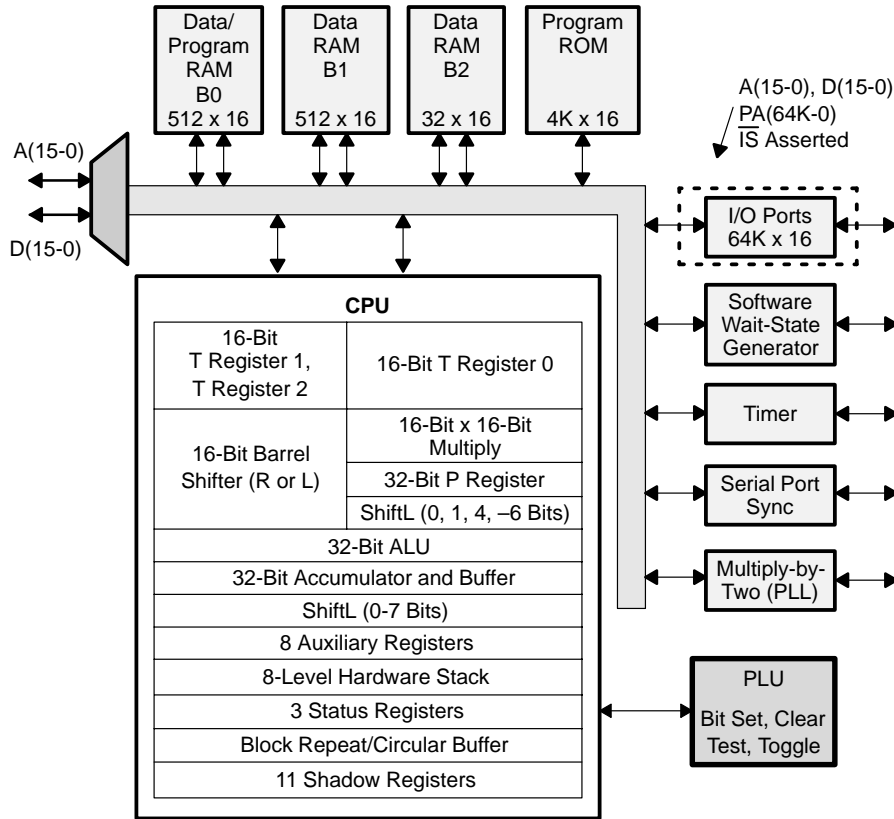
## 9.12 TMS320C52 and TMS320LC52

The 'C52 is a cost-effective implementation of the 'C5x architecture. The 'LC52 is the low-voltage version. Traditionally, devices in the same price range have offered 10-MIPS performance. The 'C52 provides twice the performance at 20 MIPS and has room to grow into a 50-MIPS version. The 4K 16-bit words of ROM and 1K 16-bit words of RAM can be configured with your code or purchased preprogrammed with a bootloader. The 'C52 is available in 3.3 V or 5 V; has 50-, 35-, 25-, or 20-ns cycle times; comes in a 100-pin QFP and a 100-pin TQFP; has a full-duplex synchronous serial port; and has an optional preprogrammed ROM boot loader.

The 'C52 accepts source code from the 'C1x, 'C2x, and 'C2xx generations. It also has a 192K-word external address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control.

Figure 9–10 shows a block diagram of the 'C52/LC52.

Figure 9–10. TMS320C52/LC52 Block Diagram



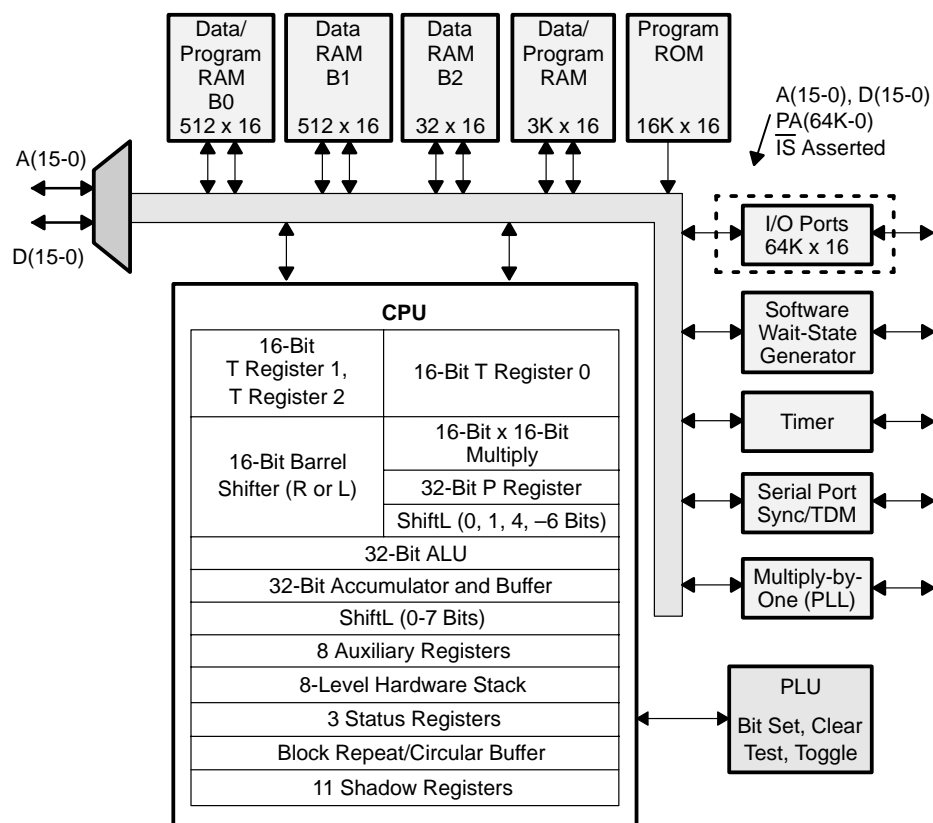
### 9.13 TMS320C53 and TMS320LC53

The 'C53 and 'LC53 provide greater integration of on-chip ROM than the 'C51. The advantage of bringing memory on chip reduces power and board-space requirements; on-chip memory also provides a considerable advantage in cost and performance. The 16K 16-bit words of ROM and 4K 16-bit words of on-chip RAM can be configured with your code or purchased preprogrammed with a bootloader. The 'C53 is available in 3.3 V or 5 V; has 50-, 35-, or 25-ns cycle times; comes in a 132-pin PQFP; and has a full-duplex synchronous serial port, and a TDM communications port.

The 'C53 accepts source code from the 'C1x, 'C2x, and 'C2xx generations. It also has a 192K-word external address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control.

Figure 9–11 shows a block diagram of the 'C53/LC53.

Figure 9–11. TMS320C53/LC53 Block Diagram



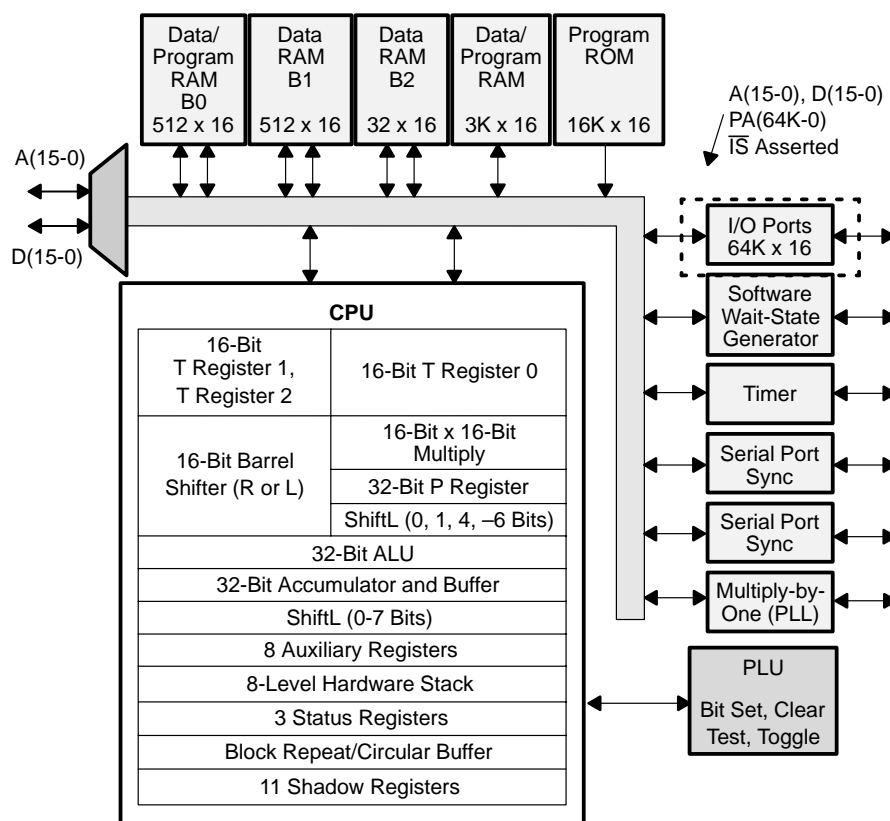
## 9.14 TMS320C53S and TMS320LC53S

The 'C53S and 'LC53S are similar in most respects to the 'C53 and LC53. To accommodate the integration capabilities of the 'C53 into a 100-pin TQFP, some features were removed from the standard 'C53. The 'C53S offers two standard serial ports instead of the TDM and standard serial ports in the 'C53. The 'C53S has reduced capability of the on-chip analysis block and has no boundary scan.

The 'C53S offers 25-, 35-, and 50-ns instruction cycle times and accepts source code from the 'C1x, 'C2x, and 'C2xx generations. Other features of the 'C53s include a 192K-word external address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control. The 'C53S also offers an optional preprogrammed ROM boot loader.

Figure 9–12 shows a block diagram of the 'C53S/LC53S.

Figure 9–12. TMS320C53S/LC53S Block Diagram



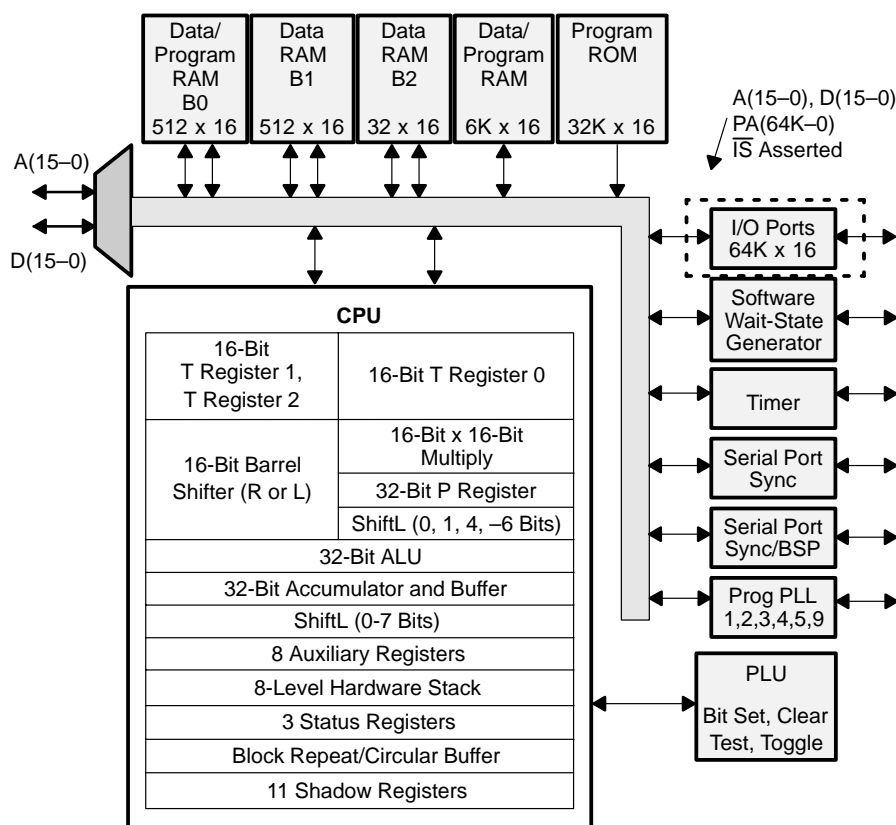
## 9.15 TMS320LC56

The 'LC56 provides greater integration of on-chip ROM than the 'C53. With 32K 16-bit words of on-chip ROM and 7K 16-bit words of on-chip RAM, the 'LC56 can accommodate large program and data spaces on-chip, thereby minimizing off-chip accesses. The communications ports comprise a full-duplex synchronous serial port and a very fast BSP with a dedicated bus. The BSP is capable of 40 Mbps at a 25-ns instruction cycle time. The 'LC56 is optimized for high-performance, low-power applications; as a result, it operates at 3.3 V only.

The 'LC56 offers 25- and 35-ns instruction cycle times and accepts source code from the 'C1x, 'C2x, and 'C2xx generations. Other features of the 'LC56 include a 192K-word external address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control, a boot ROM option, and programmable PLL. The 'LC56 comes in a 100-pin TQFP.

Figure 9–13 shows a block diagram of the 'LC56.

Figure 9–13. TMS320LC56 Block Diagram



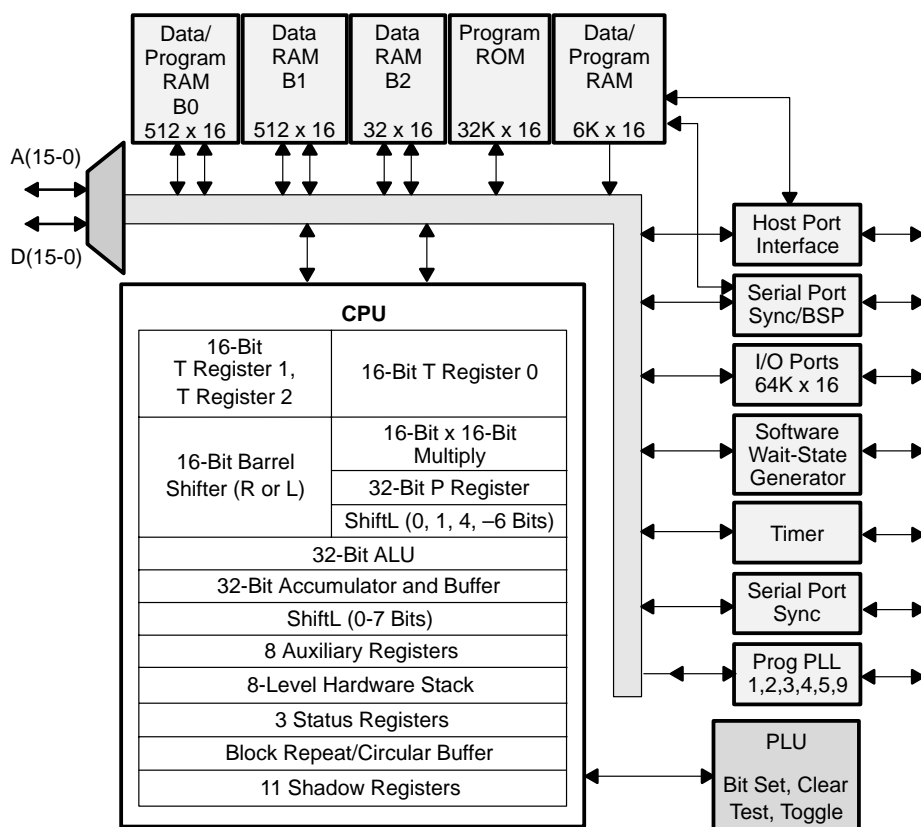
## 9.16 TMS320LC57

The 'LC57 incorporates the same amount of on-chip memory as the 'LC56 and offers a high-throughput buffered serial port. In addition, the 'LC57 provides an 8-bit wide host port interface (HPI), which can be used to communicate with other 'LC57 devices or embedded microprocessors. The 'LC57, like the 'LC56, is capable of 25-ns instruction cycle time at 3.3 V.

The 'LC57 offers 25- and 35-ns instruction cycle times and accepts source code from the 'C1x, 'C2x, and 'C2xx generations. Other features of the 'LC57 include a boot load through the HPI or a standard serial port, a 192K-word external address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control. The 'LC57 also offers a boot ROM option, a full-duplex synchronous serial port, programmable PLL, a BSP with a dedicated bus, and an HPI with a dedicated bus. The 'LC57 is packaged in a 128-pin TQFP.

Figure 9–14 shows a block diagram of the 'LC57.

Figure 9–14. TMS320LC57 Block Diagram



## 9.17 TMS320BC57S

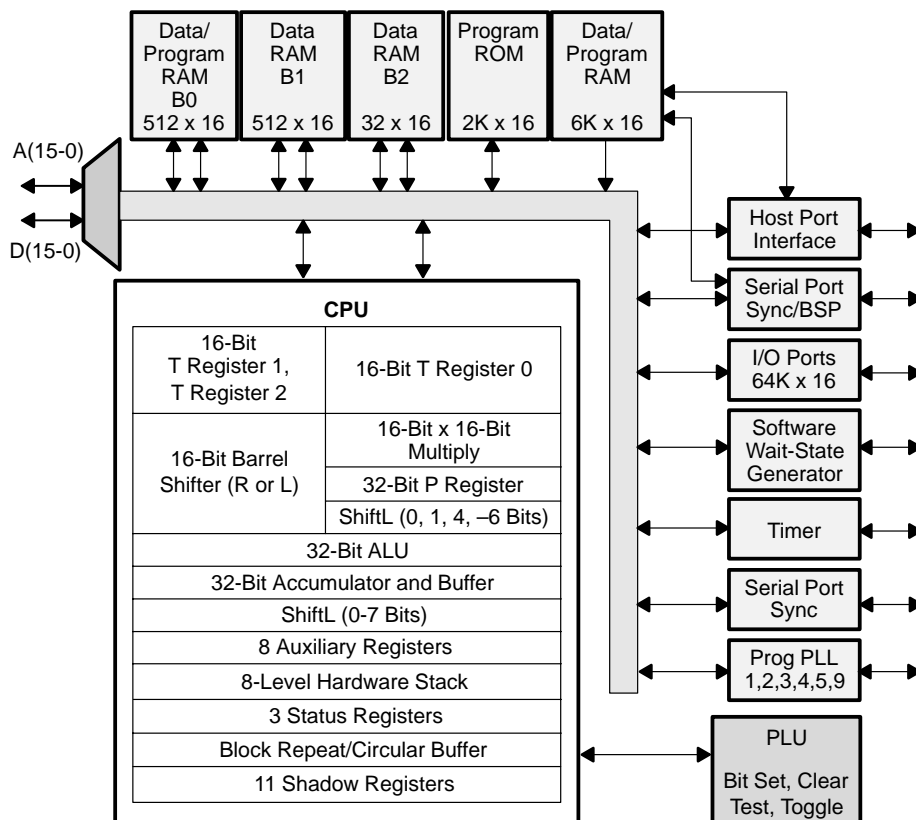
The 'BC57S takes advantage of the same peripherals that are on the 'LC57 to make the 'BC57S a cost-effective embedded data I/O engine. In order to provide a broad-based appeal, the 'BC57S differs from the 'LC57 in four ways:

- ☐ The 32K 16-bit words of ROM space has been replaced with a boot ROM.
- ☐ The 'BC57S can operate at 5 V.
- ☐ The 144-pin package of the 'BC57S has a wider lead pitch than the package of the 'LC57.
- ☐ The 'BC57S is lower in cost.

The 'BC57S offers 25-, 35-, and 50-ns instruction cycle times at 5 V; accepts source code from the 'C1x, 'C2x, and 'C2xx generations; and has 7K 16-bit words of RAM. Other features include a 192K-word external address reach, an ANSI C compiler, and an IEEE 1149.1-standard (JTAG) emulator control. The communication ports include a full-duplex synchronous serial port, an HPI with a dedicated bus, and a BSP with a dedicated bus. The 'LC57S is packaged in a 144-pin TQFP.

Figure 9–15 shows a block diagram of the 'BC57S.

Figure 9–15. TMS320BC57S Block Diagram





## 9.18 Tools for TMS320C5x

For information about the code generation and debugging tools available for the 'C5x devices, refer to Chapter 15, *Code Generation Tools*, and Chapter 16, *System Integration and Debugging Tools*. Table 2–14 and Table 2–15 in Chapter 2, *Selection Guide*, provide part numbers and host system information.

# TMS320C54x Devices

The TMS320C54x devices are fixed-point digital signal processors (DSPs) in the TMS320 family. The '54x meets the specific needs of real-time embedded applications, such as telecommunications. The '54x central processing unit (CPU), with its modified Harvard architecture, features minimized power consumption and a high degree of parallelism. Also, the versatile addressing modes and instruction set improve the overall system performance.

The '54x devices offer these advantages:

- ☐ Enhanced Harvard architecture built around one program and three data buses for increased performance and versatility
- ☐ Advanced CPU design with a high degree of parallelism and application-specific hardware logic for increased performance
- ☐ A highly specialized instruction set for faster algorithms and for optimized high-level language operation
- ☐ Modular architecture design for fast development of spinoff devices
- ☐ Advanced IC processing technology for increased performance and low power consumption
- ☐ Low power consumption and increased radiation hardness because of new static design techniques

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## 10.1 TMS320C54x Introduction

With two 40-bit accumulators, the 'C54x is an accumulator-based DSP. A 40-bit adder dedicated to multiply and accumulate (MAC) operations has a separate 40-bit arithmetic logic unit (ALU) that feeds the accumulators. The ALU and two accumulators support eight special parallel instructions that execute in one cycle. The ALU also features a dual 16-bit configuration that enables dual single-cycle operations. The 40-bit adder, at the output of the multiplier, allows unpipelined MAC operations as well as dual addition and multiplication in parallel. The multiplier performs  $17 \times 17$ -bit multiplies to allow 16-bit signed or unsigned multiplication, with rounding and saturation control in one cycle. Single-cycle normalization and exponential encoding support floating-point arithmetic.

The 'C54x's instruction set complements the parallelism of the architecture. It supports many two- and three-operand instructions, as well as some 32-bit operands. Eight individually addressable auxiliary registers and a software stack aid a C compiler's efficiency.

The standard serial port operates at up to 12.5 Mbps. This is a synchronous double-buffered serial port with independent transmit and receive sections. The time division multiplexed (TDM) serial port has all of the same features as the standard serial port with the addition of time division multiplexing, making it well suited for interprocessor communication in multiprocessor DSP systems.

The buffered serial port (BSP) comprises a full-duplex, double-buffered serial port interface and an auto-buffering unit. The serial port interface block of the BSP is an enhanced version of the standard serial port interface.

The host port interface (HPI) is an 8-bit parallel port used to interface a host processor to the TMS320C54x. The HPI memory is a  $2K \times 16$ -bit single-access RAM block that can also be used as general-purpose on-chip or program single-access RAM (SARAM).

The 'C54x's architectural efficiencies, 100 MIPS, and low power dissipation make it an ideal device for a variety of wireless and wireline communications systems. Standard wireless applications like cellular handsets can take advantage of the 'C54x's power-down modes, high performance, and large ROM memory spaces for integrating entire algorithms on-chip. The high performance and large RAM of the 'C542 and 'C548 are useful for reconfigurable systems where a variety of different algorithms must be executed from on-chip memory. Data communications or telephony applications can increase system functionality while lowering system cost by allowing the 'C54x to absorb the existing system functionality of multiple-DSP implementations.

## 10.2 TMS320C54x CPU Key Features

The 'C54x, 'LC54x, and 'VC54x fixed-point digital signal processors are fabricated with an advanced modified Harvard architecture which has one program memory bus and three data memory buses. The core's key features include a 17-bit x 17-bit multiplier (16-bit signed or unsigned); a dedicated 40-bit adder for unpipelined MAC (multiply/accumulate) operation; a separate 40-bit ALU for increased parallelism; two 4-bit accumulators; and a compare, select, store unit (Viterbi accelerator). The 'C54x uses a highly specialized dual-operand instruction set that is the basis of the operational flexibility and speed of these DSPs. The 'C54x also includes eight auxiliary registers and a software stack to enable a highly-optimized C compiler. The devices lower power consumption, reduce chip count, and enable system cost savings for communications applications.

The 'C54x CPU key features include:

- ☐ Advanced multibus architecture with three separate 16-bit data buses and one program bus
- ☐ 40-bit ALU, including a 40-bit barrel shifter and two independent 40-bit accumulators
- ☐ 17-bit x 17-bit parallel multiplier coupled to a 40-bit dedicated adder for nonpipelined, single-cycle multiply and accumulate (MAC) operation
- ☐ Compare, select, store unit (CSSU) for the add/compare selection of the Viterbi operator
- ☐ Exponent encoder to compute the exponent of a 40-bit accumulator value in a single cycle
- ☐ Two address generators, including eight auxiliary registers and two auxiliary register arithmetic units

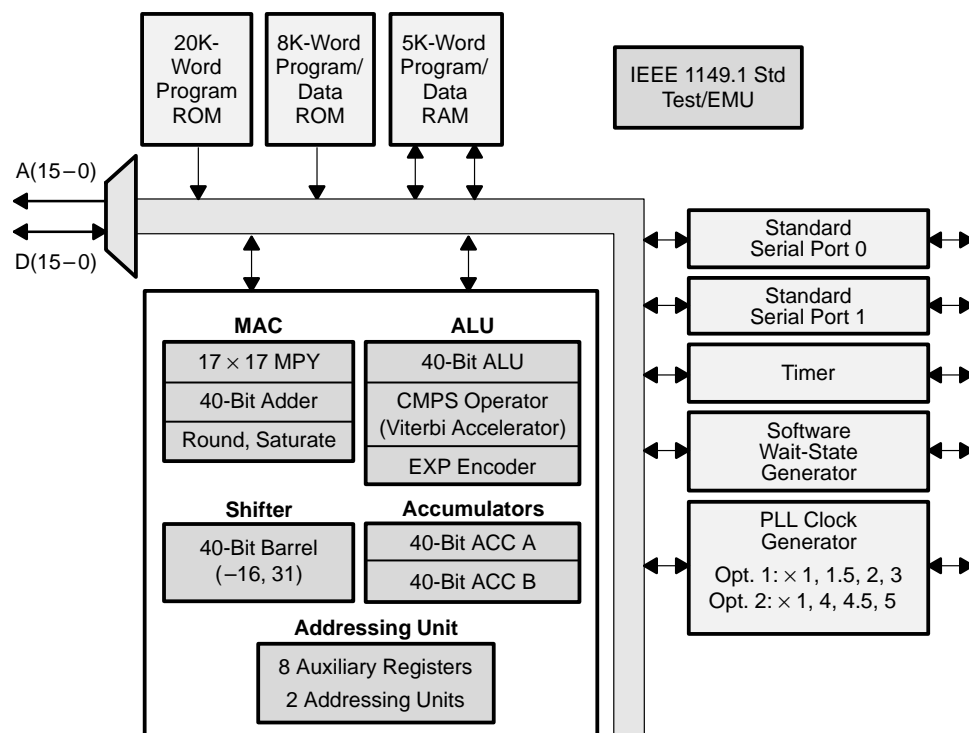
### 10.3 TMS320C541

The 'C541 family consists of advanced performance, low-power digital signal processors optimized for communications applications. There are two low-voltage versions: the 'LC541 (3.3 V) and the 'VC541 (3.0 V). The device offers 28K 16-bit words of ROM and 5K 16-bit words of RAM on-chip, two standard serial ports, a timer, a software wait-state generator, and a phase-locked loop (PLL) clock generator all integrated into the 100-pin TQFP, measuring  $14 \times 14 \times 1.4$  mm.

The 'C541 also features an integrated Viterbi accelerator; powerful single-cycle instructions (dual-operand, parallel, and conditional instructions); low active-mode power dissipation (less than 35 mW to run VSELP); low-power standby modes; and multiple PLL options. The 'LC541 and 'VC541 offer instruction cycle times of 25 ns (40 MIPS) or 20 ns (50 MIPS); 5-V version of the 'C541 is only available at 25 ns.

Figure 10–1 shows a block diagram of the 'C541.

Figure 10–1. TMS320C541 Block Diagram



Note: The 'LC541 is available with one of two different PLL options. You choose one of the options listed.

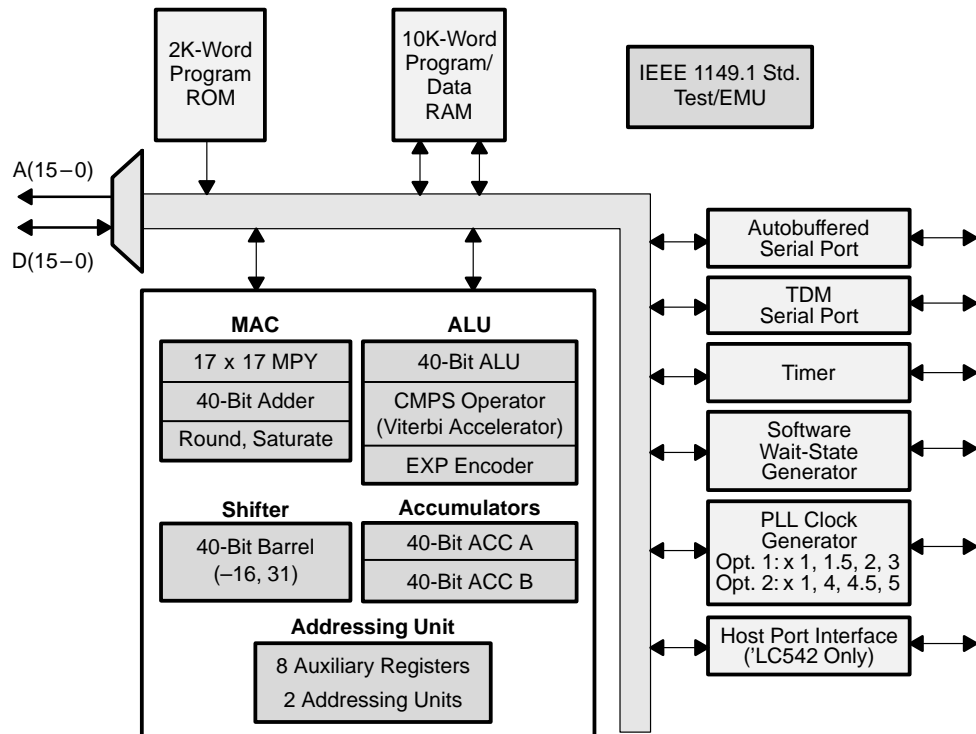
## 10.4 TMS320C542, TMS320LC542/VC542, and TMS320LC543/VC543

The 'C542 offers designers a low-cost, low-power, high-performance digital signal processor with 2K 16-bit words of boot ROM and 10K 16-bit words of RAM on-chip. There are two low-voltage versions: the 'LC542 (3.3 V) and the 'VC542 (3.0 V). Peripherals include a BSP, an HPI (which interfaces with other DSPs or embedded microprocessors), a timer, and a TDM serial port.

The 'C542 family devices feature an integrated Viterbi accelerator; powerful single-cycle instructions (dual-operand, parallel, and conditional instructions); low active-mode power dissipation (less than 35 mW to run VSELP); and low-power standby modes. These devices offer instruction cycle times of 25 ns (40 MIPS) or 20 ns (50 MIPS); the 5-V version of the 'C542 is available only at 25 ns.

The 'C542 is available in a 144-pin TQFP ( $20 \times 20 \times 1.4$  mm), while the 'LC542 and 'VC542 are available in a 128- or 144-pin TQFP. The 'LC543 and 'VC543 offer a cost reduction by removing the HPI and are available in a 100-pin TQFP, measuring  $14 \times 14 \times 1.4$  mm.

Figure 10–2. TMS320C542/LC543 Block Diagram



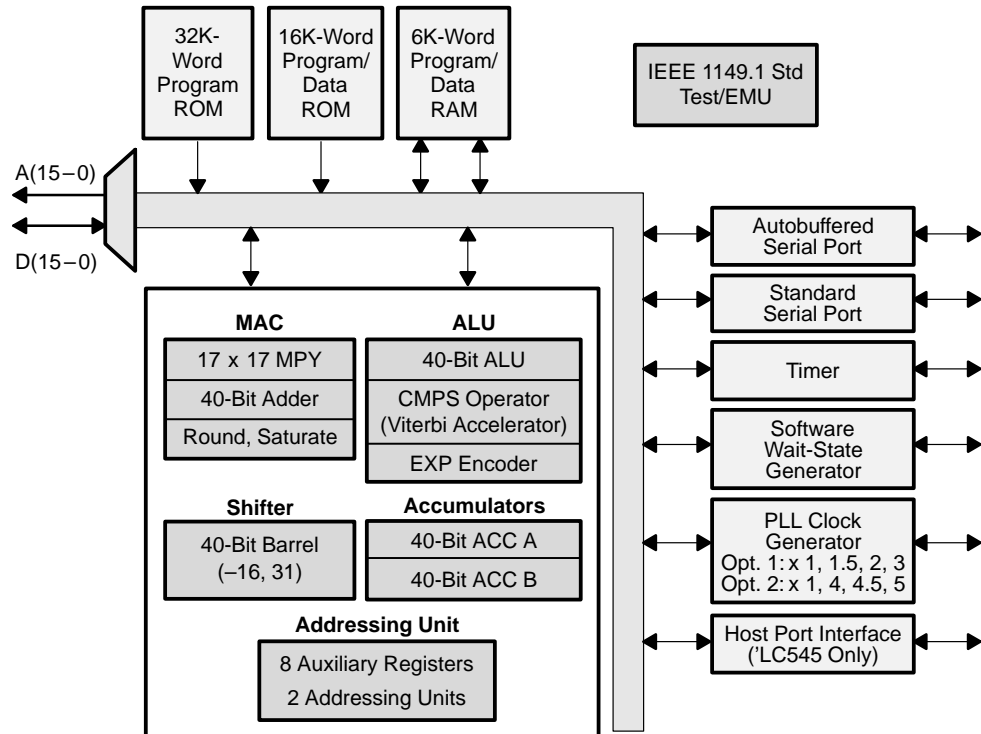
Note: The 'LC542 and 'LC543 are available with one of two different PLL options. You choose one of the options listed.

## 10.5 TMS320LC545/VC545 and TMS320LC546/VC546

The 'LC545 and 'LC546 DSPs lower power consumption and provide the first single-DSP solutions for next-generation cellular standards. The 'VC545 and 'VC546 are very-low voltage (3.0 V) versions. The devices have the on-chip memory (48K 16-bit words of ROM, 6K 16-bit words of RAM), performance, and intelligent peripherals required to support the half-rate GSM, half-rate PDC, and CDMA enhanced variable-rate coder (EVRC). Complementing the large amount of on-chip memory is an autobuffered serial port, an HPI for interfacing with other DSPs or embedded microprocessors, a standard serial port, a software wait-state generator, and a PLL clock. The 'LC545/VC545 and 'LC546/VC546 devices feature an integrated Viterbi accelerator; powerful single-cycle instructions (dual-operand, parallel, and conditional instructions); low active-mode power dissipation (less than 35 mW to run VSELP); and low-power standby modes. These devices offer instruction cycle times of 25 ns (40 MIPS) or 20 ns (50 MIPS). The 'LC545 is available in a 128-pin TQFP. The 'LC546 offers a cost reduction by removing the HPI and is packaged in a 100-pin TQFP.

Figure 10–3 shows a block diagram of the 'LC545/LC546.

Figure 10–3. TMS320LC545/LC546 Block Diagram



Note: The 'LC545 and 'LC546 are available with one of two different PLL options.  
You choose one of the options listed.



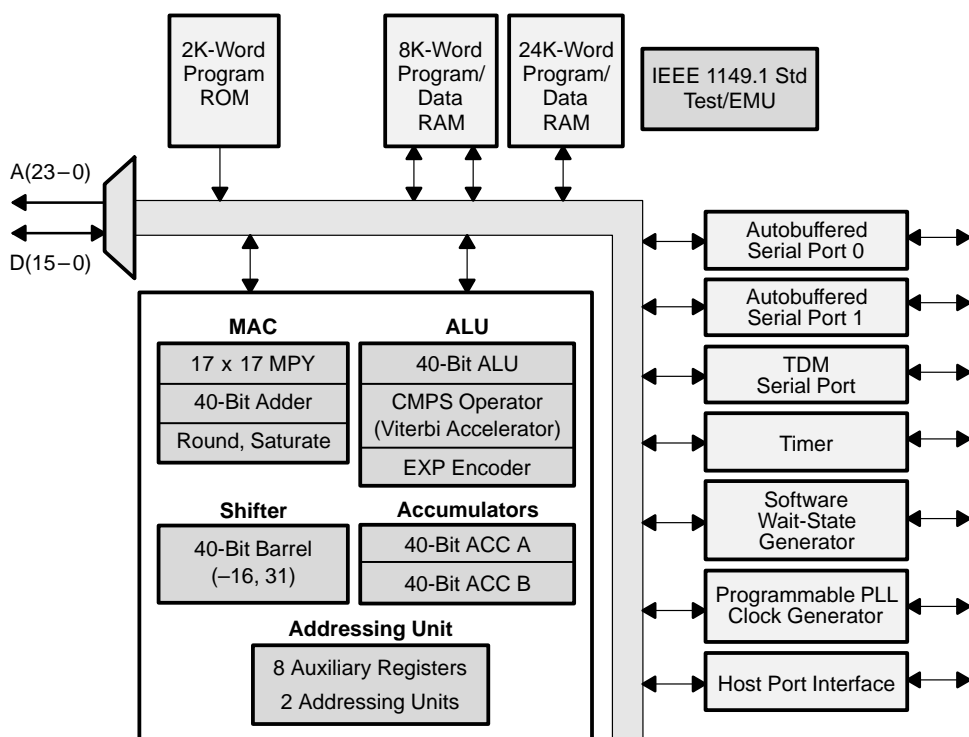
## 10.6 TMS320LC548

The TMS320LC548 combines high performance with low power consumption, making it well suited for wireless telecommunications and other mobile systems that need to perform complex functions while also conserving battery power. The 'LC548 includes two high-speed BSPs, one TDM serial port, a HPI, and a 16-bit on-chip timer. The 'LC548 can operate at 20 ns (50 MIPS), 15 ns (66 MIPS), 12.5 ns (80 MIPS), or 10 ns (100 MIPS) with a supply voltage of 3.3 V. These devices offer 32K 16-bit words of RAM and 2K 16-bit words of boot ROM on-chip, as well as an extended addressing mode for 4M x 16-bit maximum addressable external program space.

These devices also feature an integrated Viterbi accelerator; powerful single-cycle instructions (dual-operand, parallel, and conditional instructions); low active-mode power dissipation (less than 35 mW to run VSELP); low-power standby modes; and JTAG with boundary scan.

Figure 10–4 shows a block diagram of the 'LC548/VC548.

Figure 10–4. TMS320LC548/VC548 Block Diagram



## 10.7 Tools for TMS320C54x

For information about the code generation and debugging tools available for the 'C54x devices, refer to Chapter 15, *Code Generation Tools*, and Chapter 16, *System Integration and Debugging Tools*. Table 2–14 and Table 2–15 in Chapter 2, *Selection Guide*, provide part numbers and host system information.

# TMS320C8x Devices

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TMS320C8x devices—the world's first 64-bit DSPs designed for the multi-processing environment—include the 'C80 and the 'C82. This chapter describes the devices, lists key features, and provides block diagrams.

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## 11.1 TMS320C8x Introduction

The processing power of the 'C8x devices supports any application that requires high-performance digital signal processing. The first member of the 'C8x generation, the 'C80, is a single-chip, parallel processor that can be used for applications such as real-time audio/video processing, high-end data communications, and image processing. The 'C82 is the second member of the 'C8x family that can be used in high-volume applications like desktop video-conferencing, high-speed telecommunications, and three-dimensional graphics.

Since the 'C8x devices are fully programmable, you can blend industry-standard algorithms with proprietary software to optimize system performance and differentiate products in the market. You receive added flexibility, because a 'C8x-based system can be adapted to evolving technologies through software modifications rather than hardware redesigns. This enables you to upgrade as new standards emerge.

## 11.2 TMS320C8x Key Features

The following are key features of the high-performance TMS320C8x generation.

- ☐ Version capable of over 2 billion operations per second (BOPS)
- ☐ 40-, 50- or 60-MHz performance
- ☐ A 32-bit reduced instruction set computer (RISC) master processor with an integrated IEEE-754 floating-point unit
- ☐ Multiple 32-bit parallel processors (advanced DSPs) with 64-bit instruction words
  - Four parallel processors in the 'C80
  - Two parallel processors in the 'C82
- ☐ 50K bytes of on-chip RAM on the 'C80 and 44K bytes of on-chip RAM on the 'C82
- ☐ An on-chip crossbar that allows multiple instruction fetches and parallel data accesses during each cycle to support high transfer rates
  - Up to 4.2 Gbytes/s transfer rates on the 'C80
  - Up to 2.6 Gbytes/s transfer rates on the 'C82
- ☐ Big-endian and little-endian byte-ordering modes
- ☐ A 4G-byte memory address space
- ☐ A 64-bit transfer controller capable of up to 400 Mbytes/s in on-chip and off-chip memory transfers
  - Dynamic sizing of bus width (64, 32, 16, or 8 bits)
  - Direct access to 64-bit VRAM/DRAM/SRAM/SDRAM memory
  - Direct access to 64-bit extended data out (EDO) DRAM ('C82)
- ☐ A video controller that contains dual-frame timers for simultaneous image capture and display ('C80 only)
- ☐ Four external interrupts (three edge-triggered and one level-triggered)
- ☐ A full-scan design (plus boundary scan), accessed via an IEEE Standard 1149.1 (JTAG) compliant test port that provides emulation support
- ☐ A 3.3-V design
- ☐ TI EPIC™ 0.5 μm CMOS technology
- ☐ Efficient packaging
  - 305-pin ceramic pin grid array (CPGA) or 352 ceramic ball grid array (CBGA) ('C80)
  - 352-ball grid array (BGA) ('C82)

### 11.3 TMS320C8x Master Processor (MP)

The master processor (MP) is a 32-bit RISC processor with an integral IEEE-754 floating-point unit. As with other RISC processors, all accesses to memory are performed with load and store instructions, and most integer and logical operations are performed on registers in a single cycle. The floating-point instructions are pipelined; therefore, you can start a single-precision multiply or any floating-point add instruction on each clock cycle. Moreover, the floating-point unit approaches 120 MFLOPS in performance at 60-MHz internal clock rate.

Floating-point operations use the same register file as the integer and logic unit. A register scoreboard ensures that correct register-access sequences are maintained.

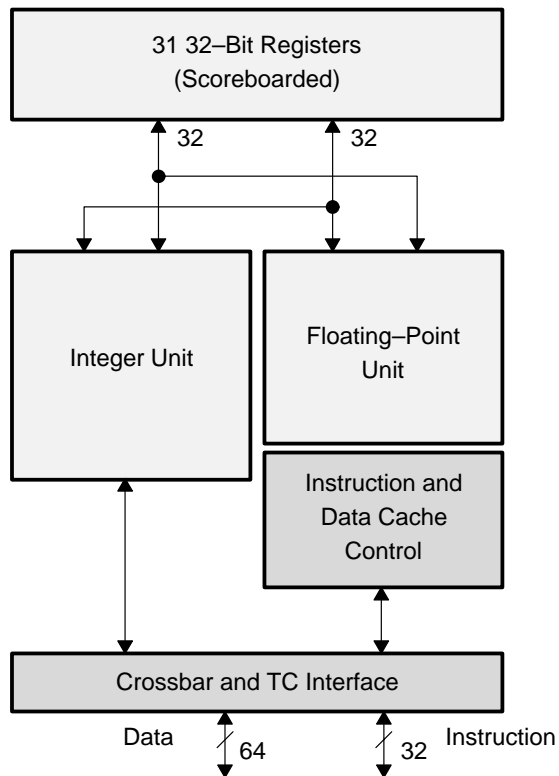
The MP is structured for efficient execution of C code. For example, the MP contains an R0 register, often called a zeroing register, used by C. Also, the MP instruction set is tailored to contain many of the C executables found in compiler technology.

Features of the master processor include:

- ☐ 32-bit RISC CPU delivering 60 MIPS at 60 MHz
  - Targeted for high-level languages
- ☐ IEEE-754 120-MFLOP floating-point unit
  - Parallel multiply, add, and load/store
- ☐ 31 32-bit registers
  - Single file for integer and floating point
  - Loads and FPU results are scoreboarded
- ☐ Instruction and data cache control
  - 4K-byte instruction cache
  - 4K-byte data cache
  - 2K-byte parameter RAM ('C80), 4K-byte parameter RAM ('C82)

Figure 11–1 shows a block diagram of the 'C8x master processor.

Figure 11–1. TMS320C8x Master Processor (MP)



## 11.4 TMS320C8x MP Floating-Point Unit

The MP's floating-point unit is capable of performing IEEE-754 floating-point operations in 32-bit single-precision and 64-bit double-precision floating point. Conversion between different formats is also supported. In addition, the floating-point unit provides vector floating-point operations with the option of performing a parallel load or store to improve program efficiency.

Hardware support for the floating-point unit consists of a full double-precision floating-point add unit and a 32-bit single-precision floating-point multiply unit.

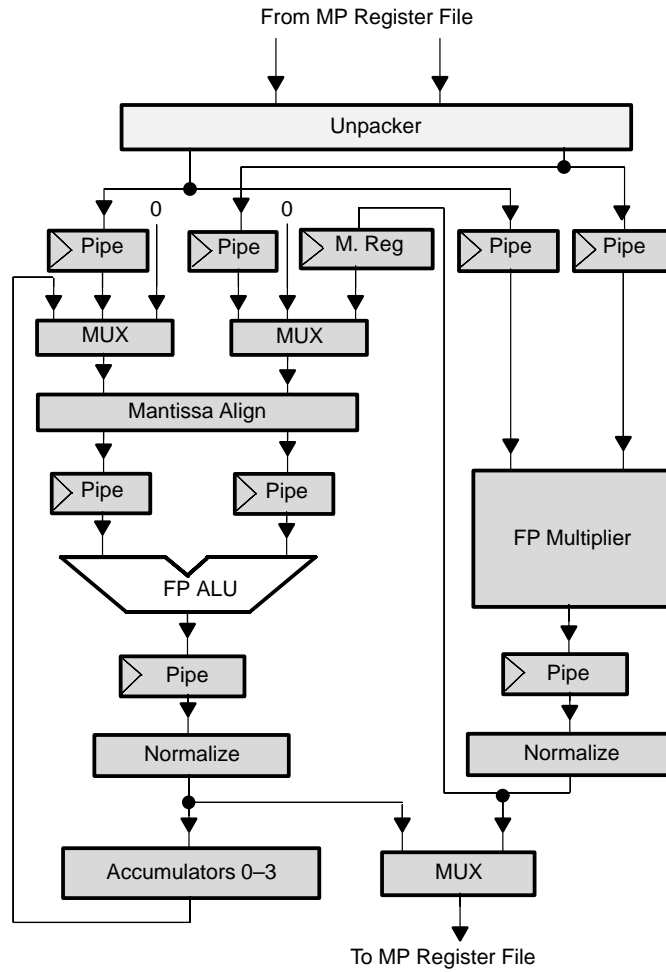
Features of the MP floating-point unit include:

- ☐ IEEE-754 floating point
  - Hardware-exception handling
- ☐ FP add unit with double-precision ALU
  - One-cycle adds/subs/compares (single and double) and conversions
  - Six-cycle single- and 20-cycle double-precision divide
  - Nine-cycle single- and 26-cycle double-precision square root
- ☐ Floating-point multiply unit performs all multiplies (integer and floating-point), divides, and square roots
  - One-cycle single-precision multiply
  - Four-cycle double-precision multiply
- ☐ Pipelined—can start a new instruction every cycle
  - Three-stage pipeline
  - Register file scoreboard prevents "races"
- ☐ Vector FP for 120-MFLOP operation
  - Parallel multiply, add, and 64-bit load (p++) in one cycle
  - Four double-precision accumulator registers support pipelining
  - Supports matrix multiplies, DCTs, and FFTs
- ☐ FP status and interrupt-enable registers
  - MP's test-and-branch instructions access FP status

Figure 11–2 shows a block diagram of the 'C8x MP floating-point unit.



Figure 11–2. TMS320C8x MP Floating-Point Unit



## 11.5 TMS320C8x Parallel Processing Advanced DSPs (PP)

The parallel processing advanced digital signal processors (PPs) provide much of the 'C8x's performance. The PPs are designed to perform digital signal processing along with bit-field and multiple-pixel manipulation. These processors have advanced features that are not found in any other DSP or general-purpose processor and can perform in excess of ten RISC-like operations in each cycle.

In order to specify the multiple parallel operations that the PPs can perform, a wide instruction word of 64 bits is used. The instruction has fields that independently control the data unit and the two address units. All instructions execute in a minimum of a single cycle.

Each PP has a register file of 44 user-visible registers. All registers can be the source or destination of ALU or memory operations. The register set is divided into files according to each register's function. The PP features:

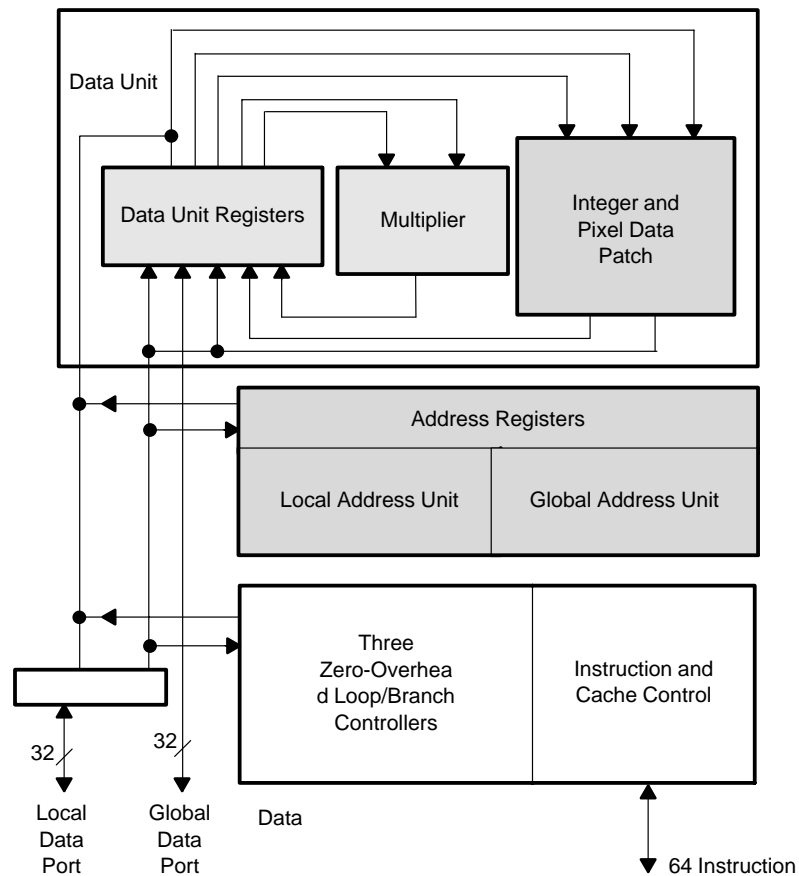
- ☐ Three-input ALU with mixed arithmetic and Boolean operations
  - Can perform masking at the same time as an add or subtract
- ☐ Flexible data path feeding 3-input ALU
  - Fast bit and file processing
- ☐ Address data paths can be used for general-purpose arithmetic
- ☐ Byte/halfword multiple arithmetic
  - Single instruction stream, multiple data stream (SIMD) processing within each processor
  - Better handling of pixels and Z-buffers than in other DSPs or general-purpose processors
- ☐ Eight primary data registers, d0 to d7 (D registers), that can perform up to seven reads and four writes
  - Two multiplier sources, three ALU sources, one multiplier result, one ALU result, and three LD/ST/MOVE
- ☐ Splittable multiplier for fast pixel path
  - Any D register can be used on a multiply-with-parallel-add
- ☐ Three levels of zero-overhead loops
- ☐ Conditional operations (for ALU, load/store, and/or register source)

Additional features include:

- ☐ Two address units
  - Up to two memory operations per cycle
- ☐ Single-cycle multiplier
  - One 16-bit or two 8-bit results per cycle
- ☐ Splittable three-input ALU
  - Multiple operations in each pass
  - Up to four 8-bit results per cycle
- ☐ Pixel and bit field hardware

Figure 11–3 shows a block diagram of the 'C8x PP.

Figure 11–3. TMS320C8x Parallel Processing Advanced DSPs (PP)



## 11.6 TMS320C8x PP Data Unit

The data unit has two data paths; each data path has its own set of hardware that functions independently of the other data path.

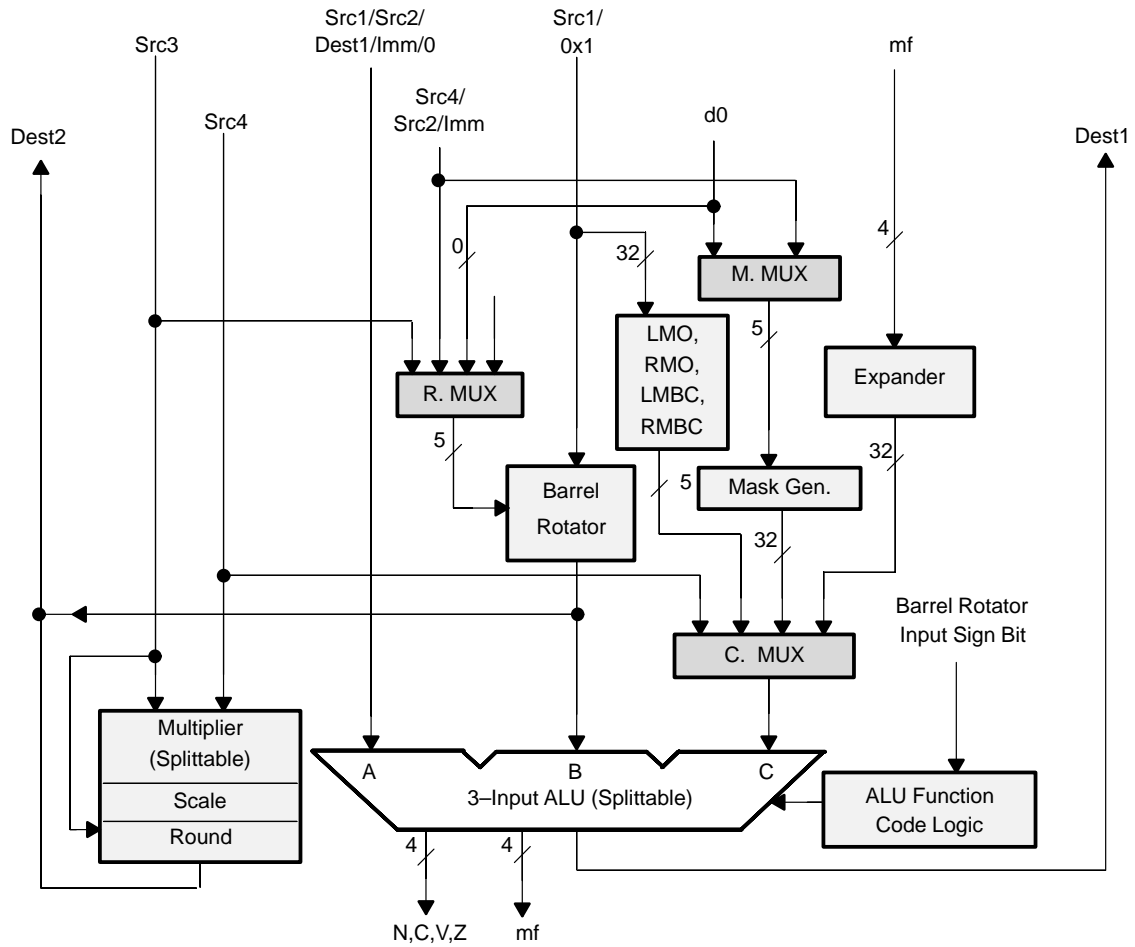
The ALU data path includes a barrel rotator, mask generator, 1-bit to n-bit expander, and a 3-input ALU that can combine the mask or expander output with register data to create over 2000 different processing options. The 3-input ALU can perform 512 logical and/or mixed logical and arithmetic operations that support masking or merging and addition/subtraction in a single pass. The ALU can also be split to perform multiple 8-bit or 16-bit operations in parallel.

The PP data unit features are:

- ☐ Three-input ALU (512 operations)
  - Mixed arithmetic and Boolean in one cycle (mask and add/sub in one pass)
  - Mask/merge and field processing
  - Splittable for multibyte operations
- ☐ 16-bit x 16-bit multiplier (32-bit results)
  - Rounding for DCT accuracy
  - Splittable into two 8-bit- x 8-bit multipliers (16-bit results)
- ☐ Flexible data path
  - Barrel rotator
  - Mask generator
  - N-to-1 and 1-to-N translations via mf register
  - Left/rightmost one and bit-change
- ☐ 44 user-visible registers
  - Any register can be operand of ALU
- ☐ Eight D registers
- ☐ Conditional operations
  - Conditional choice of register pair source
  - Conditional save of result
  - Add ... => instruction and data cache control
  - 2K-byte instruction cache ('C80), 4K-byte instruction cache ('C82)
  - 2K-byte instruction parameter RAM
  - 8K-byte data RAM

Figure 11–4 shows a block diagram of the 'C8x PP data unit.

Figure 11–4. TMS320C8x PP Data Unit



## 11.7 TMS320C8x Transfer Controller (TC)

The transfer controller (TC) is a combined DMA machine and memory interface that intelligently queues, prioritizes, and services the data requests and cache misses of the MP and the PPs. The transfer controller interfaces directly with the on-chip SRAMs. Through the TC, all of the processors can access the system external to the chip. In addition, data-cache or instruction-cache misses are automatically handled by the TC.

Data transfers are specifically requested by the PPs or the MP in the form of linked-list packet transfers, which are handled by the TC. These requests allow multidimensional blocks of information to be transferred between a source and destination, either of which can be on-chip or off-chip. Packet-oriented data transfers offer compatibility with several local area network standards, such as ATM.

The TC performs:

- ☐ Cache fills and writes
- ☐ Direct loads and stores from/to off-chip memory through DEA request
- ☐ Block movement of data through packet transfers
- ☐ Refresh and SRT (shift register transfer) cycles needed to maintain DRAMs and VRAM capture/display buffer, respectively

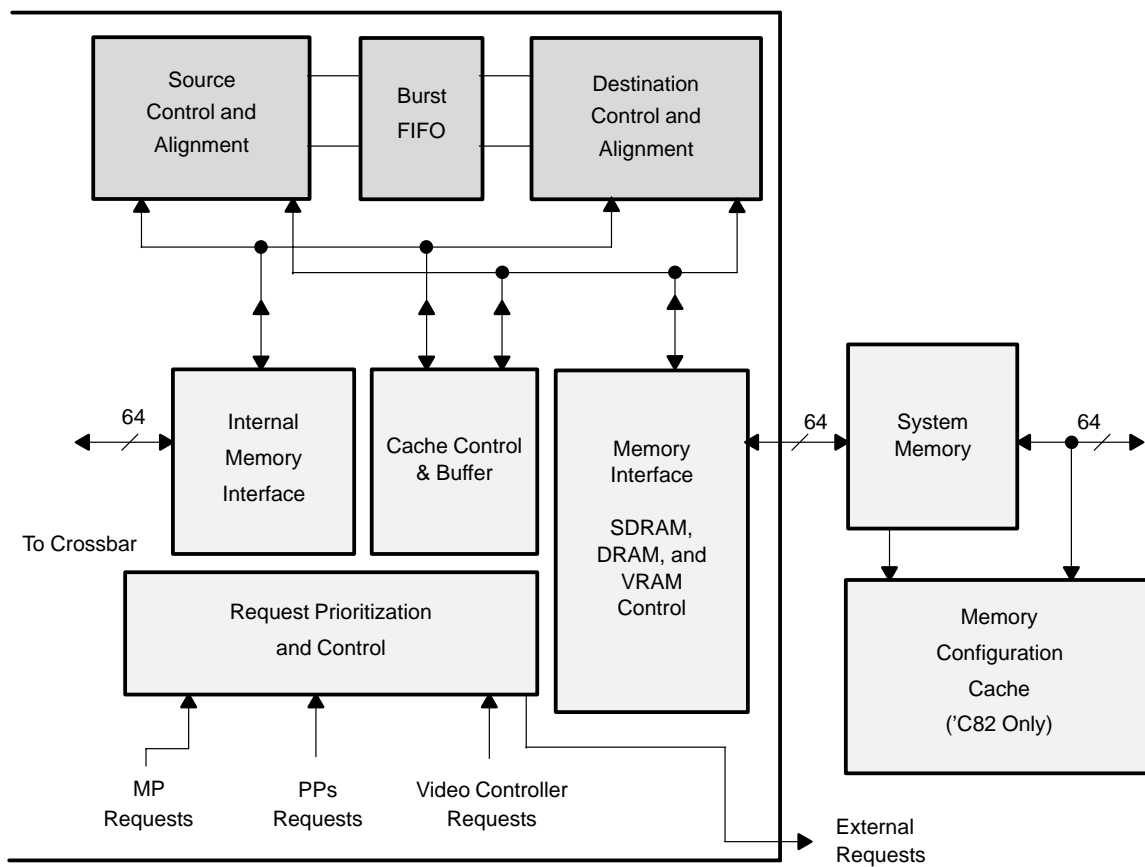
Features of the TC include:

- ☐ 400 Mbytes/s external bandwidth
- ☐ Direct RAM, VRAM, SRAM, and SDRAM control, EDO DRAM ('C82)
- ☐ Dynamic bus sizing (64, 32, 16, or 8 bits)
- ☐ Packet transfers controlled autonomously by transfer controller
- ☐ Linear x/y addressing
  - Independent source and destination
  - Automatic byte alignment
- ☐ Intelligent request
  - Queuing and prioritization

The 'C82 TC includes a memory configuration cache that consists of six 32-bit words that describe the properties of the six most recently-used banks of memory. The cache automatically loads configuration words each time an access to a new bank is made and it can be locked into a set high or low priority. The configuration cache reduces the number of pins necessary in the 'C82 and in support chips.

Figure 11–5 shows a block diagram of the 'C8x TC.

Figure 11–5. TMS320C8x Transfer Controller (TC)



## 11.8 TMS320C80

The 'C80, the first member of the TMS320C8x generation, is a 40-, 50-, or 60-MHz, CMOS multiprocessor DSP designed for high-performance processing. The 'C80 architecture combines a floating-point unit and a RISC processor to provide a multiprocessor environment on a single device.

The 'C80 combines four 32-bit parallel processors (PPs) with a 32-bit master RISC processor, a video controller, a transfer controller, and 50K bytes of SRAM on a single chip. Each PP is capable of many parallel operations per cycle. The PPs perform pixel/field processing as well as digital signal processing. The RISC processor has a 120-MFLOPS IEEE-754 floating-point unit.

The 'C80 has a 16- or 20-ns cycle time, executes at over 2 BOPS, and achieves 400M bytes/s of data to off-chip memory.

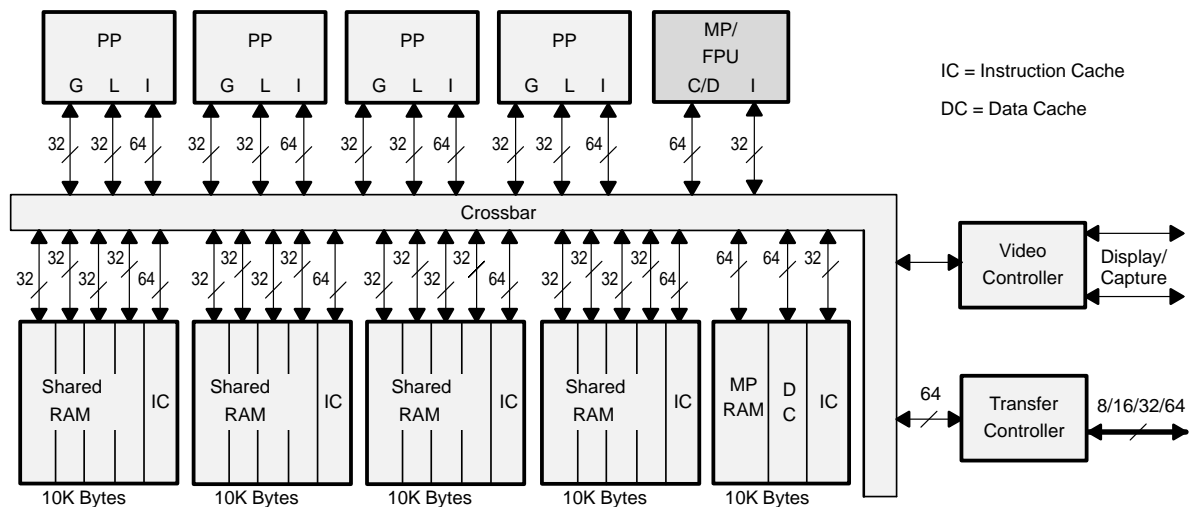
The 'C80's on-chip RAM supports many parallel accesses per cycle. A cross-bar switch supports up to 4.2G bytes/s transfer rates: 2.4G bytes/s of data and 1.8G bytes/s of instructions. 32K bytes of RAM can be shared by all processors and the transfer controller. The video controller supports any display or capture resolution. Other features of the 'C80 include:

- ☐ Transfer controller (supports multidimensional packet transfers)
  - 400 Mbytes/s on- and off-chip memory transfers
  - 4G-byte memory address space
  - Access to 8-, 16-, 32-, or 64-bit SRAM, VRAM, DRAM, SDRAM
  - Off-loads memory manipulations from the processors
- ☐ 0.5- $\mu$ m CMOS technology
- ☐ Efficient packaging: 305 ceramic pin grid array (CPGA)

Figure 11–6 shows a block diagram of the 'C80.



Figure 11–6. TMS320C80 Block Diagram



## 11.9 TMS320C80 Video Controller (VC)

The video controller is included only in the architecture of the 'C80 and is the interface between the device and image-capture display systems.

The 'C80 has two sets of frame timing counters and registers. The video controller keeps track of horizontal and vertical synchronization and blanking timing, as well as supporting a two-dimensional border region. Each counter has its own asynchronous clock inputs. These synchronization signals can be individually set up as outputs (for display) or inputs (for capture).

The shift-register transfer (SRT) controller has comparators that cause shift-register transfer cycles for VRAMs or cause packet transfers for DRAM-based display memories.

Four main sections make up the video controller:

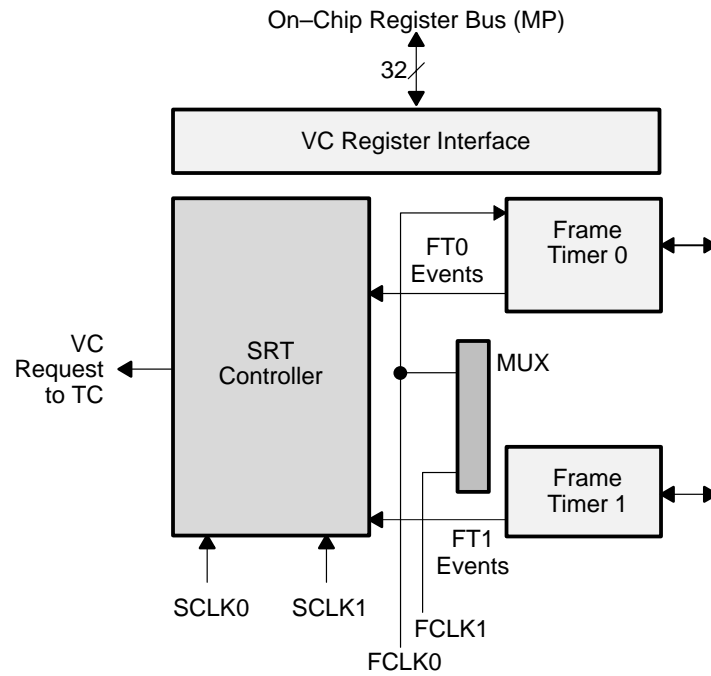
- ☐ Frame timers
- ☐ Serial register transfer controller
- ☐ Register interface
- ☐ Multiplexer

Features of the video controller include:

- ☐ Two identical frame timers
  - Can be used for display or capture
  - Each has an asynchronous clock
  - Generate fully-programmable horizontal, vertical, blank, and border timing
- ☐ SRT controller
  - Controls two display/capture regions
  - Has VRAM shift register transfer control
  - Generates timer interrupts to the MP
  - Generates timer packet requests to the TC

Figure 11–7 shows a block diagram of the 'C80 VC.

Figure 11–7. TMS320C80 Video Controller (VC)



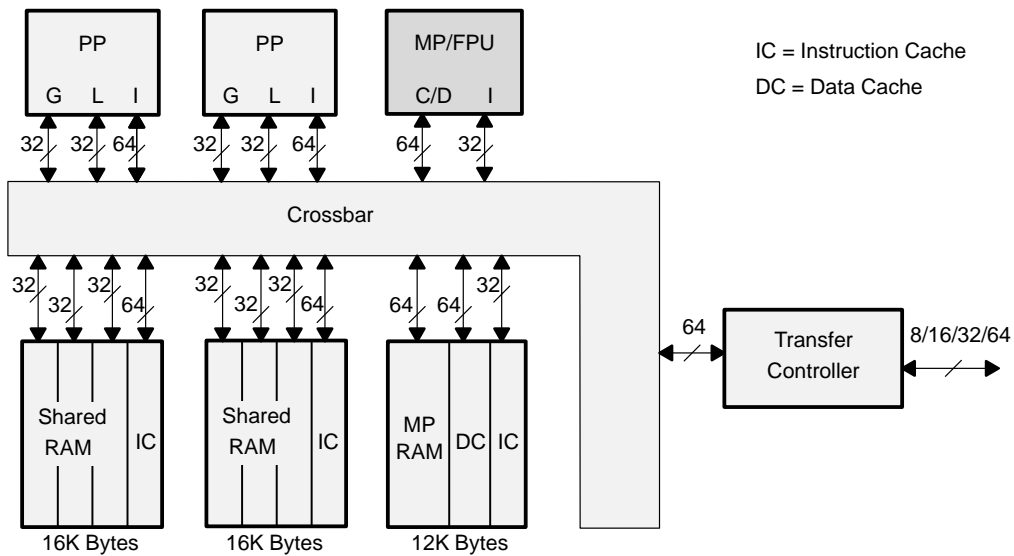
## 11.10 TMS320C82

The 'C82 is a 50-MHz DSP that combines two parallel-processing advanced DSPs (PPs) with 64-bit instructions and 32-bit fixed-point data. Each PP is capable of many parallel operations per cycle. The PPs perform pixel/field processing as well as digital signal processing. The RISC processor has a 100-MFLOPS IEEE-754 floating-point unit. The 'C82 is capable of executing at up to 1.5 BOPS, with a 20-ns cycle time.

The 'C82's on-chip RAM supports many parallel accesses per cycle. A cross-bar switch supports up to 2.6-Gbytes/s transfer rates: 1.6 Gbytes/s of data and 1.0 Gbytes/s of instructions. 32K bytes of RAM can be shared by all processors and the transfer controller. Other features of the 'C82 include:

- ☐ Transfer controller (supports multidimensional packet transfers)
  - 400 Mbytes/s on- and off-chip memory transfers
  - 4G-byte memory address space
  - Access to 8-, 16-, 32-, or 64-bit SRAM, DRAM, SDRAM, and EDO DRAM
  - Off-loads memory manipulations from the processors
  - On-chip memory configuration cache consisting of six 32-bit words to describe the properties of six banks of external memory
- ☐ 0.5- $\mu$ m CMOS technology
- ☐ Efficient packaging: 352 ball grid array (BGA) package

Figure 11–8. TMS320C82 Block Diagram



## 11.11 Tools for TMS320C8x

For information about the code generation and debugging tools available for the 'C8x devices, refer to Chapter 15, *Code Generation Tools*, and Chapter 16, *System Integration and Debugging Tools*. Table 2–14 and Table 2–15 in Chapter 2, *Selection Guide*, provide part numbers and host system information.

# TMS320AVxxx Generation

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Texas Instruments developed the TMS320AVxxx product generation for the new market. Current products generally available are included in this chapter. For information on other DSP developments for digital audio and video applications, please contact your local TI Sales Representative.

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## **12.1 Introduction**

The transition from analog to digital video storage and transmission has created a large demand for products conforming to open standards. Audio and video compression standards such as Moving Picture Expert Group (MPEG), broadcast transmission standards such as DVB, and demodulation standards such as Quality Assessment Measurement (QAM), QPSK, and VSB demand high-performance DSP technology.



## 12.2 TMS320AV110

The 'AV110 MPEG audio decoder implements the International Standards Organization - Moving Picture Expert Group (ISO-MPEG) audio decompression algorithm in a single chip. The 'AV110 accepts an MPEG-compliant compressed audio stream at any of the valid MPEG data and sampling rates and produces decompressed audio output in either 16- or 18-bit serial pulse-code modulation (PCM) format. The PCM data stream is suitable for direct input to most commercially available digital-to-analog converters (DACs).

Both MPEG layers 1 and 2 are implemented. The 'AV110 decodes a single monaural channel, two independent mono channels, stereo channels, and joint stereo channels. The compressed audio can be input either as MPEG audio frames or as the full-multiplexed system stream containing multiple audio and/or video packets. The input can be at the actual bit rate or it can be in bursts at up to 15 Mbps.

Compressed audio can be input in either bit-serial or byte-parallel formats. An eight-bit microprocessor interface is provided for control and status register access with maskable interrupts for the critical status and error flag registers.

While the 'AV110 operates as a single, standalone decoder, provision also is made for using a  $256K \times 4$  DRAM device if buffering of the audio stream is required. With the external memory in place, up to one second of audio can be buffered for synchronization purposes. The external memory also allows the employment of more robust error-concealment techniques if cyclic-redundancy check (CRC) or synchronization errors are detected by the decoder.

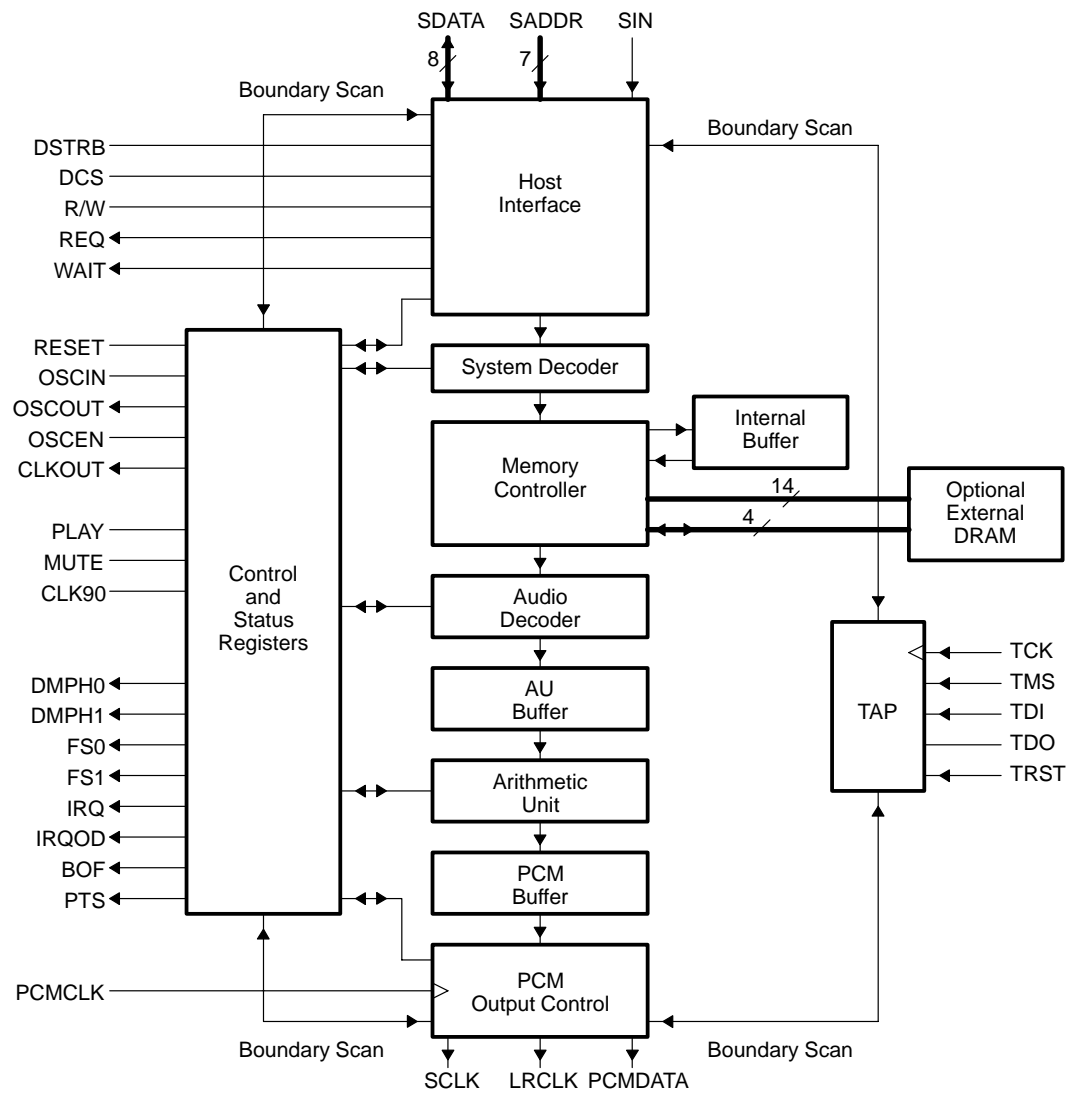
The 'AV110 is implemented in Texas Instruments enhanced performance implanted CMOS (EPIC™) submicron, triple-level-metal technology.

Features of the 'AV110 are as follow:

- ☐ Has single-chip ISO-MPEG (layers 1 and 2) audio decoder
- ☐ Decodes mono, dual, stereo, and joint-stereo modes
- ☐ Supports all MPEG sampling and data rates, including free format
- ☐ Controls stereo level
- ☐ Allows input of MPEG audio frames or full-multiplexed MPEG system stream
- ☐ Accepts compressed audio at up to 15-Mbps burst rate
- ☐ Accepts bit-serial or byte-parallel compressed data input
- ☐ Outputs 16- or 18-bit serial PCM direct interface to most serial DACs

- ☐ Has an 8-bit microprocessor control interface
- ☐ Supports up to a one-second audio delay for audio/video synchronization (with optional external DRAM)
- ☐ Provides low-power, submicron CMOS technology; fully TTL compatible
- ☐ Packaged in a small-footprint, 120-pin plastic quad flat pack (PQFP)

Figure 12–1. TMS320AV110 Block Diagram



## 12.3 TMS320AV120

The 'AV120 is a low-cost, stand-alone MPEG audio decoder (see Figure 12–2). It implements the ISO-MPEG audio decompression algorithm for layers 1 and 2. MPEG-compliant audio data streams at any of the valid MPEG data and sampling rates are accepted, producing decompressed PCM audio output. Mono, dual, stereo, and joint-stereo modes are supported. The serial-output data stream is suitable for direct input to most commercially available 1-bit DACs.

The 'AV120 design produces a simple “plug and play” audio decoder that does not require a host microprocessor for initialization and/or operation. The input is in MPEG audio-frame format with provisions for audio/video synchronization. It is a single-chip solution with no provision or need for external buffer memory. The input data rate should match the actual compressed audio bit rate, although the 'AV120 has an input buffer to absorb short-term input bit rate variations. Ancillary data in the bit stream is recovered and output serially. When the compressed audio data is at the actual bit rate, a pulse-width-modulated (PWM) error signal is generated if the PCM output clock is not at the required frequency.

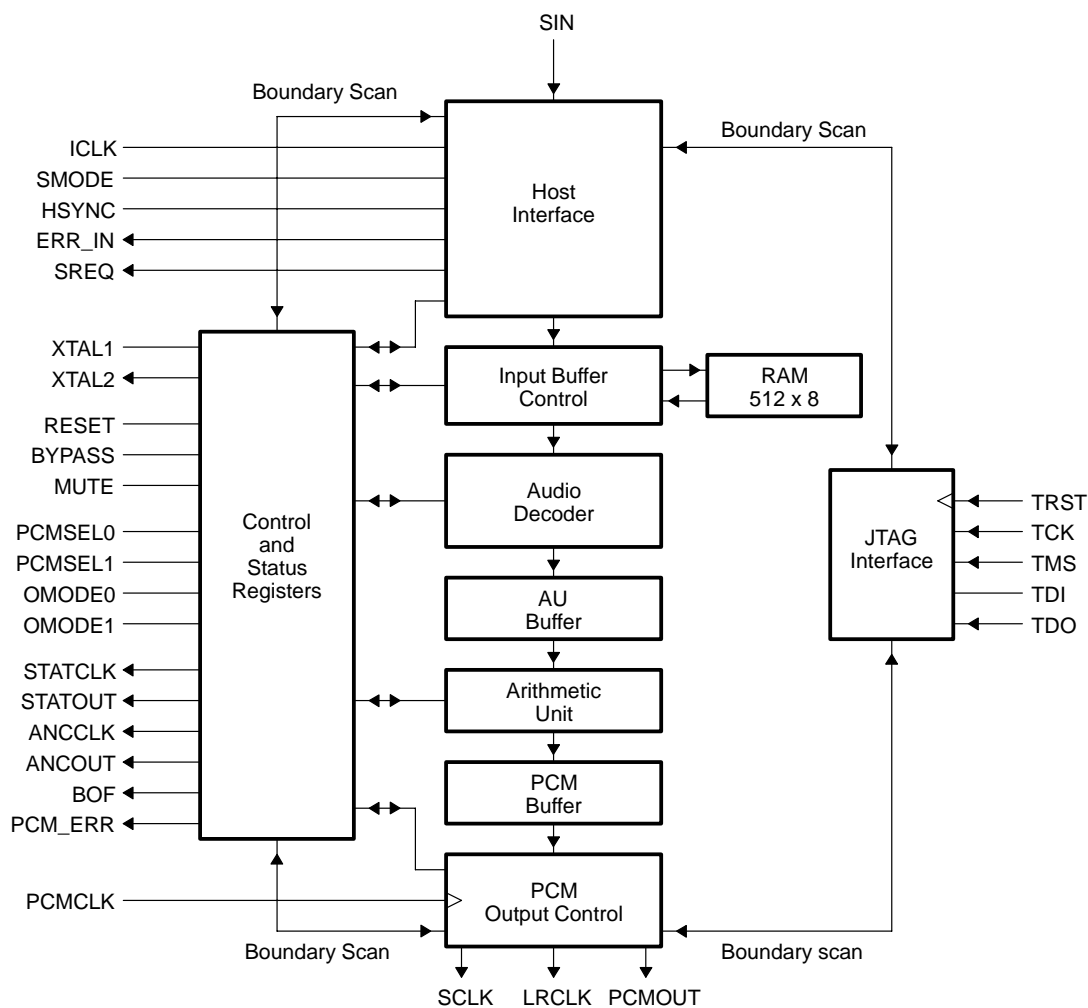
The decoded sampling rate, stereo mode, error status, and de-emphasis information is available in the serial status register synchronously with the beginning of the associated PCM data frame. The complete MPEG frame header also can be read from the chip.

In systems where audio/video synchronization is required, the 'AV120 accepts the system SCR and the audio PTS information and synchronizes the audio output to these time stamps.

Features of the 'AV120 are as follow:

- ☐ Has single-chip ISO-MPEG (layers 1 and 2) audio decoder
- ☐ Decodes mono, dual, stereo, and joint-stereo modes
- ☐ Supports all MPEG sampling and data rates
- ☐ Does not require a host microprocessor for initialization or operation
- ☐ Accepts SCR and audio PTS and provides automatic synchronization
- ☐ Provides status information at beginning of every frame
- ☐ Interfaces directly to the TMS320AV220 video decoder
- ☐ Accepts hardware frame synchronization input
- ☐ Supports 16- and 18-bit PCM data
- ☐ Recovers and outputs all ancillary data
- ☐ Provides PCMCLK-to-input-data-rate synchronization signal
- ☐ Compliant with IEEE standard 1149.1 (JTAG)
- ☐ Fabricated using low-power submicron CMOS technology: fully transistor-to-transistor logic (TTL) compatible

Figure 12–2. TMS320AV120 Block Diagram



## 12.4 TMS320AV220

The 'AV220 is a video CD MPEG-1 decoder (see Figure 12–3). It is designed to operate with the 'AV120 MPEG audio decoder to implement a complete audio and video decoder solution. It also interfaces directly with the 'AV420 National Television Standards Committee (NTSC) encoder.

The 'AV220 is fully compatible with the new video-CD and karaoke standards, and is targeted at low-cost, consumer-oriented applications. All components required to accept and decode the multiplexed MPEG-1 system stream are included on the chip, including the logic necessary for audio/ video synchronization.

The 'AV220/120 chipset can interface to a host system through a generic 8-bit microprocessor interface. Glueless interface is possible to a Z-80, H-8, or similar processor.

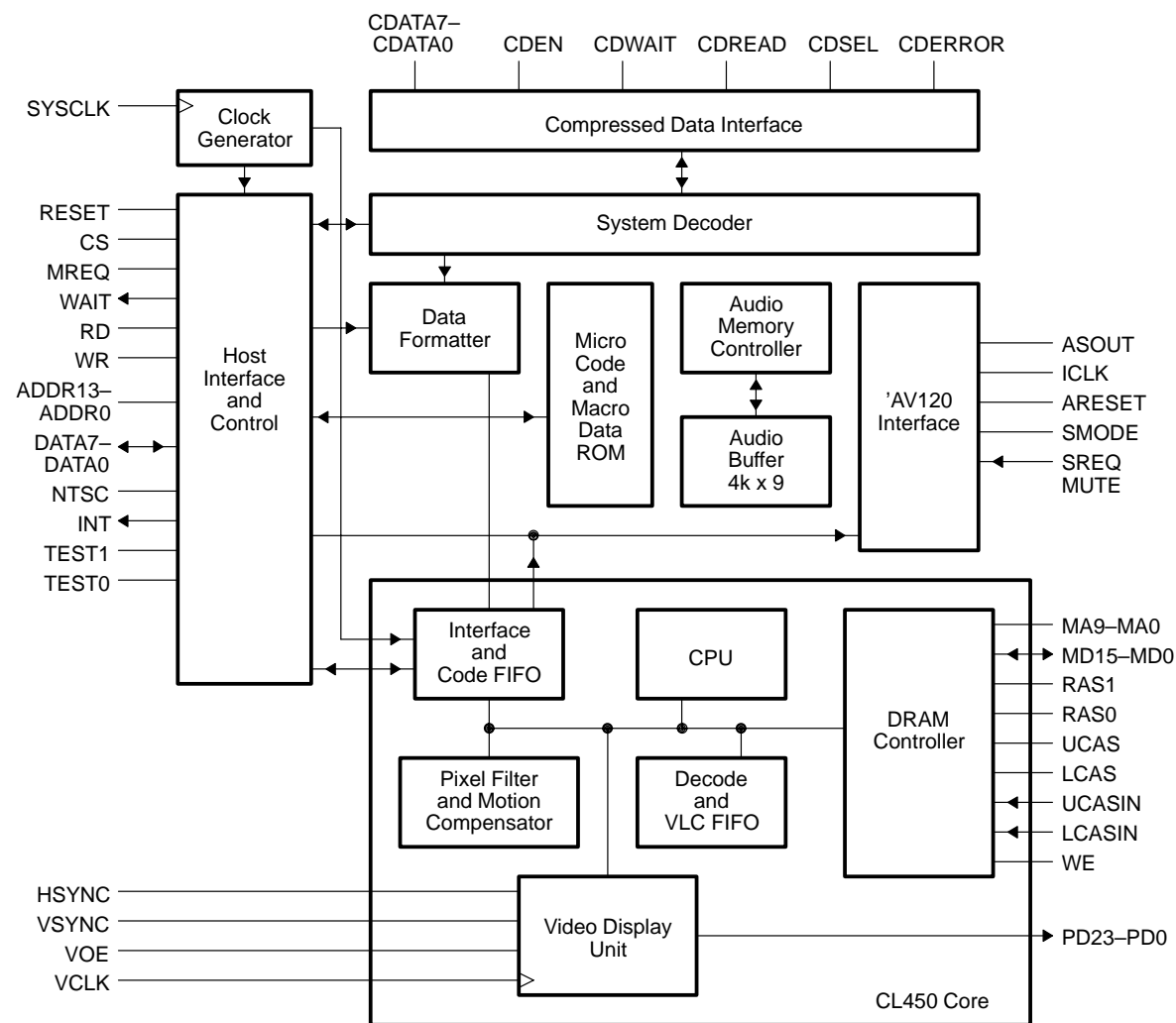
The compressed MPEG-1 data-stream interface is through an 8-bit port that can connect directly to either of the popular Sanyo (LC8950 or LC8951) or Sony (CXD1186BQ) CD-ROM decoders.

Features of the TMS320AV220 are as follow:

- ☐ Provides a single-chip ISO-MPEG video decoder
- ☐ Interfaces directly to the TMS320AV120 MPEG audio decoder and the TMS320AV420 NTSC encoder
- ☐ Based on the C-Cube CL450 core
- ☐ Stores microcode in an on-chip ROM
- ☐ Provides an integrated system decoder: the chip accepts the multiplexed MPEG-1 system data stream
- ☐ Supplies an on-chip audio-input buffer
- ☐ Provides audio/video synchronization logic
- ☐ Complies fully with all requirements of the MPEG standard (ISO CD 11172)
- ☐ Performs real-time decoding of SIF-resolution bitstreams (352 x 240 pixels at 30 Hz or 352 × 288 pixels at 25 Hz)
- ☐ Performs real-time horizontal pixel interpolation and frame duplication to produce output formats of 704 × 240 pixels at 60 Hz or 704 × 288 pixels at 50 Hz
- ☐ Converts decompressed video to red, green, blue (RGB) color-space automatically, optional YCbCr output

- ☐ Supports NTSC and phase alternate line (PAL) video-output timing formats
- ☐ Interfaces to Z-80, H-8, or similar processors and DRAM with no external logic
- ☐ Requires only 4M bits of 80-ns DRAM to decode SIF-resolution MPEG bit streams
- ☐ Provides video CD functions: fast forward and reverse, still picture, direct DRAM

Figure 12–3. TMS320AV220 Block Diagram





## 12.5 TMS320AV411

The 'AV411 is a digital NTSC/PAL encoder targeted toward the television and consumer electronics markets. (For support of the Macrovision anti-copy function, the TMS320AV410 is available to Macrovision licensees.) Multiple input and output formats are available to the user. Digital RGB and luminance [Y], chrominance-blue [Cb], chrominance-red [Cr] (YCbCr) are two common input options. Y and CbCr can be demultiplexed and delivered through two separate data ports (according to the CCIR601 specification).

Three on-chip DACs enable three analog-output formats: RGB, Y/C (S-video), or composite. Synchronized signal generation can be performed on- or off-chip. On-chip generation reduces the need for external glue logic, while off-chip generation enables the 'AV410/411 to use the synchronized signal from an external source, such as an MPEG-2 video decoder.

Three DACs enable three output formats (RGB, Y/C or composite) that are selectable by the user. Nine bits provide high-resolution consistent with consumer electronics requirements. Closed-caption encoding is supported. Sixteen colors are available at a given time to be used for various graphics (such as menus) that are overlaid on top of the video. The 'AV411 supports both interlaced and noninterlaced scan.

Key features of the 'AV411 include:

- ☐ Input: RGB or YUV
- ☐ Output: RGB, Y/C (S-video), or composite video
- ☐ On/off-chip synchronized signal generation
- ☐ Closed-caption encoding
- ☐ 16-color overlay with color lookup table for on-screen display
- ☐ Interlaced and noninterlaced operation
- ☐ 100-pin PQFP package

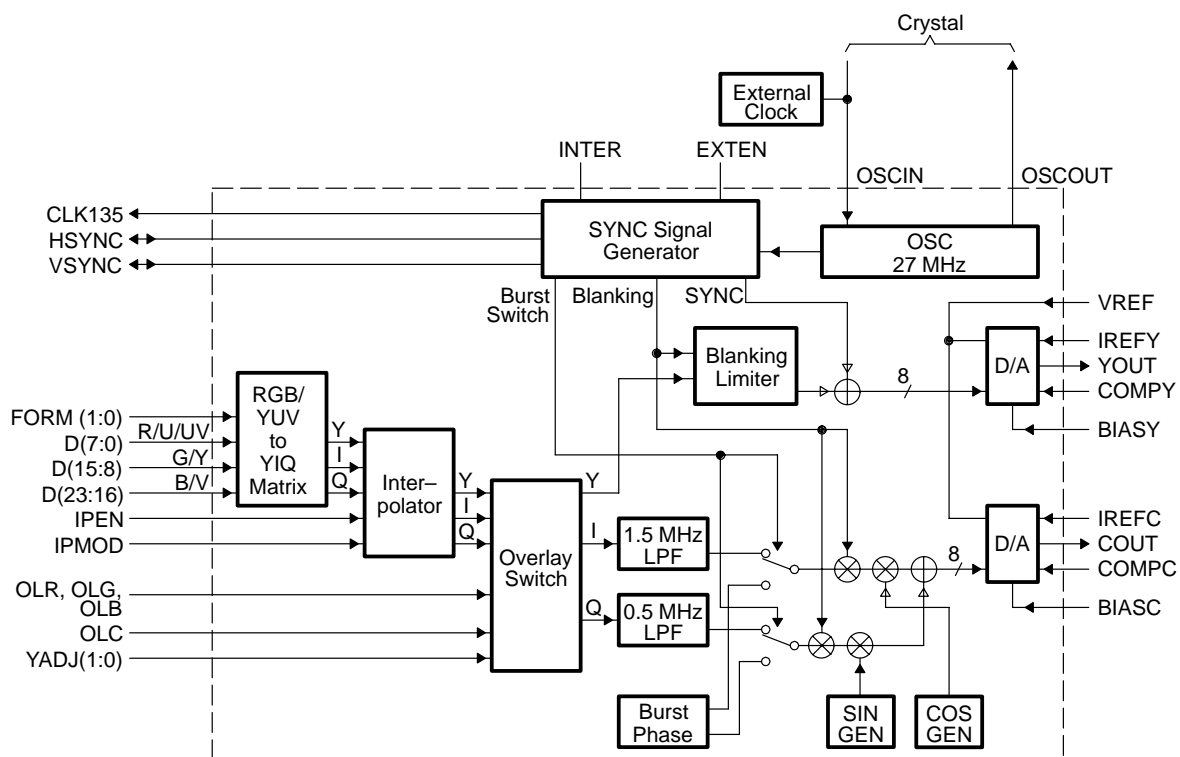
## 12.6 TMS320AV420

The 'AV420 is a video encoder that converts the RGB or YUV pixels to the analog S-video signal using digital signal processing techniques. The pixels are input to the 'AV420 using a 13.5-MHz clock. S-video is output from the 'AV420 on two separate RS170A-compatible analog channels: the luminance (Y) channel and the chrominance (C) channel. The 'AV420 operates in either interlaced or noninterlaced mode. The internal and external synchronization capabilities, vertical-line interpolation, on-screen display, and direct interfacing features provide the 'AV420 video quality and facilitate video system design. Figure 12–4 shows a block diagram of the 'AV420.

The 'AV420 also features:

- ☐ Single-chip digital NTSC encoder
- ☐ Input: RGB, YUV 4:4:4 or YUV 4:2:2
- ☐ Output: S-Video (Y and C)
- ☐ Y and C conform to the RS170A standard
- ☐ On-chip synchronization signal generator circuitry
- ☐ Internal and external synchronization capability
- ☐ Interlaced and noninterlaced operation
- ☐ Vertical-line interpolation for MPEG-1 video
- ☐ Overlay function for on-screen display
- ☐ Direct interface to the 'AV220 video CD MPEG decoder
- ☐ Small-footprint 80-pin PQFP

Figure 12–4. TMS320AV420 Block Diagram



## 12.7 Video CD Chipset

The video CD chipset from Texas Instruments provides a complete integrated circuit solution for full-motion video (FMV) subsystems used in video compact disk applications. TI created the chipset specifically to reduce costs and simplify designs in karaoke CD systems, music players, CD-based computer games, and other video CD applications such as PC-based applications.

Three application-specific DSPs make up the chipset:

- ☐ TMS320AV120 MPEG audio decoder
- ☐ TMS320AV220 video CD MPEG decoder
- ☐ TMS320AV420 digital NTSC video encoder

These three devices, along with a 4M-bit DRAM and a DAC for the audio output, allow you to create an FMV subsystem that turns a traditional audio CD player into a video CD player.

The chipset decodes, decompresses, and synchronizes MPEG audio and MPEG-1 video. It produces 16-bit CD-quality audio, as well as a video signal encoded in the NTSC format used in broadcast TV. The chipset also supports the video features included in the video-CD standard, such as fast forward, reverse, and freeze frame.

### 12.7.1 'AV120 MPEG Audio Decoder

The 'AV120 MPEG audio decoder has the following features:

- ☐ Provides a cost-effective, dedicated implementation of the MPEG Audio algorithm (layers 1 and 2)
- ☐ Has mathematically modeled architecture to minimize silicon and maximize audio quality. CD quality is maintained with no additional quantization noise added
- ☐ Can be used as a standalone MPEG audio decoder, eliminating the need for a host processor
- ☐ Derived from TI's highly successful TMS320AV110 MPEG audio decoder and optimized to reduce cost for video-CD applications

### 12.7.2 'AV220 Video CD MPEG Decoder

The 'AV220 video CD MPEG decoder has the following features:

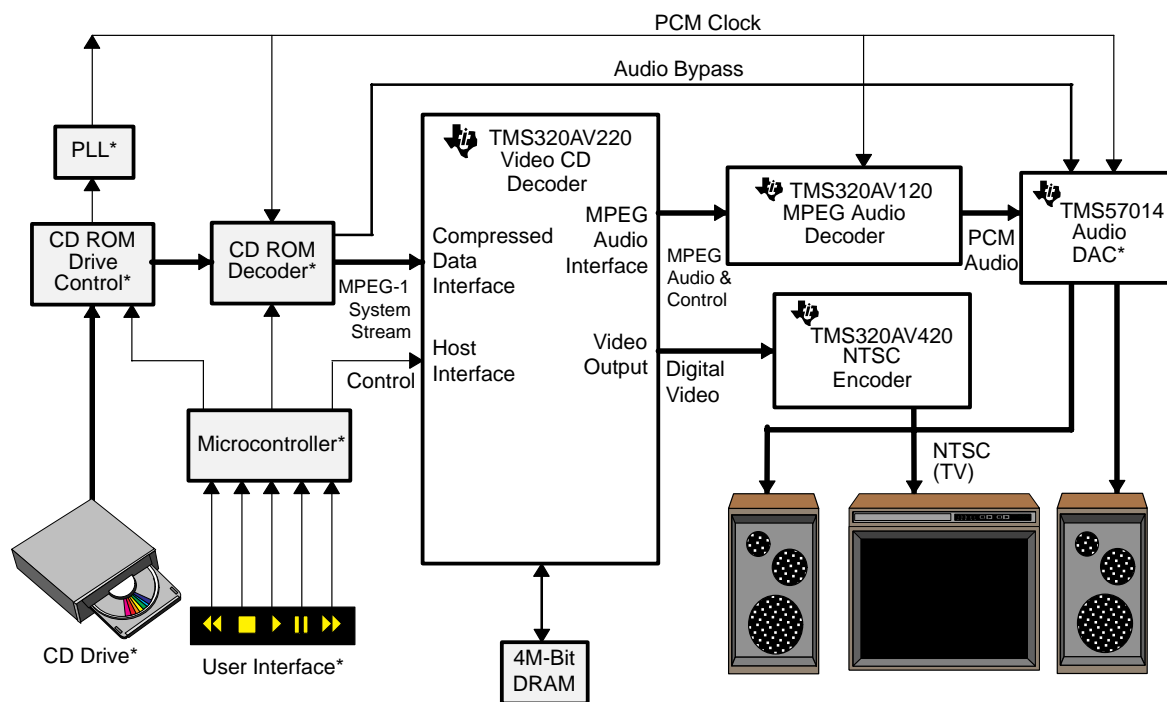
- ☐ Based on C-Cube's LC450 video decoder with integrated features specifically for video CD
- ☐ Integrates MPEG-1 system decoder, audio buffer, and on-chip microcode
- ☐ Synchronizes audio and video outputs without an external host
- ☐ Provides a seamless interface to Sony and Sanyo CD-ROM decoders

### 12.7.3 'AV420 Digital NTSC Video Encoder

The 'AV420 digital NTSC video encoder has the following features:

- ☐ Converts RGB or YUV (luminance chrominance) bitstreams output from the 'AV220 to an analog NTSC signal for TV
- ☐ Vertically interpolates scan lines to create a smooth picture by reducing the noise and flicker that is associated with line-doubled implementations of MPEG-1
- ☐ Generates synchronization timing signals for the 'AV220 video decoder
- ☐ Supports overlays, providing the ability to superimpose both text and graphics on the video display

Figure 12–5. From CD to Video CD With Four Chips



\* Components already included in a CD Player

# Mixed-Signal Products

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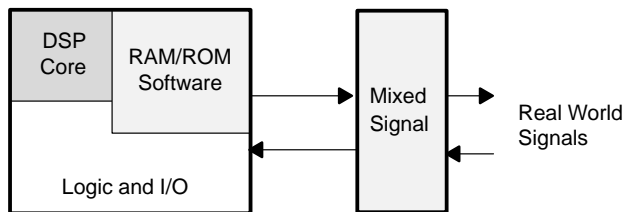
A mixed-signal product is one that provides an interface between the digital and the analog world. Digital signal processing solutions often include a DSP, software, an I/O interface, and mixed-signal products. This chapter describes mixed-signal products that are well suited to providing interfaces for DSP solutions.

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<b>13.2 Mixed-Signal Products and DSP Solutions .....</b>	<b>13-5</b>
<b>13.3 TLS1550/51 Analog-to-Digital Converters .....</b>	<b>13-8</b>
<b>13.4 LC5620 Digital-to-Analog Converter .....</b>	<b>13-9</b>
<b>13.5 TMS57014A Dual 16-/18-Bit Audio DAC .....</b>	<b>13-11</b>
<b>13.6 Analog Interface Circuits (AICs) .....</b>	<b>13-12</b>

## 13.1 DSP Solutions

DSP Solutions (DSPS) are composed of a DSP core, software, system expertise, and a mixed signal product (see Figure 13–1) with peripheral devices such as memory and logic used in embedded systems where the DSP is the primary processor.

Figure 13–1. DSP Solutions



As part of TI's effort to support communications standards worldwide with complete DSP Solutions, TI has developed mixed-signal devices optimized for various uses. Examples of DSP Solutions (see Figure 13–2) include:

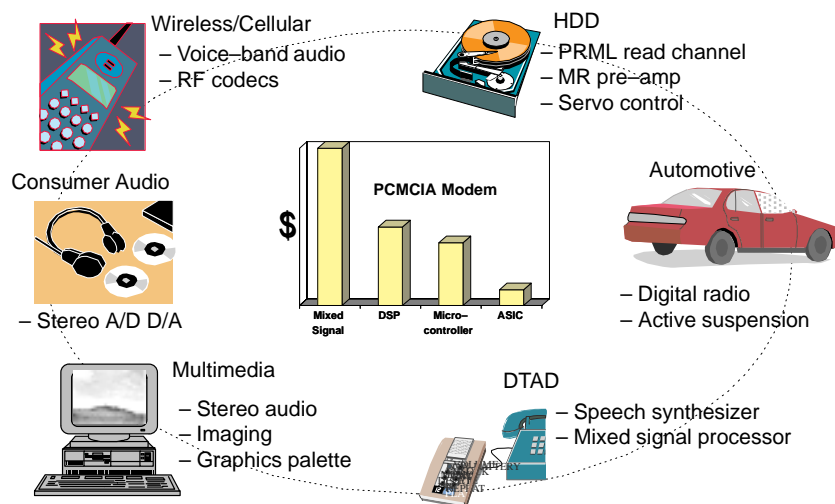
- ☐ Hard disk drives (HDDs)
- ☐ Digital telephone answering devices (DTADs)
- ☐ Automotive audio and suspension systems
- ☐ Multimedia
- ☐ Consumer audio
- ☐ Wireless/cellular

One of the best examples is in the wireless/communications field. Originally, cellular telephones were the size and weight of a brick with talk times of 30 minutes. Cellular phones now fit in your pocket, weigh less than a pound, and have talk times of three hours. All of this has been made possible because of DSPS.

The integration of various functions and features within DSP software and the use of an RF codec and the voice-band audio processor have made this progress possible.



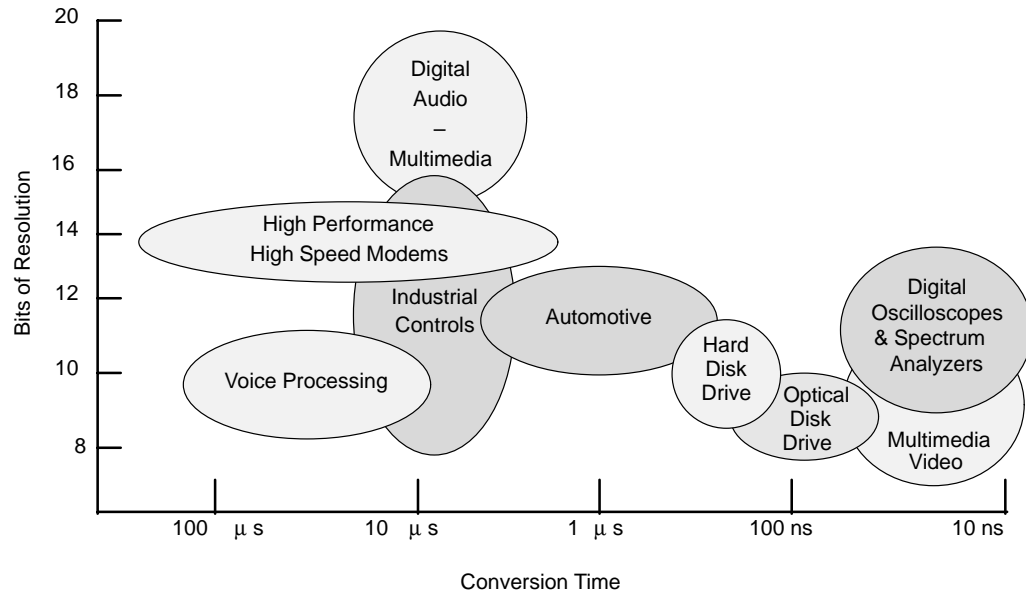
Figure 13–2. Examples of DSP Solutions



Data converters are the classic form of DSP peripherals from the analog point of view. Classic data converters, 10- to 12-bit data converters with a 10- $\mu$ s conversion time, have been around for several years, supplied by Texas Instruments and other manufacturers. The new equipment, driven by DSPs, is pushing this envelope out in two directions. In the video direction, the need is for much greater speed. Bits of resolution are not as important as very high speed, often with conversion time of 10 ns or less.

On the other end of the spectrum, in audio, the ear is a very discriminating instrument so you need very high resolution and speed is not as critical. For the 10- $\mu$ s conversion time, we need 18-bit precision conversion. Figure 13–3 shows the progress being made in data converters. Driven by the pervasion of DSP solutions, this progress spans the range of DSP markets.

Figure 13–3. Mixed Signal Products Enable DSP Solutions



## 13.2 Mixed Signal Products and DSP Solutions

To assist in the selection of analog-to-digital converters (ADCs) and digital-to-analog converters (DACs), two decision trees are provided in this section.

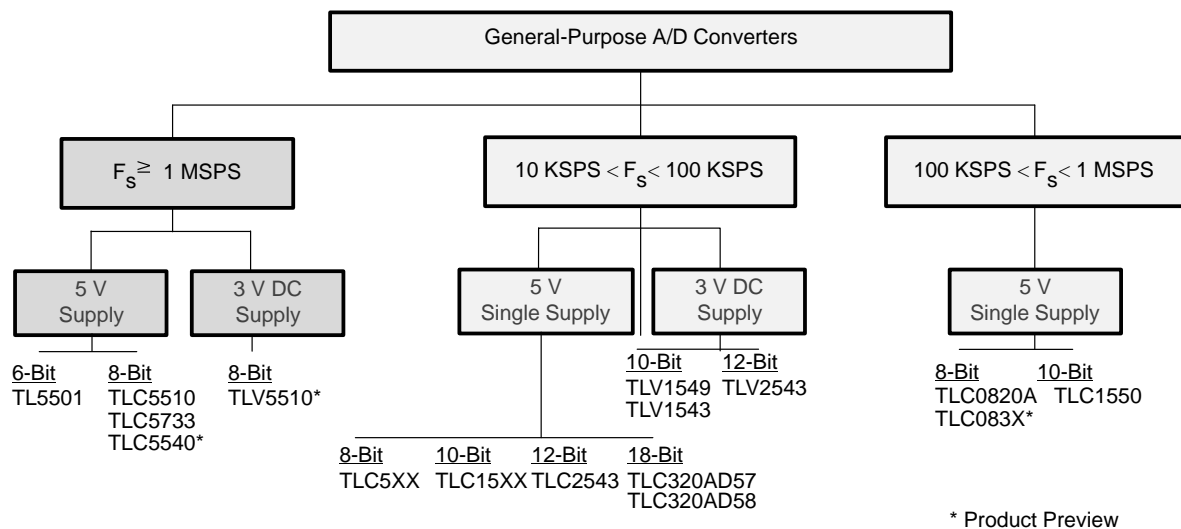
### 13.2.1 ADC Decision Tree

The choice of ADCs is usually driven by two parameters: speed and resolution. Figure 13–4 is designed to help select the appropriate converter for the desired application.

The first decision is to select the required speed from the three ranges in the ADC decision tree. Next, you select the operating voltage. Finally, you select bits of resolution.

In addition to helping you select an appropriate analog-to-digital converter, Figure 13–4 also illustrates the range of general-purpose ADCs.

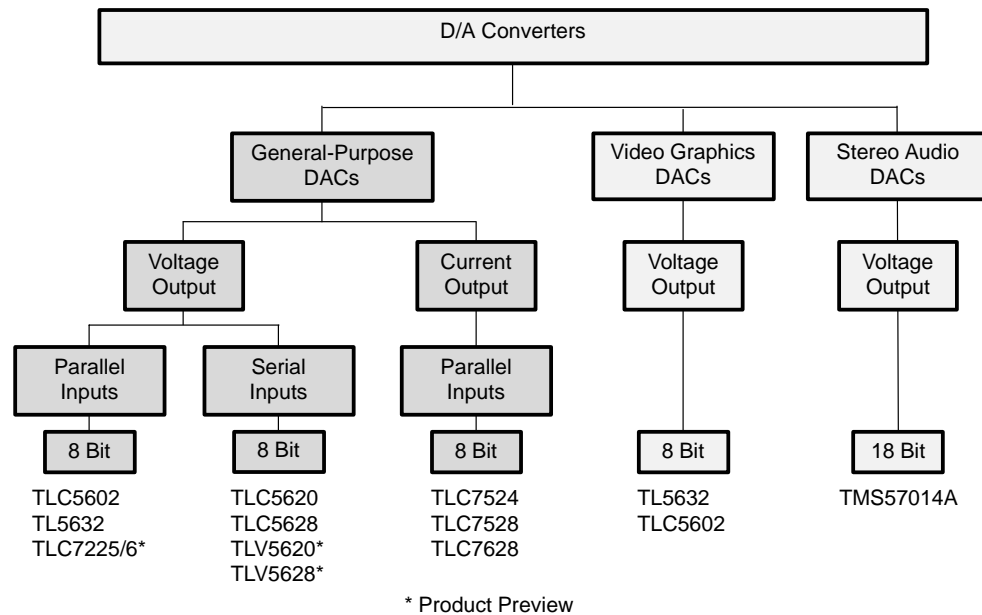
Figure 13–4. ADC Decision Tree



### 13.2.2 DAC Decision Tree

Figure 13–5 presents a DAC decision tree with selection based on general applications (general purpose, video graphics, and stereo). The tree is then divided by output type (voltage or current). Although speed is not specifically stated, the fastest devices generally are located in the video graphics path.

Figure 13–5. DAC Decision Tree

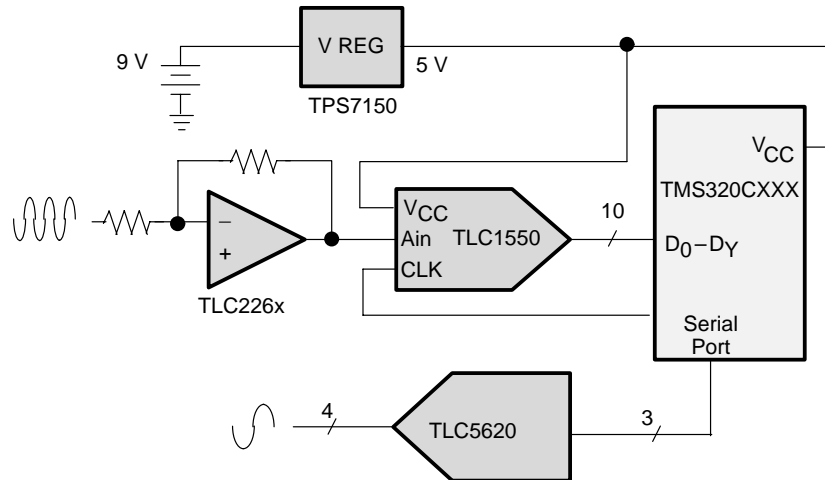


### 13.2.3 DSPS: The Total Solution

A DSP Solution for a closed-loop control system can include both an ADC to sense real-world conditions and a DAC to provide proportional feedback or control. Often the requirements for the DAC and ADC are significantly different, requiring separate components for these functions.

Figure 13–6 shows a TLC1550 ADC, which is a 10-bit single-channel converter interfaced through a parallel port to a TMS320Cxxx DSP. The feedback path is from the DSP through a serial port to a TLC5620, which is a quad eight-bit DAC.

Figure 13–6. An Example of a DSP Solution



### 13.3 TLC1550/51 Analog-to-Digital Converters

The TLC1550 and TLC1551 10-bit, 6- $\mu$ s ADCs are successive approximation converters that offer a high sample rate (166 ksps) at a low-cost. They feature a parallel interface for speed and a selectable external or internal clock for versatility.

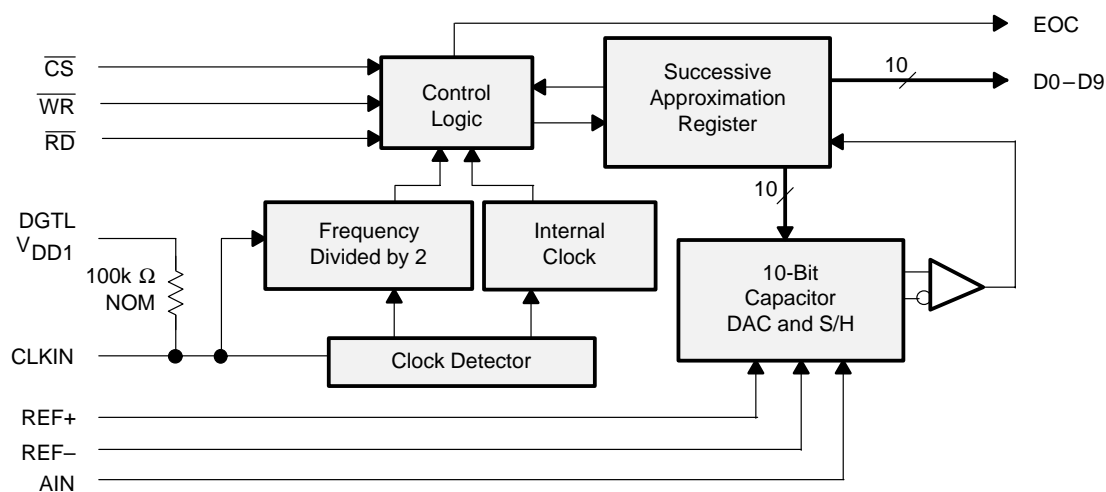
Key features of the TLC1550/51 ADCs include:

- ☐ Single 5-V power supply
- ☐ 3-state outputs
- ☐ Power dissipation of 40 mW maximum
- ☐ Fast parallel processing for DSP and microprocessor interface
- ☐ An external or internal clock
- ☐ DSP/microprocessor interface compatible
- ☐ Conversion time of 6  $\mu$ s
- ☐ 166-ksps sample rate
- ☐ Total unadjusted error
  - TLC1550,  $\pm 0.5$  LSB maximum
  - TLC1551,  $\pm 1.0$  LSB maximum

Applications for these ADCs include vehicle active suspension, data-acquisition systems, DSP front ends, industrial controls, and digital motor control.

Figure 13–7 shows a block diagram of the TLC1550/51 ADC.

Figure 13–7. TLC1550/51 Functional Block Diagram



## 13.4 TLC5620 Digital-to-Analog Converter

The TLC5620 quad DAC has individual reference inputs for each of the four DACs. This feature enables this circuit to be used as four DACs with separate ranges, as programmable gain blocks, or as a combination of both. The flexibility, simple serial interface, and small (14-pin) package make this circuit well suited to many control-feedback-circuit applications.

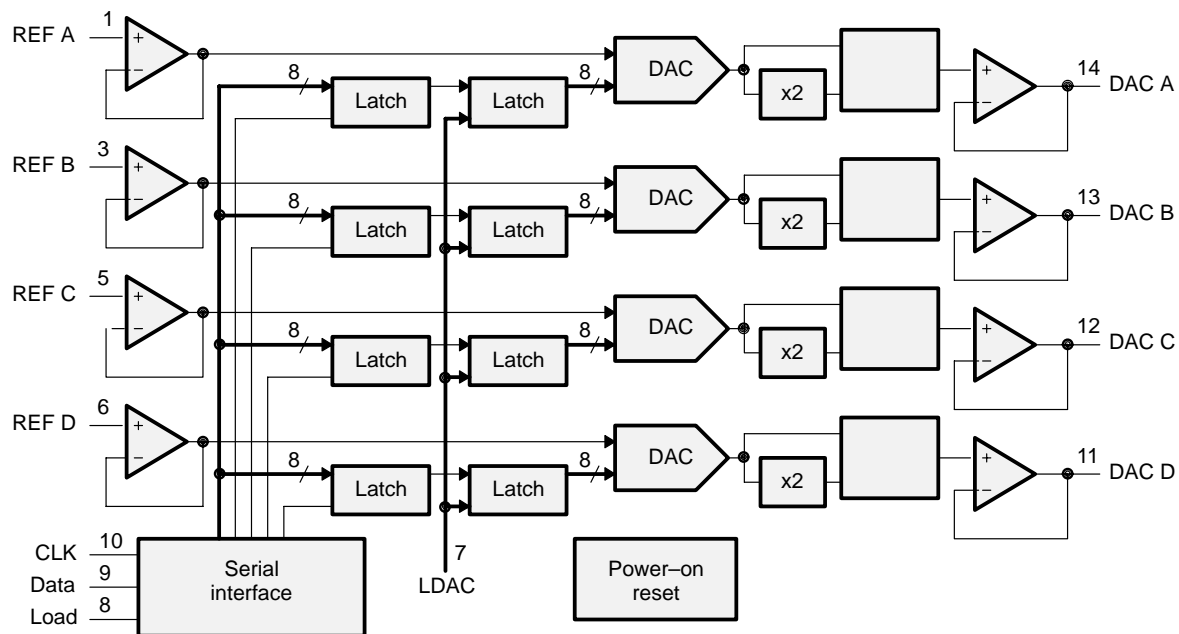
Key features of the TLC5620 DAC include:

- ☐ Four 8-bit voltage output DACs
- ☐ Individual  $V_{REF}$  for each DAC
- ☐ Maximum serial input clock rate of 1 MHz
- ☐ Buffered reference inputs
- ☐ Programmable 1 or 2 times output range
- ☐ Double-buffered registers for synchronous updates
- ☐ Internal power-on reset
- ☐ Low power consumption (20 mW maximum)
- ☐ Characterized operating temperatures:
  - TLC5620C 0° to 70°C
  - TLC5620I -40° to 85°C

Applications for the TLC5620 quad DAC include programmable voltage sources, digitally-controlled amplifiers/attenuators, wireless communications, automatic test equipment, process monitoring and control, and signal synthesis.

Figure 13–8 shows a block diagram of the TLC5620 DAC.

Figure 13–8. TLC5620 Block Diagram





### 13.5 TMS57014A Dual 16-/18-Bit Audio DAC

The TMS57014A is a dual DAC using sigma-delta architecture. This product includes two separate DAC channels with a common serial data interface.

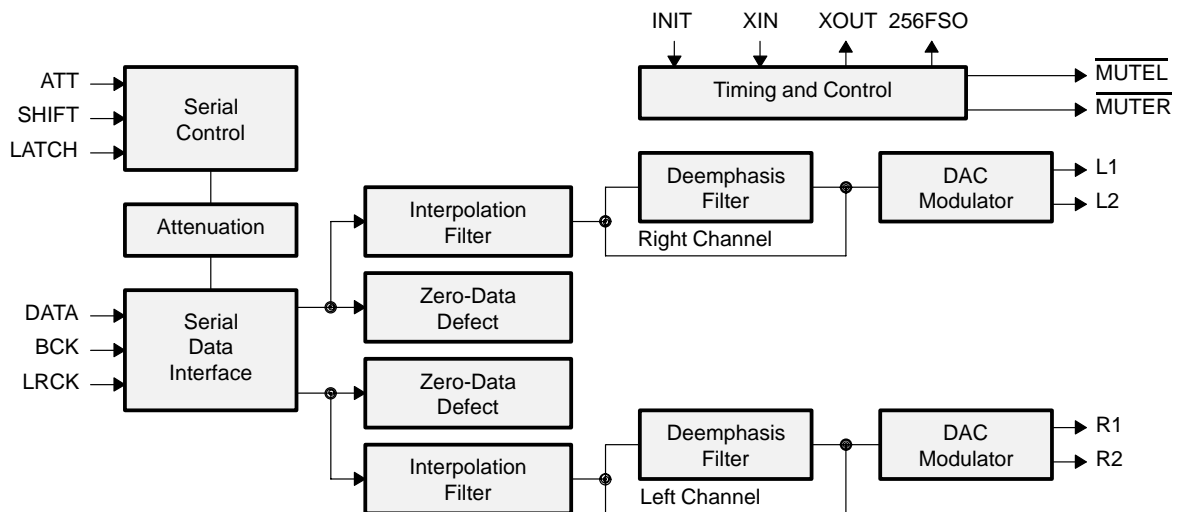
Key features of the TMS57014A include:

- ☐ Sample rates up to 48 kHz
- ☐ Deemphasis filter for 32, 37.8, 44.1, and 48 kHz
- ☐ Digital soft mute to –60 dB
- ☐ Single 5-Vdc supply
- ☐ 18-bit resolution
- ☐ Mute capability with zero data detect flags
- ☐ 2s-complement data format
- ☐ Pulse-width-modulation (PWM) output
- ☐ Serial port interface

Applications of the TMS57014A include digital audio systems, professional quality audio, high-performance audio-speed DAC, waveform generation, and automated test systems.

Figure 13–9 shows a block diagram of the TMS57014A DAC.

Figure 13–9. TMS57014A Dual 16-/18-Bit Audio DAC



## 13.6 Analog Interface Circuits (AICs)

AICs are described in this section, with block diagrams and features of each one.

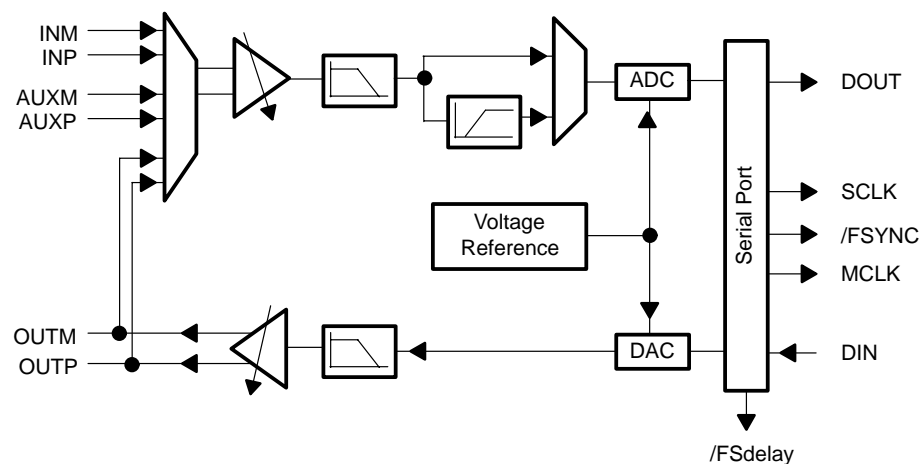
### 13.6.1 TLC320AC01/02 AICs

The analog-interface circuit (AIC) is a complete analog-interface system. The system consists of an ADC with an input amplifier multiplexer and antialiasing filter, a DAC path with a reconstruction filter and output amplifier, and the necessary serial data interfaces.

The AIC products were originally designed for modem-type applications; however, they are currently being used with DSPs in applications such as speech processing, speech analysis, voice encryption/decryption, modems, and industrial-process controls.

Figure 13–10 shows a block diagram of the TLC320AC01/02 AIC.

Figure 13–10. TLC320AC01/02 Block Diagram



### 13.6.2 TLC320AD55 Sigma-Delta AIC

The TLC320AD55 is a very high performance AIC. A sigma-delta architecture is used to achieve the high performance. This circuit provides the functionality and performance necessary to implement applications such as the V.34 modem.

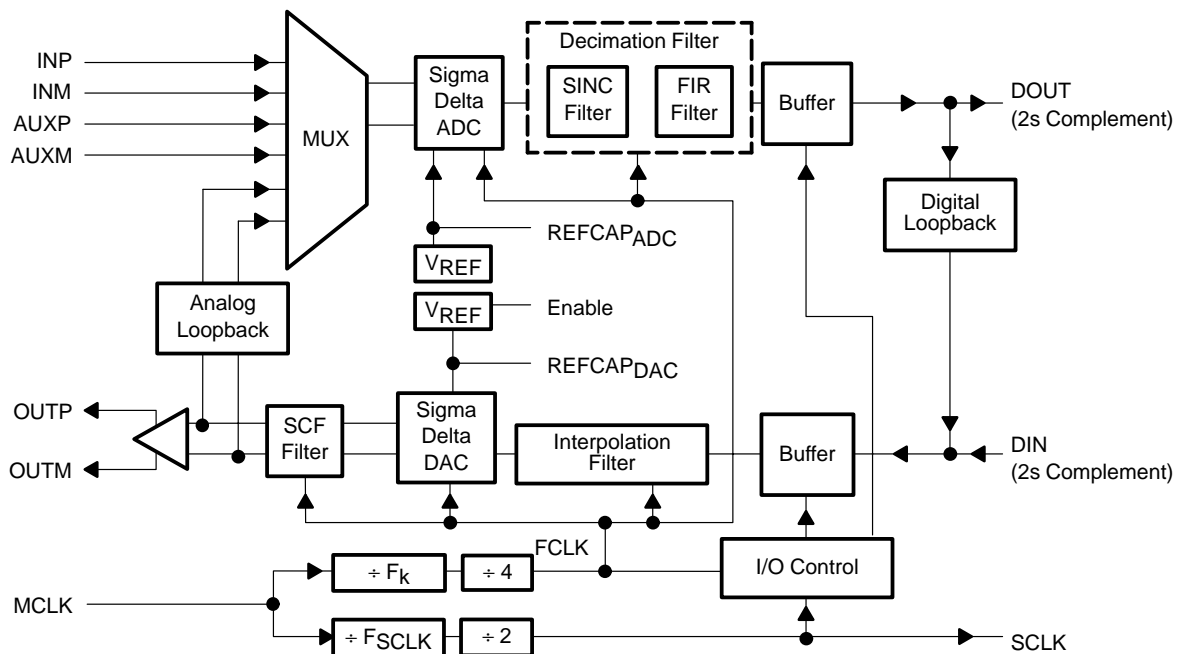
Key features of the TMC320AD55 include:

- ☐ Power supply: single 5 V
- ☐ Power-down mode
- ☐ Serial-port interface
- ☐ Antialiasing and anti-imaging filters
- ☐ 89-dB dynamic range
- ☐ 80-dB signal-to-noise (S/N) ratio
- ☐ 16-bit resolution
- ☐ Output gain control

Applications of the TLC320AD55 AIC include V.34 modems, DSP analog interfaces, noise-cancellation techniques, speech processing, and industrial process control. The TLC320AD55 has a 28-pin SOIC (DW) package.

Figure 13–11 shows a block diagram of the TLC320AD55 sigma-delta AIC.

Figure 13–11. TLC320AD55 Block Diagram



### 13.6.3 TLC320AD56 Sigma-Delta AIC

The TLC320AD56 is a cost-reduced version of the 'AD55. The cost reduction was accomplished by removing the switched capacitor filter in the DAC section, reducing the chip size and cost. Depending on the specific application, an external filter may be required.

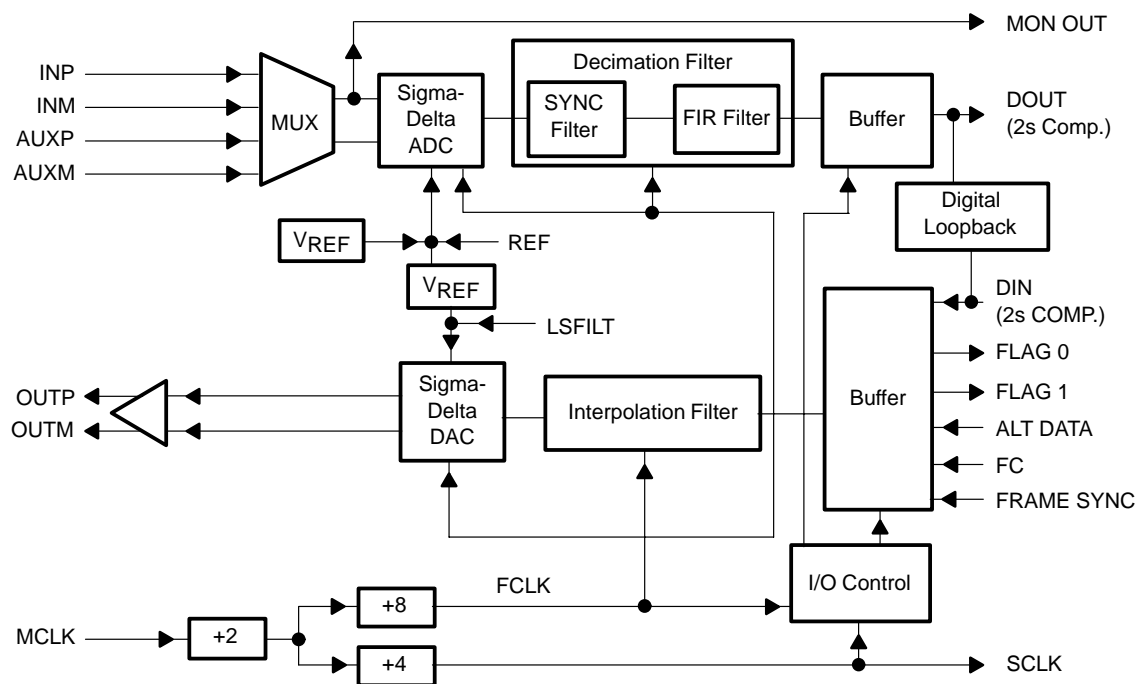
Features of the 'AD56 include:

- ☐ Power supply: single 5-V or 5-V analog/3-V digital
- ☐ Power-down mode to <1 mW
- ☐ Serial-port interface
- ☐ 91-dB dynamic range
- ☐ 88-dB S/N+D (ADC)
- ☐ 85-dB S/N+D (DAC)
- ☐ 16-bit resolution
- ☐ Cost-reduced solution

Applications of the 'AD56 include V.34 modems, DSP analog interfaces, noise-cancellation techniques, speech processing, industrial process control, and business audio. The 'AD56 has 28-pin PLCC and 48-pin SQFP (PCMCIA™) packages.

Figure 13–12 shows a block diagram of the TLC320AD56 sigma-delta AIC.

Figure 13–12. TLC320AD56 Functional Block Diagram



### 13.6.4 TLC320AD57/58 Stereo Sigma-Delta AICs

The TLC320AD57 and TLC320AD58 are stereo ADCs using the sigma-delta architecture. These converters contain two separate converters with a common control and serial interface.

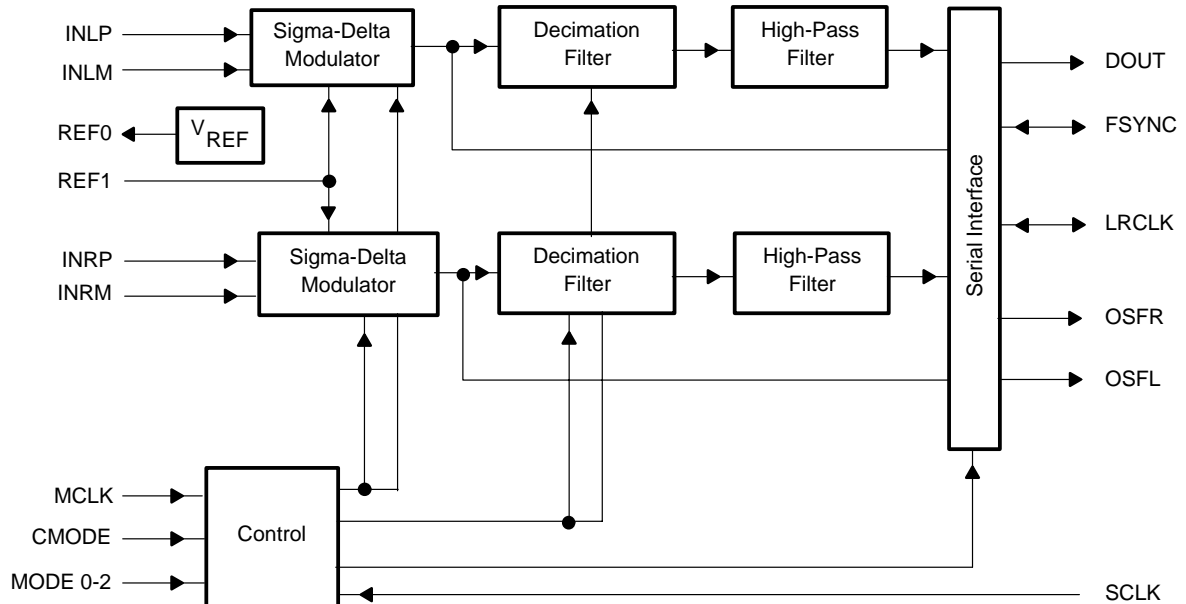
Features of the 'AD57/58 include:

- ☐ Power supply: Single 5 V
- ☐ Power-down mode
- ☐ Serial port interface
- ☐ 95-dB dynamic range
- ☐ 93-dB S/N+D
- ☐ 16-/18-bit resolution
- ☐ Sample rates to 48 kHz

Applications of the 'AD57/58 include consumer audio, digital radio, industrial process control, multimedia audio, workstations, and DSP analog interface.

Figure 13–13 shows a block diagram of the 'AD57/58 stereo sigma-delta AIC.

Figure 13–13. TLC320AD57/58 Functional Block Diagram



# Customizable DSPs (cDSP™)

Texas Instruments is the world leader in DSP solutions with offerings that suit a wide range of applications. Customizable DSPs utilize high-performance industry-standard cores with leading edge standard cell and gate-array application-specific integrated-circuit (ASIC) technology to enable a custom solution for your application requirements. With more than five years of experience shipping cDSP technology in volume, TI offers you its TMS320 family core architecture, a proven leader worldwide with more than 20,000 customers of mass market and custom products.

TI's exclusive cDSP™ technology enables high-performance full-integrated DSP systems on a single chip. The crucial parts of this solution are the TMS320 DSP cores and all peripherals, software and support needed to create the cost-effective, high-performance chip our customers demand. Timeline Technology™ is the name given to the TI integration technology that is used on customizable DSPs of up to 125-million transistors. This technology can cut development time in half.

The cDSP solution is now used in an array of industries and products, including automotive, cellular telephones, modems, CD-ROMs, and hard disk drives. The task of creating a cDSP device means your design team and TI's design team are committed to work together to meet your design goals.

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14.1 Attributes .....	14-2
14.2 Benefits .....	14-3
14.3 Key Features .....	14-4

## 14.1 Attributes

Various combinations of cores, memory blocks, peripherals, and ASIC logic are available through TI's cDSP and ASIC libraries to build a cDSP device configured to your specifications. Cores are optimized to minimize size and power consumption while maximizing processing power and ease of use. Presently, there are three proven TMS320 family cores available: the TMS320C2xLP, T320C52, and T320C54x. In addition to core memory, numerous selections of on-chip memory are available, including RAM, ROM, flash, and DRAM. The cDSP option offers an array of peripherals targeted at the wireless, hard disk drive, multimedia, and automotive markets. The complete ASIC library is available to integrate your custom design functions onto the die of the cDSP.

TI defines customizable DSPs as the ability to integrate on a single chip:

- ☐ An industry-standard DSP core ('C2xx, 'C5x, 'C54x...)
- ☐ The user's choice of memory (RAM, ROM, flash)
- ☐ Custom logic gates
- ☐ Analog modules (ADC, DAC,...)
- ☐ Software and hardware macros

For instance, TI supplies about 95 percent of the DSPs found in hard disk drives today, and because a single DSP can replace multi-component designs, HDD manufacturers have been able to cut the cost of drive electronics by more than 30 percent.

Development time for an HDD is just six months in today's competitive environment, followed by a short product life cycle of about 18 months. This makes time-to-market critical to the success of the new products. TI has demonstrated that it is able to move cDSP solutions for HDD designs from samples to volume production in less than three months.

## **14.2 Benefits**

The goal of TI's cDSP solution is to develop a unique product with enhanced system integration and performance, reduced cost, low power consumption and, most importantly, fast time to market. By consolidating system memory, logic, and peripherals within a single chip, cDSP customers save significant board space and reduce cost. Power consumption is lowered by reducing the system loading from several devices and their interconnection to a single cDSP. In addition, consolidation will increase system performance due to reduced access times and enhanced architecture. To minimize your time to market, the cDSP design flow is accompanied by extensive tools and support every step of the way. From a starter kit that allows you to sample the power of DSP products to the in-depth analysis of an IEEE Standard 1149.1 (JTAG)-compliant scan port, you are empowered with the tools and technical support needed to get your product to market quickly. By defining a cDSP solution to meet your exact system requirements, you can clearly differentiate your product from those of your competitors.



## 14.3 Key Features

Presently, there are three proven TMS320 family cores available:

DSP Cores Available	ASIC Family	Performance	Power Consumption (3/5 V)
TMS320C2xLP	TxC2000, TxC4000	30 and 40 MIPS	1.1/1.9 mA/MIPS
T320C52	TxC2000	40 and 50 MIPS	1.4/2.0 mA/MIPS
T320C54x	TxC4000, TSC5000	40 and 60 MIPS	1.5/2.5 mA/MIPS

The cDSP option offers many peripherals needed by DSP systems. The peripherals listed below are available or planned for development.

Peripherals:

- ☐ Analog switch
- ☐ ASIC PLL (APLL)
- ☐ Host port interface (HPI)
- ☐ 16-bit timer
- ☐ Synchronous serial port
- ☐ Serial-port interface (SPI)
- ☐ Keyboard interface
- ☐ Serial-control interface (SCI)
- ☐ Pulse-width modulation (PWM)
- ☐ Universal asynchronous receiver/transmitter (UART)
- ☐ Real-time clock
- ☐ Interface controller
- ☐ LCD controller
- ☐ Buffered serial port (BSP)
- ☐ General-purpose chip selects
- ☐ Maskable interrupts
- ☐ Synchronous serial port
- ☐ Asynchronous serial port
- ☐ Event timer
- ☐ Watchdog timer
- ☐ DMA controller

You can specify any of the available memory options listed below to meet your system specifications. All three cores can address up to 64K 16-bit words of program memory, 64K 16-bit words of local data memory, 32K 16-bit words of global data memory, and 64K 16-bit words of I/O ports for a total of 224K words address reach.

Memory type:

- ☐ Single-access RAM
- ☐ ROM
- ☐ Flash
- ☐ DRAM

Because cDSP is built into TI ASIC backplane technology, you benefit from all the features that are part of the associated TI ASIC library, including:

- ☐ 8-bit ADC
- ☐ 10-bit ADC
- ☐ 8-bit DAC
- ☐ ASIC logic
- ☐ General-purpose and specialized I/Os

## Code Generation Tools

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Texas Instruments supports designers in the complete development of their applications, from concept to production. This results in fast time to market, design ease, and increased productivity. TI development support products include the code-generation tools discussed in the sections listed below.

Topic	Page
15.1 TMS320 Optimizing ANSI C Compilers .....	15-2
15.2 TMS320 Macro Assembler, Linker, and Archiver .....	15-26

For part numbers, refer to Table 2–14 in Chapter 2, Selection Guide; for availability, cost, and other information, contact the nearest TI field sales office or authorized distributor.

## 15.1 TMS320 Optimizing ANSI C Compilers

Speedy development and code maintenance over the life cycle of a product are concerns that all developers share. TI supports DSP developers with a family of optimizing compilers for the TMS320 DSPs. TMS320 optimizing ANSI C compilers translate ANSI standard C language files into highly efficient TMS320 assembly language source files, which then are input to a TMS320 assembler/linker. All TMS320 compilers have been validated for their conformance to the ANSI C specification, using the industry-standard Plum-Hall test suite.

TI offers optimizing ANSI C compilers that support the 'C2x, 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x devices, and are complemented by the standard TMS320 programmer's interface for debugging C and assembly source code. The C compilers produce a rich set of information for the debugger, which allows source-level debugging in C. This enhances productivity and shortens the development cycle for both fixed-point and floating-point applications.

This section discusses four different compilers that have similar capability but different target processors:

- ☐ The TMS320 'C2x/C2xx/C5x optimizing ANSI C compiler is a full-featured C compiler that supports the 'C2x, 'C2xx, and 'C5x product families.
- ☐ The 'C54x optimizing ANSI C compiler supports the 'C54x. The 'C2x/C2xx/C5x and the 'C54x compilers are referred to as the fixed-point compilers.
- ☐ The TMS320 'C3x/'C4x floating-point optimizing ANSI C compiler is a full-featured C compiler that supports the 'C3x and 'C4x. Throughout this book, this compiler is referred to as the floating-point compiler.
- ☐ The 'C80 compiler is actually two compilers, one for the master processor and one for the parallel processor.

The TMS320 optimizing ANSI C compilers feature an ANSI-standard, runtime-support library (a source interlist utility to enable customers to associate assembly language statements with the C code that produced them), and a shell program that facilitates one-step translation from C source to TMS320 object-code files. The object code is then ROM-able, relocatable, and reentrant.

The benefits of ANSI C support are:

- ☐ **Standardization.** C, although one of the most portable programming languages, has lacked standardization, particularly in the area of common extensions to the language. ANSI provides a standard for these extensions.
- ☐ **Compatibility.** In general, the ANSI C standard is a superset of the Kernighan and Ritchie (K&R) standard. Most C programs that compile and run under a K&R compiler (including earlier releases of the TMS320 C compilers) should be capable of running under the new optimizing ANSI compiler. The few cases of obscure, obsolete, or questionable program constructions can be easily rewritten for ANSI compliance. ANSI compatibility also enhances portability; that is, existing code written for another processor can be ported into the TMS320 C compiler with little or no additional coding.
- ☐ **New types.** The new *const* and *volatile* types allow improved optimizations.
- ☐ **Improved function conventions.** Function prototypes allow improved type checking and enable optimization of calling conventions.

The optimizing ANSI C compilers were designed with three major efficiency goals in mind:

- ☐ Producing compiled, general-purpose C code that compares favorably to hand-coded assembly language
- ☐ Providing a simple and accessible programming interface to the C runtime environment so that time-critical DSP algorithms demanding extreme performance can be implemented in assembly language
- ☐ Establishing a comprehensive, easy-to-use tool set for the development of high-performance DSP applications in C

### 15.1.1 'C2x/C2xx/C5x Fixed-Point Compiler

The 'C2x/C2xx/C5x compiler enhances productivity by enabling you to program in C. C code is easier to prototype, debug, and benchmark than assembly language.

The fixed-point compilers translate the widely used ANSI C language directly into highly optimized assembly language for either a 'C2x, 'C2xx, or 'C5x device, according to a command line switch. Once an algorithm is coded in C, the TMS320 C compiler generates the appropriate assembly code, which is then assembled and linked by the TMS320 assembler and linker.

The fixed-point C compiler and assembly language tools support modular programming by allowing you to compile and assemble individual modules and then link them together. The fixed-point C compilers also perform both global optimizations and loop optimizations, such as strength reduction.

### 15.1.2 'C54x Fixed-Point Compiler

The 'C54x compiler enhances productivity by enabling you to program in C. C code is easier to prototype, debug, and benchmark than assembly language.

The 'C54x compiler translates the widely used ANSI C language directly into highly optimized assembly language for the 'C54x, according to a command line switch. Once an algorithm is coded in C, the TMS320 C compiler generates the appropriate assembly code, which is then assembled and linked by the TMS320 assembler and linker.

The 'C54x compiler and assembly language tools support modular programming by allowing you to compile and assemble individual modules and then link them together. The 'C54x compiler also performs both global optimizations and loop optimizations, such as strength reduction.

### 15.1.3 'C3x/C4x Floating-Point Compiler

The 'C3x/C4x floating-point compiler supports the 'C3x and 'C4x devices and performs both global optimizations and loop optimizations, such as strength reduction. Additionally, it thoroughly analyzes code to optimize the use of memory and register variables. It also searches for vector/matrix operations by mapping memory accesses to those 'C4x addressing modes that were optimized for the vector and matrix operations.

For the 'C40, a parallel-processing, runtime-support library uses the communication ports and DMA controller of the 'C4x. This simplifies the use of this device's powerful features for multiprocessor applications.

### 15.1.4 'C8x Multiprocessing Compilers

The C compilers for the single-chip, multiprocessing 'C8x support both the on-chip parallel-processing DSPs (PPs) and the RISC master processor (MP). This allows programmers to develop sophisticated applications in a high-level language such as C and then optimize their code in assembly. The C compilers allow for easy implementation of data and message passing between tasks (or processors) in parallel-processing systems.

The compiler package includes a 4-level optimization program that improves the execution speed and reduces the size of C programs by simplifying loops, rearranging statements and expressions, and allocating variables into registers.

### 15.1.5 Key Features of TMS320 Optimizing ANSI C Compilers

Key features of the TMS320 optimizing ANSI C compilers include:

- ☐ Complete and exact conformance with the ANSI C specification
- ☐ Highly efficient code. The compilers incorporate state-of-the-art generic and target-specific optimizations (described in detail in the following subsections).
- ☐ ANSI standard runtime-support library
- ☐ ROM-able, relocatable, and reentrant code
- ☐ The ability to link C programs with assembly language routines, allowing hand coding of time-critical functions in assembly language
- ☐ A full-featured, flexible linker that allows total control over memory allocation, memory configuration, and partial linking and contains features that allow easy runtime relocation of code
- ☐ A C shell program that facilitates one-step translation from C source to executable code
- ☐ Fast compilation to increase productivity
- ☐ Unlimited symbol table space (up to the amount of available host memory)
- ☐ Complete and useful diagnostics (error messages)
- ☐ An archiver utility that allows you to collect files into a single archive file or library by adding new files or by extracting, deleting, or replacing files. You can use a library of object files as input to the linker.
- ☐ Ability to expand inline both runtime-support and user-defined functions
- ☐ A utility that builds object libraries from source libraries
- ☐ A variety of listing files, including:
  - Assembly-source file, which can optionally include interlisted, C source code as well as register-usage information
  - Preprocessed output file useful for separating preprocessing/parsing (if memory limitations dictate) and for troubleshooting macro definitions
  - Assembly-listing file with line numbers and opcodes

The TMS320 C compilers have passed all Plum-Hall validation suites, which are a series of routines that test the validity and conformability of a C compiler. Plum-Hall validation is the *de facto* standard for validating ANSI C compilers.

The floating-point compilers have a big memory model with unlimited space for global data, static data, and constants. In the small (default) model, this space is limited to 64K words for faster, more efficient coding/execution.

The floating-point compiler for the 'C30 also has a short multiplication option that generates efficient MPYI instructions. These are  $24 \times 24$ -bit multiplication on the 'C3x, yielding a 32-bit resultant for integer multiplications instead of runtime-support calls.

### 15.1.6 TMS320 ANSI C Compiler Optimizations

The efficiency of a C compiler depends on the scope and number of optimizations the C compiler performs, as well as on the application. The TMS320 C compilers perform a wide variety of optimizations to improve the efficiency of the compiled code. The following list and the explanations in Section 15.1.6.1 to Section 15.1.6.3 describe some of the optimizations and highlight particular strengths of the C compilers.

#### ☐ General-purpose C optimizations

- Algebraic reordering, symbolic simplification, constant folding
- Alias disambiguation
- Data flow optimizations
  - Copy propagation
  - Common subexpression elimination
  - Redundant assignment elimination
- Branch optimizations/control-flow simplification
- Loop induction variable optimizations, strength reduction
- Loop rotation
- Loop-invariant code motion
- Inline expansion of function calls

#### ☐ Fixed-point compiler optimizations

- Register variables
- Cost-based register allocation
- Autoincrement addressing modes
- Repeat blocks
- Delayed branches, calls, and returns
- Arranging of variables on the local frame
- Elimination of unnecessary LDPK instructions



- ☐ Floating-point compiler optimizations
  - Register variables
  - Register tracking/targeting
  - Cost-based register allocation
  - Autoincrement addressing modes
  - Repeat blocks
  - Delayed branch instructions
  - Use of registers for passing function arguments
  - Parallel instructions
  - Conditional instructions
  - Loop unrolling

#### 15.1.6.1 General-Purpose Optimizations

Differences in the same optimizations for fixed-point and floating-point compilers are highlighted in the examples.

- ☐ Algebraic reordering, symbolic simplification, constant folding

For optimal evaluation, the compiler simplifies expressions into equivalent forms requiring fewer instructions or registers. For example, the expression  $(a + b) - (c + d)$  requires more instructions and registers to evaluate than the equivalent expression  $((a + b) - c) - d$ . Operations between constants are folded into single constants. For example,  $a = (b + 4) - (c + 1)$  becomes  $a = b - c + 3$ . See Example 15–1.

- ☐ Alias disambiguation

Programs written in C generally use many pointer variables. Frequently, compilers are unable to determine whether two or more l (lowercase L) values (symbols, pointer references, or structure references) refer to the same memory location. This aliasing of memory locations often prevents the compiler from retaining values in registers, because it cannot be sure that the register and memory continue to hold the same values over time. Alias disambiguation is a technique that determines when two pointer expressions cannot point to the same location, allowing the compiler to freely optimize such expressions.

- ☐ Data flow optimizations

Collectively, the following three data flow optimizations replace expressions with less costly ones, detect and remove unnecessary assignments, and avoid operations that produce values already computed. The compiler performs these data flow optimizations both locally (within basic blocks) and globally (across entire functions). See Example 15–1 for fixed-point compilers and Example 15–2 and Example 15–3 for floating-point compilers.

■ Copy propagation

Following an assignment to a variable, the compiler replaces references to the variable with its value. The value could be another variable, a constant, or a common subexpression. This may result in increased opportunities for constant folding, common subexpression elimination, or even total elimination of the variable.

■ Common subexpression elimination

When the same value is produced by two or more expressions, the compiler computes the value once, saves it, and reuses it.

■ Redundant assignment elimination

Often, copy propagation and common subexpression elimination optimizations result in unnecessary assignments to variables (variables with no subsequent reference before another assignment or before the end of the function). The compiler removes these dead assignments.

**Example 15–1. Data Flow Optimizations for Fixed-Point Compilers**

```

simp(int j)
{
    int a = 3;
    int b = (j*a)+(j*2);
    int c = (j<<a);
    int d = (j>>3)+(j<<b);

    call(a,b,c,d);
    ...
}

```

**Fixed-point compiler ('C5x option) output is:**

```

_simp:
...
*****
*   b = j*5;
*****
LARK   AR2,-3+LF1      ;AR2 = &j
MAR     *0+
LT      *              ;T = *AR2
MPYK    5              ;P = T * 5
ADRK    4-LF1          ;AR2 = &b
SPL     *              ;*AR2 = P
*****
*   call(3, b, j << 3, (j >> 3) + (j << b));
*****
LT      *              ;T = *AR2
SBRK    4-LF1          ;AR2 = &j
LACT    * ,AR1         ;ACC = j<<b
SACL    * ,AR2         ;save off ACC on TOS (top of stack)
SSXM    *              ;need sign extension for right shift
LAC     * ,12,AR1      ;high ACC = j>>3
ADD     * ,15          ;add TOS to high ACC
SACH    *+,1,AR2       ;stack high ACC
LAC     * ,3,AR1       ;ACC = j<<3
SACL    *+,AR2         ;stack ACC
ADRK    4-LF1          ;AR2 = &b
LAC     * ,AR1         ;ACC = b
SACL    *+            ;stack ACC
CALLD   _call          ;call begins
LACK    3              ;ACC = 3
SACL    *+            ;stack ACC
CALL    _call          ;call occurs
...

```

*The constant 3, assigned to a, is copy-propagated to all uses of a; a becomes a dead variable and is eliminated. The sum of multiplying j by 3 (the value of a) and by 2 is simplified into b = j\*5, which is recognized as a common subexpression. The assignments to c and d are dead and are replaced with their expressions. These optimizations are performed across jumps.*

**Example 15–2. Data Flow Optimizations for Floating-Point Compilers**

```

simp(int j)
{
    int a = 3;
    int b = (j * a) + (j * 2);
    int c = (j << a);
    int d = (j >> 3) + (j << b);

    call(a,b,c,d);
    ...
}

```

**Floating-point compiler output is:**

```

_simp:
*
* RC   is allocated to user var 'j'
* RS   is allocated to temp var 'T$2'
* RE   is allocated to temp var 'T$1'
*
...
LDI     2,R0           ; (j*a + 2j) == (3j + 2j) == (5j) == (4j + j)
LSH     R0,RC,R1       ; R1 = (4j) == (j << 2)
ADDI    R1,RC,RE       ; b = (4j + j) == 5j
LDI     3,R1           ; load shift count
LSH     R1,RC,RS       ; c = (j << a) == (j << 3)
LSH     RE,RC,R2       ; R2 = (j << b)
ADDI    RS,R2,R3       ; R3 = (j << b) + (j << a)
PUSH    R3             ; push R3 (d)
PUSH    RS             ; push c
PUSH    RE             ; push b
PUSH    R1             ; push a (tracked in R1)
CALL    _call
...

```

*The constant 3, assigned to a, is copy-propagated into all uses of a. a becomes a dead variable and is removed completely. The sum of multiplying j by 3 (a) and by 2 is simplified into a multiply by 5, which is computed with a shift and add. The expression (j << a) is computed once for assignment to c and then reused for calculating d. These optimizations are also performed across jumps.*

**Example 15–3. Copy Propagation and Control-Flow Simplification for Floating-Point Compilers**

```
fsm()
{
    enum { ALPHA, BETA, GAMMA, OMEGA } state = ALPHA;
    int *input;

    while (state != OMEGA)
        switch (state)
        {
            case ALPHA: state = ( *input++ == 0 ) ? BETA : GAMMA; break;
            case BETA : state = ( *input++ == 0 ) ? GAMMA : ALPHA; break;
            case GAMMA: state = ( *input++ == 0 ) ? GAMMA : OMEGA; break;
        }
}
```

**Floating-point compiler output is:**

```
_fsm:
*
* AR4      is allocated to user var 'input'
*
    LDI      *AR4++,R0    ; initial state == ALPHA.
    BZ      L4           ; if input == 0      goto state BETA
    B       L12          ; else                goto state GAMMA
L9:  LDI      *AR4++,R0    ; state == ALPHA.
    BNZ     L12          ; if input != 0      goto state GAMMA
L4:  LDI      *AR4++,R0    ; state == BETA.
    BNZ     L9           ; if input != 0      goto state ALPHA
    LDI      *AR4++,R0    ; state == GAMMA.
    BNZ     EPI0_1       ; if input != 0      goto state OMEGA
L12: LDI      *AR4++,R0    ; state == GAMMA.
    BZ      L12          ; if input == 0      goto state GAMMA
EPI0_1:...              ; state == OMEGA.
    ...
```

*The switch statement and the state variable from this simple finite-state machine process are optimized completely away, leaving a streamlined series of conditional branches.*

☐ Branch optimizations/control-flow simplification

The compiler analyzes the branching behavior of a program and rearranges the linear sequences of operations (basic blocks) to remove branches or redundant conditions. Unreachable code is deleted, branches to branches are bypassed, and conditional branches over unconditional branches are simplified to a single conditional branch. When the value of a condition can be determined at compile time (through copy propagation or other data flow analysis), a conditional branch can be deleted. Switch case lists are analyzed in the same way as conditional branches and are sometimes eliminated entirely. Some simple control-flow constructs can be reduced to conditional instructions, totally eliminating the need for branches. See Example 15–3 for floating-point compilers.

☐ Loop induction variable optimizations, strength reduction

Loop induction variables are variables whose value within a loop is directly related to the number of executions of the loop. Array indices and control variables of *FOR* loops are very often induction variables. Strength reduction is the process of replacing costly expressions involving induction variables with more efficient expressions. For example, code that indexes into a sequence of array elements is replaced with code that increments a pointer through the array. Loops controlled by incrementing a counter are written as either floating-point or fixed-point repeat blocks, or by using efficient decrement-and-branch instructions. Induction variable analysis and strength reduction together often remove all references to the programmer's loop control variable, allowing it to be eliminated entirely.

☐ Loop rotation

The compiler evaluates loop conditionals at the bottom of loops, saving a costly extra branch out of the loop. In many cases, the initial entry conditional check and the branch are optimized out.

☐ Loop-invariant code motion

This optimization identifies expressions within loops that always compute the same value. The computation is moved in front of the loop, and each occurrence of the expression in the loop is replaced by a reference to the precomputed value.

☐ Inline expansion of function calls

The special keyword *inline* directs the compiler to replace calls to a function with inline code, saving the overhead associated with a function call as well as providing increased opportunities to apply other optimizations. See Example 15–4 and Example 15–5.

**Example 15–4. Inline Function Expansion for Fixed-Point Compilers**

```

inline int acc(int *p, int n)
{
    int i;
    int sum = 0;

    for (i = 0; i<n; i++)
        sum += p[i];
    return sum;
}
process(int *p)
{
    int sum;

    sum = acc(p, 100)
    ...
}

```

**Fixed-point compiler ('C5x option) output is:**

```

_process:
LF2  .set      0
....

                                ;ARP = AR6
LARK  AR6,1      ;AR6 = &acc_1_sum
MAR   *0+
LACK  0          ;ACC = 0
SACL  *,AR2      ;acc_1_sum = 0
LARK  AR2, -3+LF2 ;AR2 = &p
MAR   *0+
LAR   AR5,*,AR5  ;AR5 = p
LACK  99
SAMB  BRCL      ;loop 100 times
RPTB  L9-1      ;begin loop
LAC   ++,AR6    ;ACC = *p+
ADD   *         ;ACC += acc_1_sum
SACL  *,AR5     ;acc_1_sum = ACC
L9:   ....
                                ;end loop
....

```

*The keyword inline signals the compiler to expand the call to acc in place. The symbol acc\_1\_sum is created to accumulate the sum.*

**Example 15–5. Inline Function Expansion for Floating-Point Compilers**

```

inline blkcpy (char *to, char *from, int n)
{
    if (n > 0 )
        do *to++ = *from++; while (--n !=0);
}
struct s { int a,b,c[10]; } s;
initstr (struct s *ps, char t[12])
{
    blkcpy((char *)ps, t, 12);
}

```

**Floating-point compiler output is:**

```

_initstr
* R2  assigned to variable 't'
* AR2 assigned to variable 'blkcpy_1_to'
* AR4 assigned to variable 'blkcpy_1_from'
* BK  assigned to variable 'ps'
* RC assigned to variable 'L$1'

        LDI        BK,AR2          ;blkcpy_1_to = ps
        LDI        R2,AR4          ;blkcpy_1_from = t
        LDI        *AR4++,R0       ;+-----
        RPTS       10              ;| expansion of blkcpy:
        STI        R0,*AR2++       ;| copy 12 words
||      LDI        *AR4++,R0       ;+-----
        STI        R0,*AR2++       ;
...

```

*The special inline declaration of blkcpy results in the call being replaced with the function's body. The compiler creates temporary variables blkcpy\_1\_to and blkcpy\_1\_from, corresponding to the parameters of blkcpy. Often, copy propagation can eliminate assignments to such variables when the argument expressions are not reused after the call.*

**15.1.6.2 Fixed-Point Compiler Optimizations**

The following optimizations are specific to the 'C2x/C2xx/C5x compiler.

☐ Register variables

The compiler maximizes the use of the address registers of the 'C2x/C2xx/C5x DSPs by using them as pointers. This optimization is particularly effective for pointers that arise when array index constructs are turned into loop induction variables.

☐ Cost-based register allocation

The compiler allocates registers to user variables and temporary values according to their type, use, and frequency. Variables used within loops are weighted to have priority over others, and those variables whose uses do not overlap can be allocated to the same register.



#### □ Autoincrement addressing modes

For pointer expressions of the form *\*p++*, the compiler uses efficient 'C2x/C2xx/C5x autoincrement addressing modes. In many cases, where code steps through an array in a loop, such as *for (i = 0; i < N; ++i) a[i]...*, the loop optimizations convert the array references to indirect references through autoincremented register variable pointers.

#### □ Repeat blocks

For the 'C5x, the compiler supports zero-overhead loops with the RPTB instruction. The compiler can detect loops controlled by counters and generate them via the efficient repeat forms. The iteration count can be either a constant or an expression. For the 'C2x, which does not have a repeat block instruction, the compiler allocates an AR as the loop counter and implements the loop with a BANZ instruction. See Example 15–6.

**Example 15–6. Repeat Blocks, Autoincrement Addressing Modes, Strength Reduction, Induction Variable Elimination, Register Variables, and Loop Test Replacement for Fixed-Point Compilers**

```
int a[10], b[10];
scale (int k)
{
    int i;
    for (i = 0; i < 10; ++i)
        a[i] = b[i] *k;
```

**Fixed-point compiler ('C5x option) output is:**

```
_scale:
...
LRLK    AR6, _a          :AR6 = &a[0]
LRLK    AR5, b           ;AR5 = &b[0]
LACK    9
SAMB    BRCCR
LARK    AR2, -3+LF1      ;AR2 = &k
MAR     *0+, AR5
RPTB    L4-1             ;repeat block 10 times
LT      ++, AR2          ;T = *AR5++
MPY     *, AR6           ;P = T ** AR2
SPL     ++, AR5          ;*AR6 += P
L4:
...
```

*Induction variable elimination and loop test replacement allow the compiler to recognize the loop as a simple counting loop and then generate a repeat block. Strength reduction turns the array references into efficient pointer autoincrements.*

□ Delayed branches, calls, and returns

The 'C5x supports a number of delayed branch, call, and return instructions. Three of these are used by the compiler: branch unconditional (BD), call to a named function (CALLD), and simple return (RETD). These instructions execute in two fewer cycles than their nondelayed counterparts. They execute two instruction words after they enter the instruction stream. Sometimes it is necessary to insert an NOP after a delayed instruction to ensure proper operation. This involves one more word of code than a non-delayed sequence, but it is still one cycle faster. Note that the compiler emits a comment in the instruction sequence where the delayed instruction executes. See Example 15–7.

□ Arranging variables on the local frame

Local variables are accessed by adjusting AR2 to point to the variable on the frame and then by accessing AR2 indirectly. If variables that are allocated far apart on the local frame must be accessed sequentially, an ADRK or SBRK instruction is required to adjust AR2. If variables that are allocated next to each other must be accessed sequentially, the ADRK or SBRK instruction is not required, because AR2 can be adjusted to point to the next variable by adding a + or a – symbol to the previous indirect access. The compiler takes advantage of this situation by recognizing local variables that are accessed sequentially and allocating those variables next to each other. See Example 15–8.

**Example 15–7. Fixed-Point Compiler Delayed Branch, Call, and Return Instructions**

```

driver()
{
    int i0, i1;
    while (input(&i0) && input(&i1))
        process(i0, i1);
}

```

**Fixed-point compiler ('C5x option) output is:**

```

_driver:
    POPD      *+
    SAR       AR0,*+           ;save AR0 and return address
    SAR       AR1,*           ;set up local frame
    LARK      AR0,3
    LAR       AR0,*0+
;   <save register vars>
    SAR       AR6,*+           ;save AR6
    SAR       AR7,*+,AR6       ;save AR7
    LARK      AR6,1           ;AR6 = &i0
    LARK      AR7,2           ;AR7 = &i1
    BD        L2              ;begin branch to loop control
    MAR       *0+,AR7
    MAR       *0+

*** B        L2              ;branch to loop control occurs
L1:
    LAC       *,AR1           ;stack *AR7
    SACL      *+,AR6
    CALLD     _process        ;call occurs
    LAC       *,AR1
    SACL      *+
*** CALL     _process OCCURS ;begin call
    SBRK      2
L2:
    CALLD     _input          ;loop control
                                ;begin call
    MAR       *,AR1
    SAR       AR6,*+          ;stack AR6 (&i0)
*** CALL     _input OCCURS   ;call occurs
    MAR       *-              ;clear stack
    BZ        EPIO_1         ;quit if _input returns 0
    CALLD     _input          ;begin call
    SAR       AR7,*+          ;stack AR7 (&i1)
    NOP                          ;necessary, no branches in delay slot
    CALL      _input          ;call occurs
    MAR       *-,AR7          ;clear stack
    BNZ       L1              ;continue if _input returns !0
EPIO_1:
    MAR       *,AR1           ;function epilog
;   <restore register vars>
    MAR       *-
    LAR       AR7,*-          ;restore AR7
    LAR       AR6,*           ;restore AR6
    SBRK      4               ;clear local frame
    PSHD      *-              ;push return address on hardware stack
    RETD                          ;begin return
    LAR       AR0,*           ;restore AR0
    NOP                          ;necessary, no PSHD in delay slot
*** RET      OCCURS          ;return occurs

```

**Example 15–8. Arranging Variables on the Local Frame**

```
func()
{
    int a,b,i,j;
    ...
    call(i+a,j+b);
}
```

**Fixed-point compiler ('C5x option) output is:**

```
_func:
    ...
    LAC    *+                ;ARP = AR2, AR2 points to b
    ADD    *+,AR1            ;ACC = b, AR2 point to j
    SACL   *+,AR2            ;ACC += j, AR2 points to a
    LAC    *+                ;stack ACC
    CALLD  _call             ;ACC = a, AR2 points to i
    ADD    *,AR1             ;begin call
    SACL   *+                ;ACC += i
    *** CALL _call OCCURS   ;stack ACC
    SBRK   2                 ;call occurs
    SBRK   2                 ;clear stack
```

*The compiler rearranges the order of the variables on the local frame from int a,b,i,j; to int b,j,a,i; so that the expressions can be computed without unnecessary additional adjustments to AR2, the local variable pointer register.*

☐ **Elimination of unnecessary LDPK instructions**

Whenever a global variable is accessed, the compiler must first ensure that the page pointer has the right value to allow correct access of that variable. If the page pointer does not have the right value, the value must be loaded with an LDPK instruction. To avoid emitting unnecessary LDPK instructions, the compiler performs analysis of global variables declared in a module. This analysis determines where, relative to page boundaries, the global variables are allocated. Note that this analysis does not include variables declared in a different module which are only referenced in the current module. Therefore, when handling successive accesses of global variables declared in the current module, the compiler issues an LDPK instruction only when a variable does not reside in the same page as the last global variable accessed. See Example 15–9.

**Example 15–9. Elimination of Unnecessary LDPK Instructions**

```
int g1, g2, g3;
extern int e1;
```

```
func()
{
    g1 = g2+g3;
    e1 = g2;
}
```

**Fixed-point compiler ('C5x option) output is:**

```
_func
```

```
...
LDPK    _g3          ;set page pointer for this module
LAC     _g3          ;load g3
ADD     _g2          ;add g2
SACL    _g1          ;store g1
LAC     _g2          ;load g2
LDPK    _e1          ;set page pointer for external variable
SACL    _e1          ;store e1
```

*Because g1, g2, and g3 are all declared in the local module, the compiler can determine where the variables are in relation to page boundaries and can change the page pointer accordingly — in this case, only once. Note that the page pointer is reset to access the variable that is declared in another module and only referenced in this module.*

### 15.1.6.3 Floating-Point Compiler Optimizations

The following optimizations are specific to the floating-point compiler.

#### ☐ Register variables

The compiler helps maximize the use of registers for storing local variables, parameters, and temporary values. Variables stored in registers can be accessed more efficiently than variables in memory. This optimization is particularly effective for pointers that arise when array index constructs are turned into loop induction variables. See Example 15–10 and Example 15–11.

#### Example 15–10. Register Variables and Register Tracking/Targeting

```
int gvar;
reg(int i, int j)
{
    gvar = call() & i;
    j = gvar + i;
}
```

#### **Floating-point compiler output is:**

```
_reg:
*
*R4 is allocated to user var 'i'
*R5 is allocated to user var 'j'
*
...
CALL    _call        ;R0 = call()
AND     R4,R0        ;R0 &= i
STI     R0,@_gvar     ;gvar = R0
ADDI    R4,R0,R5      ;tracks gvar in R0,
...                          ;targets result into R5 (j)
```

*The compiler allocates local variables *i* and *j* into registers *R4* and *R5*, as indicated by the comments in the assembly listing. Allocating *i* to *R4* and tracking *gvar* in *R0* allows the sum *gvar + i* to be computed with a 3-operand instruction, targeting the result directly into *j* in *R5*.*

#### ☐ Register tracking/targeting

The compiler tracks the contents of registers so that it avoids reloading values if they are used again soon. Variables, constants, and structure references such as *(a.b)* are tracked through both straight-line code and forward branches. The compiler also uses register targeting to compute expressions directly into specific registers when required, as in the case of assigning to register variables or returning values from functions. See Example 15–10.

**Example 15–11.** *Repeat Blocks, Autoincrement Addressing Modes, Parallel Instructions, Strength Reduction, Induction Variable Elimination, Register Variables, and Loop Test Replacement for Floating-Point Compilers*

```
float a[10], b[10];
scale(float k)
{
    int i;
    for (i = 0; i < 10; ++i)
        a[i] = b[i] * k;
    ...
}
```

**Floating-point compiler output is:**

```
_scale:
...
    LDI        @CONST+0,AR4        ; AR4 = &a[0]
    LDI        @CONST+1,AR5        ; AR5 = &b[0]
    MPYF       R4,*AR5++,R0        ; compute first product
    RPTS       8                   ; loop for next 9
    STF        R0,*AR4++           ; store this product...
|| MPYF       R4,*AR5++,R0        ; ...and compute next
    STF        R0,*AR4++           ; store last product
    ...
```

*This process shows general and floating-point-specific optimizations working together to generate highly efficient code. Induction variable elimination and loop test replacement allow the compiler to recognize the loop as a simple counting loop and then generate a repeat block. Strength reduction turns the array's references into efficient pointer autoincrements. The compiler unrolls the loop once to separate the first multiply and last store, allowing the body of the loop to be written as a single parallel instruction.*

#### ☐ Cost-based register allocation

The compiler, when enabled, allocates registers to user variables and compiles temporary values according to their type, use, and frequency. Variables used within loops are weighted to have priority over others, and those variables whose uses do not overlap may be allocated to the same register. Variables with specific requirements are allocated into registers that can accommodate them.

#### ☐ Autoincrement addressing modes

For pointer expressions of the form  $*p++$ ,  $*p--$ ,  $*++p$ , or  $*--p$ , the compiler uses efficient TMS320 autoincrement addressing modes. In many cases, where code steps through an array in a loop, such as `for (i = 0; i < N; ++i) a[i] ...`, the loop optimizations convert the array's references to indirect references through autoincremented register variable pointers. See Example 15–11.

### ❑ Repeat blocks

The floating-point compiler supports zero-overhead loops with the RPTS (repeat single) and RPTB (repeat block) instructions. The compiler can detect loops controlled by counters and generate them by using the efficient repeat forms: RPTS for single-instruction loops or RPTB for larger loops. For both forms, the iteration count can be either a constant or an expression. See Example 15–5 and Example 15–11.

Induction variable elimination and loop test replacement allow the compiler to recognize the loop as a simple counting loop and then generate a repeat block. Strength reduction turns the array references into efficient pointer autoincrements.

### ❑ Delayed branch instructions

The floating-point compiler supports delayed branch instructions that can be inserted three instructions early in an instruction stream, avoiding costly pipeline flushes associated with normal branches. The compiler uses unconditional delayed branches wherever possible and conditional delayed branches for counting loops. See Example 15–12.

#### Example 15–12. Floating-Point Compiler Delayed Branch Optimizations

```
wait(volatile int *p)
{
    for(;;)
        if (*p & 0x80) *p |= 0xF0;
}
```

**Floating-point compiler output is:**

```
_wait:
L6:
    LDI  *AR4,R0      ; R0 = *p (AR4 is allocated to p)
    TSTB 128,R0      ; test *p & 0x80
    BZ   L6           ; false: loop back
    BD   L6           ; true: loop back (delayed)
    LDI  *AR4,R0      ; R0 = *p
    OR   0f0h,R0      ; R0 = *p | 0xF0
    STI  R0,*AR4      ; *p = R0
***    B    L6        ; branch occurs
```

*The unconditional branch at the bottom of this loop is written as a delayed branch, allowing it to execute in one machine cycle.*



☐ Use of registers for passing function arguments

The compiler supports a new, optional calling sequence that passes arguments to registers rather than pushing them onto the stack. This can result in significant improvement in performance, especially if calls are important in the application. See Example 15–3.

☐ Parallel instructions

Several floating-point instructions such as load/load, store/operate, and multiply/add can be paired and executed in parallel. When adjacent instructions match the addressing requirements, the compiler combines them in parallel. Although the code generator performs this optimization, the optimizer greatly increases effectiveness because operands are more likely to be in registers. See Example 15–5 and Example 15–11.

☐ Conditional instructions

The load instructions in the floating-point C compiler can be executed conditionally. For simple assignments such as *a = condition ? expr1 : expr2* or *if (condition) a = b*, the compiler can use conditional loads to avoid costly branches.

☐ Loop unrolling

When the compiler determines that a short loop is executed a low, constant number of times, it replicates the body of the loop rather than generating the loop; note that low and short are subjective judgments made by the compiler. This avoids any branches or use of the repeat registers. See Example 15–13.

**Example 15–13. Loop Unrolling**

```

add3(int a[3])
{
    int i, sum = 0;
    for (i = 0; i < 3; ++i) sum += a[i]

    return sum;
}

```

***Floating-point compiler output is:***

```

_add3:
    ...
    LDI        *-FP(2),AR4    ; AR4 = &a[0]
    LDI        *AR4++,RC      ; sum += a[0]
    ADDI       *AR4++,RC      ; sum += a[1]
    ADDI       *AR4++,RC      ; sum += a[2]
    LDI        RC,R0          ; return sum
    ...

```

*The compiler determines that this loop is short enough to unroll, resulting in a simple three-instruction sequence and no branches.*

**15.1.6.4 'C80 Multiprocessing Compiler Optimizations**

The following optimizations are specific to the multiprocessing compilers:

- ☐ Register allocator streamlines code development by efficiently managing variable usage of registers
- ☐ Code compactor examines serially-written code to identify instructions that can run in parallel
- ☐ Multitasking executive simplifies the synchronization and execution of multiple DSP tasks running concurrently on the 'C80. Supports 'C8x-to-host processor communications and provides local control of on-chip parallel-processing tasks.
- ☐ Allocates variables to registers
- ☐ Performs control-flow-graph simplification, loop rotation, loop unrolling
- ☐ Simplifies expressions and statements, and functions with return values that are never used
- ☐ Expands calls to functions declared inline
- ☐ Performs local copy/constant propagation and loop optimizations
- ☐ Eliminates local common expressions, global common subexpressions, and global redundant assignments

- ☐ Converts array references in loops to incremented pointer form
- ☐ Reorders function definitions so attributes of called functions are known when the caller is optimized
- ☐ Propagates arguments into function bodies when all call sites pass the same value in the same argument position

## 15.2 TMS320 Macro Assembler, Linker, and Archiver

The TMS320 macro assemblers and linkers are currently available for all TMS320 devices. The fixed-point assembler and linker support the 'C1x/C2x/C2xx/C5x devices; the floating-point assembler and linker support the 'C3x/C4x devices. Assemblers and linkers are also available for both the 'C54x and the 'C8x. The assembler/linker is shipped with the C compiler package. For the 'C1x/C2x/C2xx/C5x, 'C54x, and 'C3x/C4x, a PC version without the C compiler is available. This section discusses the two assembler and linker toolsets (floating point and fixed point) and highlights their differences.

The TMS320 macro assembler and linker are code-generation tools that convert TMS320 assembly language source files into executable object code. Key features include:

- ☐ Macro capabilities and library functions
- ☐ Conditional assembly
- ☐ Relocatable modules
- ☐ Complete error diagnostics
- ☐ Symbol table and cross-references

The **assembler** translates assembly language source files into machine language object files. Source files can contain instructions, assembler directives, and macro directives. Assembler directives control various aspects of the assembly process such as the source-listing format, symbol definition, and the way the source code is placed into sections. The assembler has the following features:

- ☐ Processes the source statements in a text file to produce a relocatable object file
- ☐ Produces a source listing (if requested) and provides control over this listing
- ☐ Appends a cross-reference listing to the source listing (if requested)
- ☐ Allows segmentation of your code
- ☐ Maintains a section program counter (SPC) for each section of object code
- ☐ Defines and references global symbols
- ☐ Assembles conditional blocks
- ☐ Supports macros, allowing the user to define macros either inline with or within a macro library

- ☐ For the TMS320C8x assemblers:
  - Separate assemblers support the MP and PP assembly languages and a linker links assembled code in common object file format (COFF) into common memory.
  - Directives map program and data code on specific processors for fast integration and debugging of parallel-processing code.
  - Support is provided to relocatable modules for maximum code flexibility.

The **linker** combines object files into a single executable object module. As it creates the executable module, it performs relocation operations and resolves external references. The linker accepts COFF object files (created by the assembler) as its input. It can also accept archive library members and modules created by a previous linker run. Linker directives allow you to combine object file sections, bind sections and symbols to specific addresses, and define/redefine global symbols. The linker has these features:

- ☐ Defines a memory model that conforms to the target system's memory
- ☐ Combines object file sections
- ☐ Allocates sections into specific areas within the target system's memory
- ☐ Defines or redefines global symbols to assign them specific values
- ☐ Relocates sections to assign them to final addresses
- ☐ Resolves undefined external references between the input files

The **archiver** makes it possible to collect a group of files into a single archive file. For example, several macros can be collected together into a macro library. The assembler searches through the library and uses the members that are called as macros by the source file. Also, it is possible to use the archiver to collect a group of object files into an object library. The linker includes the members in the library that resolve external references during the link.

Most EPROM programmers do not accept COFF object files as their input. The assembler/linker includes a utility to convert the COFF file into Intel™, Tektronix™, TI-tagged, Motorola-S™, or ASCII hex-object formats.

# System Integration and Debugging Tools

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The system integration and debugging tools for the TMS320 family of digital signal processors include the TMS320 debugger's interface (C/assembly source debugger), software simulators, standard evaluation modules (EVMs), and emulators (XDS/22™ and XDS510™/XDS510WS). These tools are described in the following sections.

<b>Topic</b>	<b>Page</b>
<b>16.1 TMS320 Debugger's Interface (C/Assembly Source Debugger) . . .</b>	<b>16-2</b>
<b>16.2 TMS320 Software Simulators . . . . .</b>	<b>16-7</b>
<b>16.3 TMS320 System Debugging and Evaluation Tools . . . . .</b>	<b>16-12</b>
<b>16.4 Code Composer—An Integrated Development Environment (IDE) . . . . .</b>	<b>16-28</b>

## **16.1 TMS320 Debugger's Interface (C/Assembly Source Debugger)**

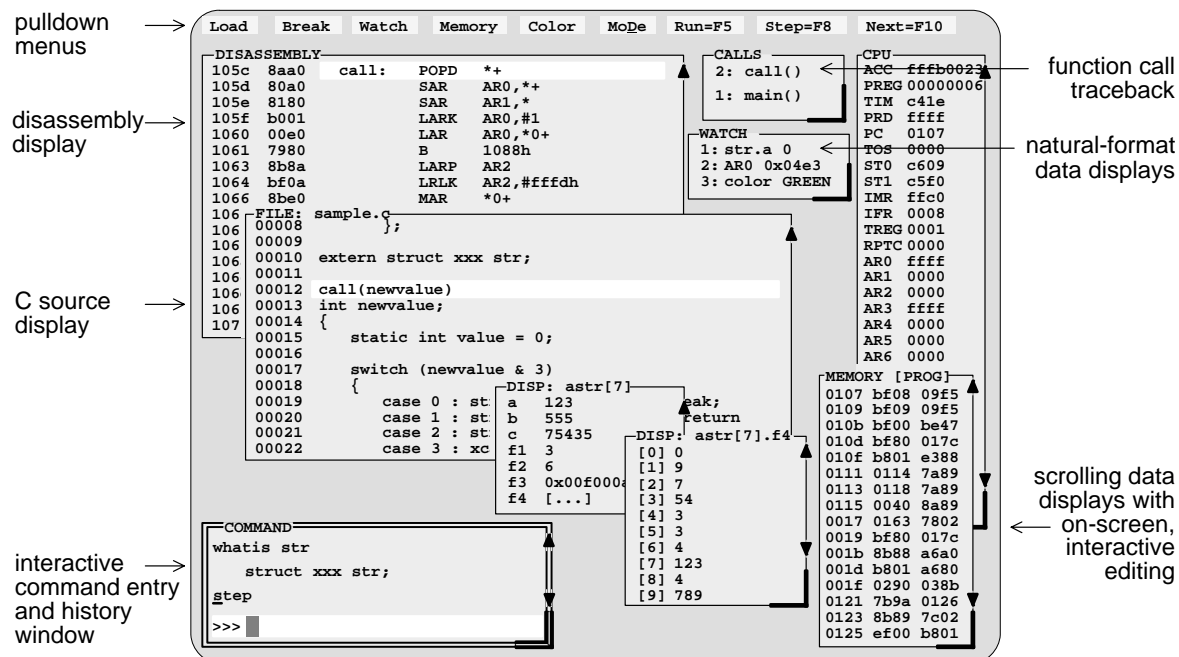
The TMS320 debugger's interface brings new levels of power and flexibility to embedded systems development. The C/assembly source debugger is the standard interface for the simulators, evaluation modules, and emulators. The debugger interface is now available for the TMS320C16 EVM and all 'C2x, 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x tools.

The debugger is an advanced software interface that runs on a PC or SPARC™ and works with TI debugging tools such as the unique, scan-based, real-time TMS320 emulators, the XDS510 and XDS510WS. The debugger provides complete control over programs written in C or assembly language.

The debugger improves productivity by enabling you to debug a program in the language in which it is written. Programs can be debugged in C, assembly language, or both. The debugger also has profiling capabilities that show where to focus development time by quickly identifying the hot or time-consuming sections of a program.

The debugger is easy to learn and use. Its menu-driven window and mouse-oriented interface reduces learning time and eliminates the need to memorize complex commands. The debugger's custom-made displays and flexible command entry let you develop a debugging environment that suits the systems needs (see Figure 16–1). A shortened learning curve and increased productivity reduce the software development cycle, speeding products to market.

Figure 16–1. Debugger's Customized Display



### 16.1.1 Debugger Features

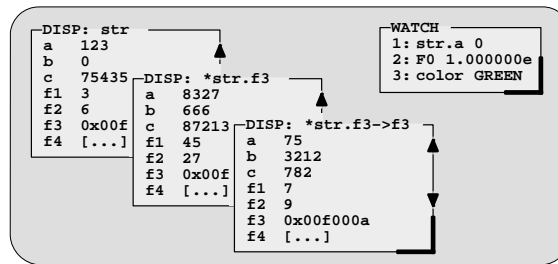
Conditional execution and single-stepping (including single-stepping into and over function calls) give you complete control over program execution. A breakpoint can be set or cleared with a click of the mouse or by typing commands. A memory map identifies the portions of target memory that the debugger can access and that can be defined. You can load only the symbol table's portion of an object file to work with systems that have code in ROM. The debugger can execute commands from a batch file, providing an easy method for entering often-used command sequences. Key features include:

- ☐ **Multioperation support.** For the 'C2xx, 'C4x, 'C5x, 'C54x, and 'C8x, the C/assembly debugger has been enhanced with special parallel-processing capabilities (multiple-processor debug/breakpoint and single-step).
- ☐ **Multilevel debugging.** The debugger allows you to debug both C and assembly language codes. While debugging a C program, you can choose to view the C source, the disassembly of the object code created from the C source, or both.



- ☐ **Fully configurable, window-oriented interface.** The debugger separates code, data, and commands into manageable information. You can select from several displays or, since the debugger's display is completely configurable, you can create the interface that best suits the application. You can change the display colors, the physical appearance of displayed features (such as window borders), and the window size and position.
- ☐ **Flexible command entry.** Commands can be entered by using a mouse, the function keys, or the pull-down menus. The debugger's command history can be used to reenter commands. Symbolic debug is supported, so structure and variable names can be used instead of address or data locations.
- ☐ **On-screen editing.** Any data value displayed in any window can be changed easily by pointing (with the mouse) at the value, clicking, and entering the correct value.
- ☐ **Continuous update.** The debugger continuously updates information on the screen, highlighting changed values.
- ☐ **Comprehensive data display.** You can easily create windows for watching, displaying, and editing the values of variables, arrays, structures, pointers — any kind of data — in their natural format (floating point, integer, character, enumerated, or pointer). Entire linked lists can be displayed (see Figure 16–2).

Figure 16–2. Debugger's Data Display



- ☐ **Powerful command set.** The TMS320 debugger supports a powerful command set that makes full use of C expressions. One debugger command performs actions that might require several commands in another system.
- ☐ **Compatibility.** The C source debugger runs on IBM PC-ATs and compatible PCs and SPARC workstations.
- ☐ **Simplicity.** The debugger's simple setup, default configurations, predefined commands, and inherent flexibility facilitate sophisticated debugging within a short time.

- ☐ **Calls stack window.** The calls stack window displays function names in the order that they are called and put on the stack. A function name is removed when popped from the calls stack. This allows you to debug a program that is not executing properly because of a lack of stack space.
- ☐ **Memory window.** Memory contents can be displayed and edited to allow you to observe the movement of data and compare expected values to actual ones.

### 16.1.2 Code Profiler

The code profiling functionality increases the debugging flexibility of the Texas Instruments C source debugger. By using the familiar debugger interface, the profiler shows you where to focus your development time by quickly identifying the time-consuming sections of the program. Code optimizations, such as eliminating bottleneck problems, can dramatically impact execution time. A powerful set of profiling commands simplifies the process of maximizing code efficiency.

Key features of the code profiler include:

- ☐ **User-friendly interface.** The TI code profiler shares the same fully configurable, window-oriented, and mouse-controlled interface as the TI C source debugger, so learning to profile is quick and easy.
- ☐ **Multilevel profiling.** An assembly window and a C window are displayed, so you can profile C code, assembly code, or both.
- ☐ **Powerful command set.** A rich set of commands is available to select and manipulate profile areas on the global, module, function, and explicit levels, so you can efficiently profile even the most complex applications.
- ☐ **Comprehensive statistics.** The profiler provides all the information you need to identify bottlenecks in your code:
  - The number of times each area was entered during the profile session
  - The total execution time of an area, including or excluding the execution time of any subroutines called from within that area
  - The maximum time for one iteration of an area, including or excluding the execution time of any subroutines called from within that area
- ☐ **Versatile display.** The profiler allows you to choose profile areas, the type of statistical data, and the sorting criteria, which ensures an efficient, customized display of statistics. The data also can be accompanied by histograms to show the statistical relationship between profile areas.

- ☐ **Disabled areas.** You can disable portions of a profile area to prevent them from adding to the statistics. This is convenient for removing the timing impact of standard library functions or a fully optimized portion of code.

Profiling capability is available in the 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x C source debuggers and simulators. Profiling is supported in versions that run on Windows<sup>™</sup>, OS/2<sup>™</sup>, and SunOS<sup>™</sup> operating systems.

## 16.2 TMS320 Software Simulators

A TMS320 simulator is a software program that simulates the TMS320 microprocessor and microcomputer modes for cost-effective TMS320 software development and program verification in other than real time. With the inexpensive software simulator, you can debug without target hardware. Files can be associated with I/O ports so that specific I/O values can be used during test and debug. Time-critical code, as well as individual portions of the program, can be tested. The clock's counter allows loop timing during code optimization. Breakpoints can be established according to read/write executions (using either program or data memory) or instruction acquisitions.

Each of the TMS320 simulator's software programs simulates TMS320 operation and allows monitoring of the state of the TMS320. Simulation speed is typically on the order of thousands of instructions per second (SPARC) or hundreds of instructions per second (IBM PC). TMS320 simulators are available for the 'C1x, 'C2x, 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x devices. The 'C8x simulator is shipped with the 'C8x software tool kit for the Sun development platform.

### 16.2.1 Simulator Key Features

Key features common to the TMS320 software simulators include:

- ☐ Execution of user-oriented DSP programs on a host computer
- ☐ Modification and inspection of registers
- ☐ Data and program memory modification and display:
  - Modification of an entire block at any time
  - Initialization of memory before a program is loaded
- ☐ Simulation of peripherals, caches, and pipelined timings
- ☐ Extraction of instruction cycle timing for device performance analysis
- ☐ Programmable breakpoints on:
  - Instruction acquisition
  - Memory reads and writes (data or program)
  - Data patterns on the data bus or the program bus
  - Error conditions
- ☐ Trace on:
  - Accumulator
  - Program counter
  - Auxiliary registers

- ☐ Single-stepping of instructions
- ☐ Interrupt generation at user-specified intervals
- ☐ Error messages for:
  - Illegal opcodes
  - Invalid data entries
- ☐ Execution of commands from a journal file
- ☐ Use of save states for restarting simulation ('C25)
- ☐ Simulation of the entire instruction set for the appropriate device
- ☐ Simulation of the peripheral's key features for the appropriate device ('C1x, 'C2x, 'C2xx, 'C3x, 'C4x)
- ☐ Command entry from either menu-driven keystrokes (menu mode) or line mode ('C1x, 'C2x, 'C3x, 'C4x)
- ☐ Simulation parameters quickly stored/retrieved from files to facilitate preparation for individual sessions
- ☐ Reverse assembly for editing and reassembling source statements
- ☐ Memory that can be displayed (at the same time) as
  - Hexadecimal 16-bit values
  - Assembled source code
- ☐ Execution modes
  - Single/multiple instruction count
  - Single/multiple cycle count
  - Until condition is met
  - While condition exists
  - For set loop count ('C2xx, 'C3x, 'C4x, 'C5x, 'C54x)
  - Unrestricted run with halt by keyed input
- ☐ Trace execution with display choices
  - Designated expression values
  - Cache memory ('C3x, 'C4x)
  - Instruction pipeline for easy optimization of code ('C2xx, 'C3x, 'C4x, 'C5x, 'C54x)
- ☐ Cycle counting
  - Display of the number of clock cycles in a single-step operation or in the run mode
  - Externally generated mode that can be configured with wait states for accurate cycle counting ('C1x, 'C2x, 'C2xx, 'C3x, 'C4x)

The simulators use TMS320 object code produced by the TMS320 macro assembler/linker or ANSI C compiler. Input and output files can be associated with the port addresses of the I/O instructions to simulate I/O devices connected to the processor. Each interrupt flag can be set periodically at a user-defined interval for simulating an interrupt signal. Before program execution is initiated, breakpoints can be defined (a branch to *self* is detected), and the trace mode set (execution is halted).

Once program execution is suspended, the internal registers and both program and data memories can be inspected and/or modified. The trace memory can also be displayed. A record of the simulation session can be maintained in a journal file so it can be reexecuted to regain the same machine state during another simulation session.

### 16.2.2 TMS320C1x Simulator

The 'C1x software simulator supports all devices in the TMS320C1x generation and offers the same common features as the 'C2x and 'C5x simulators (see Section 16.2.1, Section 16.2.3, and Section 16.2.7). In addition, the 'C1x simulator has an I/O file associated with eight ports.

### 16.2.3 TMS320C2x Simulator

The 'C2x simulator's software program simulates the operation of the 'C2x generation of DSPs. The simulator has commands that specify wait cycles for external data, program, and I/O memory, resulting in a more flexible, accurate timing analysis for interrupt generation at user-specified intervals. The simulator uses a TMS320 debugger's interface (described in Section 16.1) that allows you to debug code in C, assembly, or both.

In addition to the common features listed in Section 16.1, the 'C2x simulator also includes:

- ☐ File-associated I/O with 16 ports
- ☐ Programmable breakpoints on:
  - Instruction acquisition
  - Memory reads and writes (data or program)
  - Data patterns on the data bus or the program bus
  - Error conditions
- ☐ Commands to modify and inspect both registers and individual locations in a register

#### 16.2.4 TMS320C2xx Simulator

The 'C2xx software simulator uses the TI high-level language (HLL) debugging interface. In addition to the features listed in Section 16.1, it also simulates the serial port and timer peripherals.

The simulator lets you verify and monitor the state of the processor without having to install additional hardware. The 'C2xx software simulator performs:

- ☐ Modeling of the 'C2xx addressable memory
- ☐ Modeling of the 'C2xx additional features
- ☐ Operation of the debugging interface

#### 16.2.5 TMS320C3x Simulator

The 'C3x simulator's software program simulates the operation of the 'C3x generation of 32-bit, floating-point digital signal processors and aids in the development of effective software. The simulator uses the standard C/assembly source debugger interface, allowing the user to debug code in C, assembly, or both. The 'C3x simulator also simulates external interrupts to the 'C3x device and cache utilization.

The simulator lets you verify and monitor the state of the processor without having to install additional hardware. The 'C3x software simulator performs:

- ☐ Modeling of the 'C3x addressable memory
- ☐ Modeling of the 'C3x additional features
- ☐ Operation of the debugger's interface

#### 16.2.6 TMS320C4x Simulator

The 'C4x software simulator uses the TI debugger's interface. This flexible debugging interface lets you view both C language and assembly language simultaneously and can execute single-stepping and software breakpoints on either language for HLL debug (see Section 16.1). The 'C4x simulator also simulates cache utilization.

The simulator lets you verify and monitor the state of the processor without additional hardware. The 'C4x software simulator performs:

- ☐ Modeling of the 'C4x addressable memory
- ☐ Modeling of the 'C4x additional features
- ☐ Operation of the debugger's interface

#### 16.2.7 TMS320C5x Simulator

The 'C5x software simulator uses the TI HLL debugging interface. In addition to the features listed in Section 16.1, it also simulates the serial port and timer peripherals.

The simulator lets you verify and monitor the state of the processor without having to install additional hardware. The 'C5x software simulator performs:

- ☐ Modeling of the 'C5x addressable memory
- ☐ Modeling of the 'C5x additional features
- ☐ Operation of the debugging interface

### 16.2.8 TMS320C54x Simulator

The 'C54x software simulator also uses the TI HLL debugging interface and, in addition to the features listed in Section 16.1, simulates the serial port and timer peripherals.

The simulator lets you verify and monitor the state of the processor without having to install additional hardware. The 'C54x software simulator performs:

- ☐ Modeling of the 'C54x addressable memory
- ☐ Modeling of the 'C54x additional features
- ☐ Operation of the debugging interface

### 16.2.9 TMS320C8x Simulator

The 'C8x simulator software uses the standard TMS320 debugger interface to simulate the operation of the 'C8x master and parallel processors on the host processor rather than targeting an actual 'C8x target system. The simulator can be used to benchmark and to evaluate the 'C8x or to assist in code development when a target system is not yet available. This Sun-based software simulator provides cycle-by-cycle simulation of the 'C80 or 'C82.

Special display features include:

- ☐ An image display that shows a grayscale or color representation of an image stored in memory
- ☐ A data-flow plot that provides cycle-by-cycle visual representation of processor status and memory accesses.



## 16.3 TMS320 System Debugging and Evaluation Tools

The TMS320 family includes a full range of system debugging tools that can be used as sample target systems in evaluation and application development. Included in this broad line of tools are:

- ☐ DSK—DSP Starter Kits
- ☐ EVM—evaluation modules
- ☐ XDS™—eXtended Development Support emulators

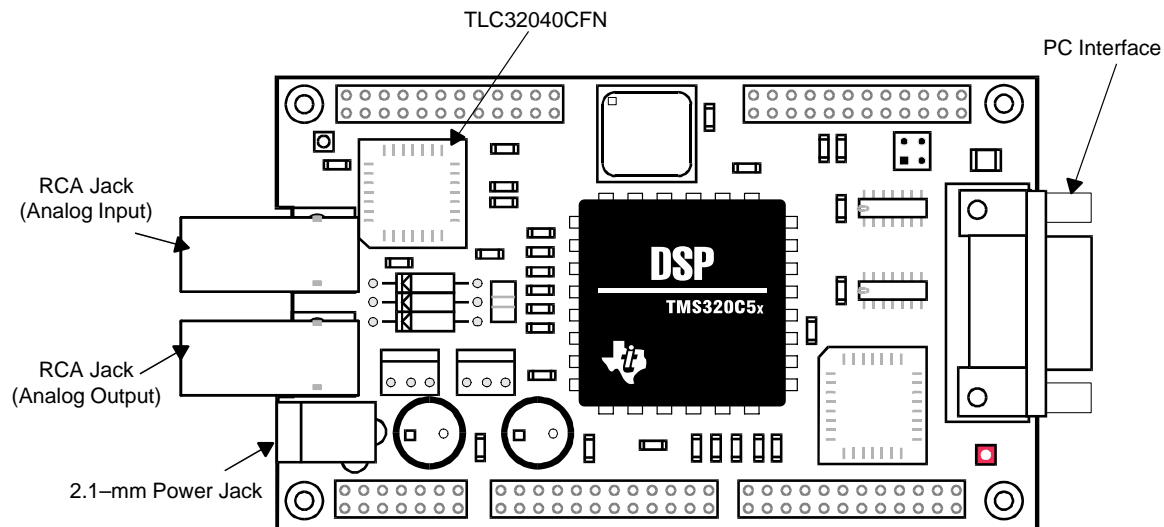
### 16.3.1 DSP Starter Kit (DSK)

The TI TMS320 DSP Starter Kit (DSK) (see Figure 16–3) is an ideal low-cost tool for first-time users interested in evaluating a DSP platform. Available for the 'C2x, 'C3x, 'C5x, and 'C54x DSPs, the DSK allows you to experiment with and use a DSP for real-time signal processing with the benefits of hardware execution and software support. With the analog-ready interface, you can easily benchmark and test applications such as control systems, audio, and speech processing. The DSK allows you to write and run real-time source code, evaluate that code, and debug your system.

Each DSK comes complete with a TMS320-based board, its own easy-to-use assembler/linker and debugger, and a documentation package. The DSK board contains:

- ☐ An RS-232 serial port ('C2x, 'C5x) or parallel printer port ('C3x) for communicating with your PC
- ☐ A 2.1-mm jack that allows you to attach a simple wall-mounted ac or dc transformer as your power supply (The 'C2x and 'C5x support ac only.)
- ☐ Two standard RCA jacks (for analog I/O) that provide direct connections to a microphone, speaker, or other analog device
- ☐ An on-board EPROM that allows the DSK to communicate with your PC ('C5x only)
- ☐ 1.5K words of on-chip RAM on the 40-MHz 'C2x board, 10K of on-chip RAM words on the 40-MHz 'C5x board, or 2K words of on-chip RAM on the 50-MHz 'C3x board

Figure 16–3. DSP Starter Kit (DSK)



The DSK assembler key features include:

- ☐ A simple and easy-to-use interface into which only the most significant features of an assembler have been incorporated
- ☐ Special directives to assemble code at an absolute address during the assembly phase. The linking function is also handled by the assembler. As a result, programs are created quickly and easily.

The DSK debugger key features include:

- ☐ An easy-to-use, window-oriented interface that enables you to download, execute, and debug assembly code
- ☐ A small command set that reduces the number of instructions the user must learn

The TMS320 DSKs run on a PC-AT with MS-DOS or PC-DOS (version 4.01 and later).

## 16.3.2 Evaluation Modules

TMS320 evaluation modules (EVMs) are low-cost development boards used for device evaluation, benchmarking, and limited system debug. EVMs are PC add-in boards that include the target processor, a small amount of memory, and limited peripherals that allow you to run code in real time and interface to an external system. EVMs are available for the 'C16, 'C26, 'C30, 'C50, and 'C54x.

Common TMS320 EVM features include:

- ☐ Modification/display of memory and registers
- ☐ Assembler/linker
- ☐ Software single-step and breakpoint capabilities
- ☐ On-board memory
- ☐ Host upload/download capabilities
- ☐ I/O capability
- ☐ HLL-debug interface

### 16.3.2.1 TMS320C16 EVM

The 'C16 EVM is a low-cost, PC-AT plug-in card that lets you evaluate certain characteristics of the 'C1x DSPs to determine whether they meet the requirements of an application. The 'C16 EVM carries a 'C16 DSP on board to allow full-speed verification of your 'C1x code. The 'C16 DSP is a speed and memory superset of the 'C10 and the 'C15, and its peripherals are identical to the peripherals of both of those devices. Therefore, the 'C16 EVM can be used to evaluate the suitability of the 'C10, 'C15, or 'C16 for a given application.

Other key features of the TMS320C16 EVM include:

- ☐ 32-MHz operation
- ☐ Single-step and breakpoints
- ☐ 64K external program static RAM (SRAM) on board
- ☐ Easy-to-use, windows-oriented, mouse-controlled user interface that features windows displaying CPU registers, memory locations, disassembled code, and other variables needed for debug
- ☐ TMS320 fixed-point assembler/linker

### 16.3.2.2 TMS320C26 EVM

The 'C2x EVM carries a 'C26 DSP on-board to allow full-speed verification of 'C2x code. The 'C26 DSP has 1568 words of on-chip RAM; it is pin compatible to the 'C25 and its peripherals are identical to the peripherals of the 'C25. Therefore, the 'C2x EVM can be used to evaluate the suitability of the 'C26 and 'C25 for a given application.

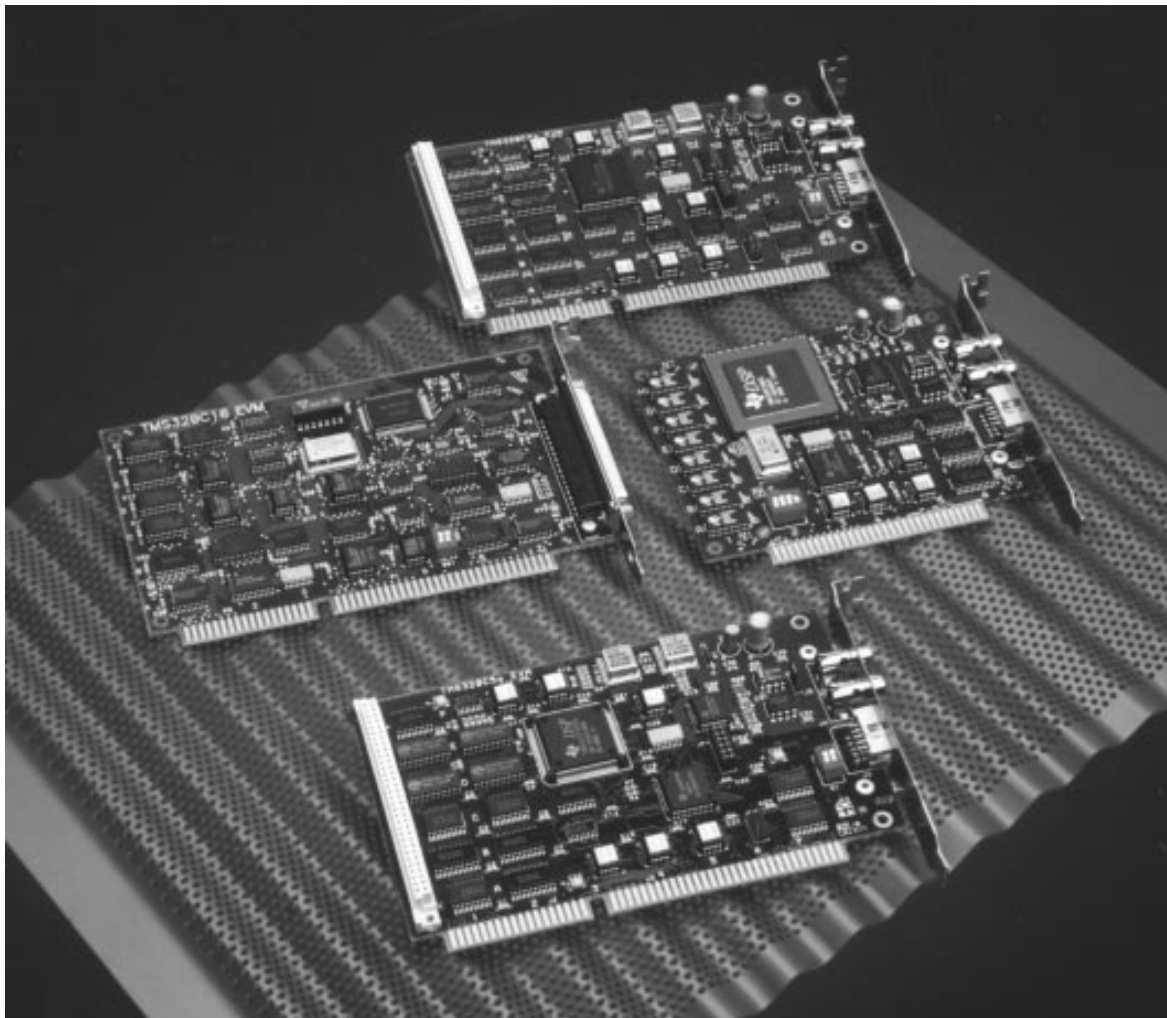
Key features of the 'C2x EVM include:

- ☐ 80-ns instruction cycle time
- ☐ 64K external zero wait-state SRAM on-board
- ☐ Voice-quality analog data acquisition through the TLC32046 analog interface circuit
- ☐ Standard RCA analog-I/O connectors for direct connection to microphone and speaker
- ☐ External TDM serial port
- ☐ 16-bit bidirectional PC host-communications port
- ☐ I/O expansion bus for application use
- ☐ On-board emulation logic for source debugger support
- ☐ IBM PC compatible, 16-bit half-card, mappable in one of four memory locations

#### **16.3.2.3 TMS320C30 EVM**

The 'C3x evaluation module (see Figure 16–4) hosts a 'C30 DSP on board to allow full-speed verification of 'C3x code.

Figure 16–4. TMS320 EVMs



The 'C3x EVM enables you to benchmark and evaluate code in real time while the device is operating at 33 MHz in the rich development environment of the 'C3x assembler/linker and C/assembly source debugger interface. Applications can be benchmarked and tested easily with the analog-ready interface.

The 'C3x EVM comes complete with a PC half-card and software package. The EVM board contains:

- ☐ One 'C30 — a 33-MFLOPS, 32-bit, floating-point DSP
- ☐ 16K-word, zero wait-state SRAM, allowing coding of most algorithms directly on the board

- ☐ A speaker/microphone-ready analog interface for multimedia, speech, and audio applications development
- ☐ An external serial-port interface that can be used for connecting multiple EVMs or for extra analog interfacing
- ☐ A host port for PC communications
- ☐ Embedded emulation support through the SN74ACT8990 test-bus controller

The system also comes with all of the software required to begin application development on a PC host:

- ☐ The window-oriented, mouse-controlled interface supports downloading, executing, and debugging of assembly code or C code.
- ☐ The 'C3x assembler/linker is also included with the EVM. For HLL programming, the optimizing ANSI C and the Ada compilers are offered separately.

#### **16.3.2.4 TMS320C50 EVM**

The 'C5x EVM carries a 'C50 DSP on-board to allow full-speed verification of 'C5x code. The 'C50 DSP has 10K on-chip ROM; it is pin compatible with the 'C51 and 'C53 and its peripherals are identical to the peripherals of those devices. Therefore, the 'C5x EVM can be used to evaluate the suitability of the 'C50, 'C51, or 'C53 for a given application.

Because the 'C5x generation is upward source-code compatible with the 'C2xx generation, the 'C5x EVM is used to develop code for 'C2xx devices.

Key features of the 'C5x EVM include:

- ☐ 50-ns instruction cycle time
- ☐ 64K-external zero-wait-state SRAM on board
- ☐ Voice quality analog data acquisition through the TLC32046 analog interface circuit
- ☐ Standard RCA connector analog input and output for direct connections to microphone and speaker
- ☐ Embedded emulation support by way of the SN74ACT8990 test-bus controller (TBC)
- ☐ 16-bit bidirectional PC host-communications port
- ☐ I/O expansion bus for application use
- ☐ IBM PC-compatible 16-bit half card, mappable in one of four memory locations

#### **16.3.2.5 TMS320C54x EVM**

The 'C54x EVM is a PC/AT plug-in card that lets you evaluate certain characteristics of the 'C54x DSP to see whether the DSP meets your application requirements. You can also create your software to run on board or expand the system in a variety of ways.

The 'C54x EVM carries of 'C541 DSP on board to allow full-speed verification of 'C54x code. The 'C541 has 5K bytes of on-chip program/data RAM, 28K bytes of on-chip ROM, two serial ports, a timer, access to 64k bytes each of external program and data RAM, and an external analog interface for evaluation of the 'C54x family of devices for a given application.

The 'C54x EVM has the following features:

- ☐ 'C541 operating at 40 MIPS with 128K words of zero wait-state memory
- ☐ Voice-quality analog interface to line I/O or speaker/microphone (user-selectable) through standard RCA connectors
- ☐ External serial port
- ☐ Parallel I/O-expansion bus
- ☐ Two 16-bit bidirectional host-/target-communication channels; one channel contains 64 words of buffering
- ☐ Embedded emulation support based on the IEEE 1149.1 standard
- ☐ A single 16-bit ISA half-card, mappable to one of four I/O locations

#### **16.3.2.6 TMS320C8x Software Development Board (SDB)**

The 'C8x SDB is a full-featured PC add-in board (see Figure 16–5) that helps designers create 'C8x-based applications that require high-speed data input and output in a Windows NT development environment. The SDB provides the system to acquire audio and video and to develop, benchmark, and debug code for any environment.

Key features of the 'C8x SDB include:

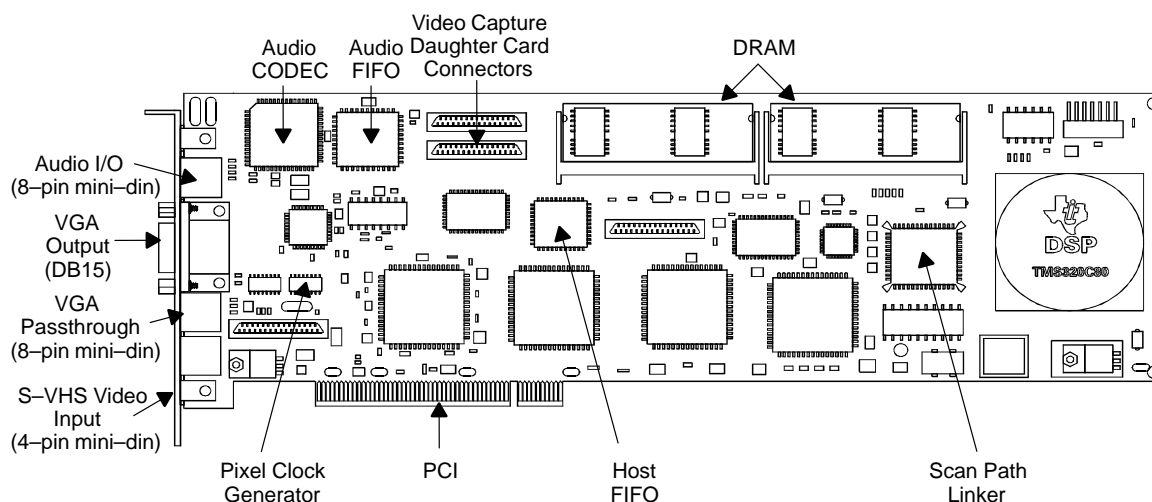
- ☐ 40-MHz 'C80
- ☐ PCI bus master interface
- ☐ 16-bit, 44.1-kHz stereo audio subsystem
- ☐ 16-bit video acquisition subsystem

- ☐ 8 Mbytes DRAM for program memory
- ☐ 2M-byte display VRAM to support 16-bit (1024 × 768) video applications
- ☐ Programming examples
- ☐ Real-time full-scan emulation environment

The video display feature allows video, whether captured or generated by the 'C80, to be output to any standard VGA monitor. Real-time video overlay features are implemented through an on-board analog video multiplexer.

The video-capture daughter card for the 'C8x SDB allows an analog video input signal to be digitized, decoded, and sent to FIFO memory for processing by the 'C80. Supported video formats include NTSC, PAL, and S-VHS.

Figure 16–5. TMS320C8x Software Development Board (SDB)





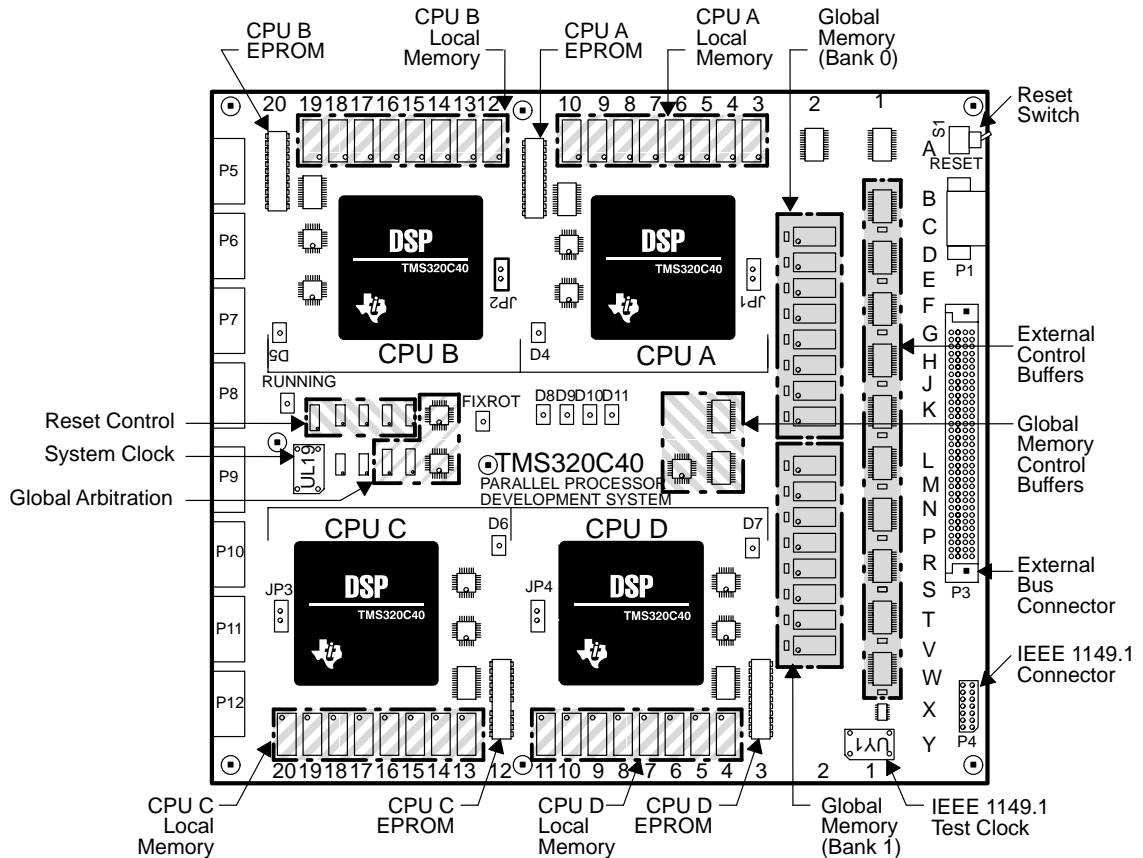
### 16.3.2.7 TMS320C4x Parallel Processing Development System

The 'C4x parallel processing development system (PPDS) (see Figure 16–6) is the first development board designed exclusively to evaluate and develop parallel-processing, floating-point software applications. You can develop, benchmark, and evaluate code in real time in a rich development environment with the power and speed of the 'C4x PPDS. For a complete system, the XDS510 is necessary.

Key features of the PPDS include:

- ☐ Four on-board 'C40 parallel processors. Each 'C40 is supported by a local bus consisting of:
  - 64K × 32-bit words of zero wait-state SRAM
  - 8K bytes of EPROM
- ☐ 128K × 32-bit words of one wait-state SRAM on a shared global bus
- ☐ An expansion bus connector that provides an external interface to the shared global-memory bus
- ☐ Eight external communication connectors that provide an interface for connecting off-board 'C40s and external peripherals to the PPDS 'C40s.
- ☐ An IEEE Standard 1149.1-compliant (JTAG) test connector that serves as an interface for connecting the XDS510 in-system emulator

Figure 16–6. The TMS320C40 PPDS Board Layout



The PPDS is placed on the desktop and is controlled through the XDS510, available separately. The PPDS is shipped with a dedicated desktop stand and its own 20-A, 50-W power supply. You also need a C compiler.

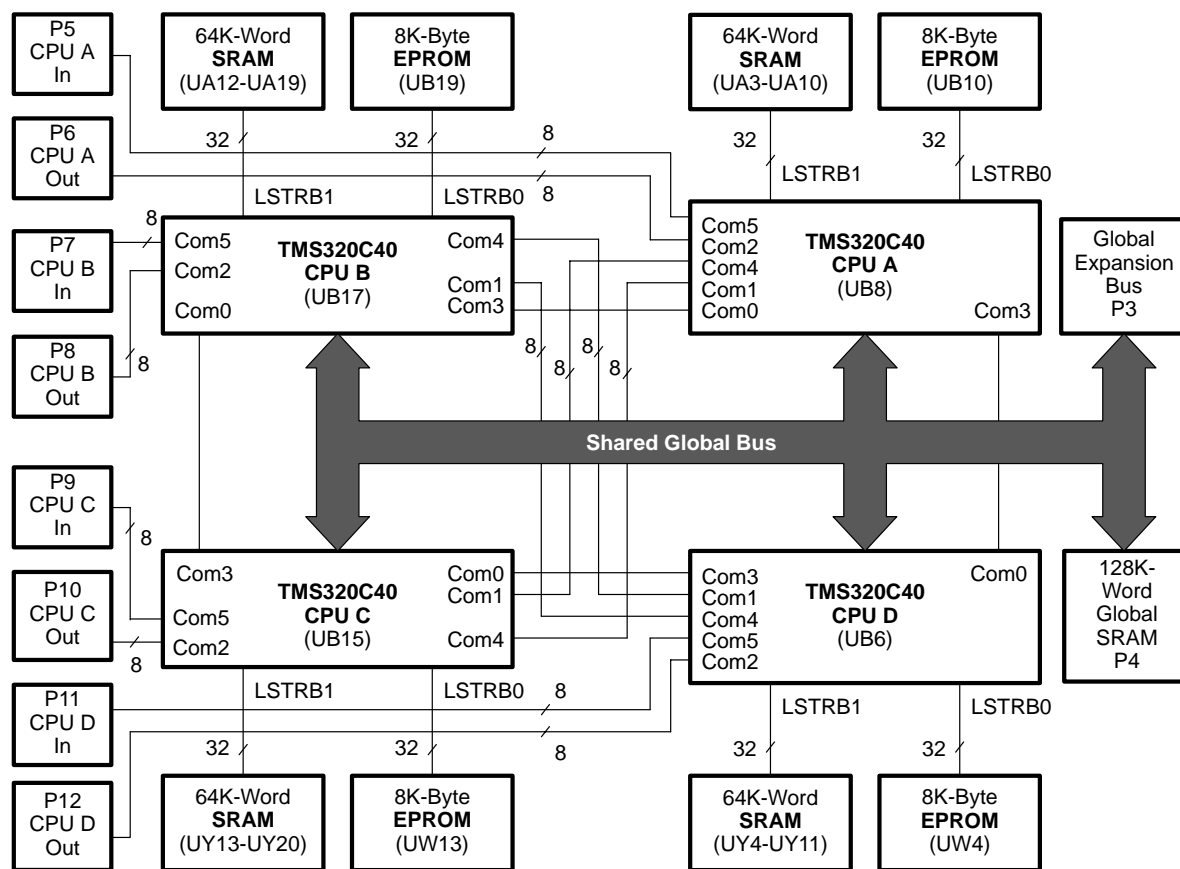
Each 'C40 on the PPDS has direct connections to each of the other 'C40s in the system through the communication ports, allowing you to experiment with various parallel-processing topologies that are best suited for your end application. In addition, each 'C40 also has two communication ports pinned out to external connectors on the left edge of the board, allowing other 'C40-based boards or peripheral boards to be connected to the 'C40s on the PPDS.

The 'C40s are also connected on a shared bus (see Figure 16–7) that has arbitration logic to decide which 'C40 receives access to the shared bus at any given time. The shared bus is brought to a connector, allowing DRAM, data acquisition, and other shared resources to be added to the PPDS.

Even though the PPDS is used with the XDS510, each 'C40 has its own source-level debugging window for code development.

These features give you the flexibility to distribute tasks between multiple processors and to develop, benchmark, and debug multiprocessing algorithms.

Figure 16–7. TMS320C40 PPDS Block Diagram



### 16.3.3 TMS320 Emulators

The TMS320 extended development systems (XDSs) are powerful, full-speed emulators used for system-level integration and debug. TI provides conventional in-circuit emulators (XDS/22) as well as in-system scan-based emulators (XDS510/XDS510WS). The XDS/22 supports the 'C1x (except 'C16) and 'C2x DSPs. The XDS510/XDS510WS emulator is currently available for the 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x DSPs.

#### 16.3.3.1 In-Circuit Emulators (XDS/22)

There are currently four different versions of the XDS/22: three for the 'C1x and one for the 'C2x. The 'C10/C15 emulator emulates operation of the 'C10, 'C10-25, 'C15, and 'C15-25; other models are available to support the 'C14 and 'C17. The 'C2x emulator supports the 'C25 and 'C26 devices.

Key features of the 'C1x/C2x emulators include:

- ☐ 25-MHz, full-speed, in-circuit emulation ('C1x)  
40-MHz, full-speed, nonintrusive, in-circuit emulation ('C2x)
- ☐ Dual-inline target connector with optional PLCC target connection ('C1x)  
PLCC target connector with a pin-grid-array adapter ('C2x)
- ☐ Software development, microcomputer, and microprocessor modes ('C1x),  
4K words each of program and data high-speed SRAM; 64K-word DRAM  
expansion/communications board ('C2x)
- ☐ Breakpoint, trace, and time-stamping (BTT) capabilities with logic analyzer  
interface cable
- ☐ Single-step execution
- ☐ Line-by-line, reverse, or patch assembler
- ☐ Enhanced decimal parameter entry and display
- ☐ Host-independent uploading/downloading of program and data memory
- ☐ Ability to inspect/modify all internal registers
- ☐ Logic tracking with extended data and address probes

The XDS/22 emulator can be configured to operate in one of four modes.

- ☐ Stand-alone: requires only the XDS/22 and your terminal
- ☐ Host computer: allows TMS320 programs to be written on a familiar editor,  
assembled, and then downloaded into the XDS/22

- ☐ PC (single-user system): supports host uploads/downloads over a single port to allow a single-user system to function as both a terminal and host
- ☐ Multiprocessor: allows up to nine XDS/22s to be connected and controlled by a single terminal

The XDS/22 emulator provides communication links to standard RS-232C ports and has debugging capabilities with a prompting monitor and full-speed hardware breakpoints and trace. The communications system establishes links with the user's terminal, a PROM programmer or printer, and a host computer system. Each XDS/22 unit is equipped with four standard RS-232C ports for communications with external devices.

A powerful set of commands is available for full debugging of the target system and complete control of both the emulator functions and the target system. Features of the debugging commands include flexibility in defining test conditions and BTT operations.

The following items are packaged with both the 'C1x and 'C2x emulators:

- ☐ XDS/22 chassis
- ☐ Emulator board (and appropriate device) with target connector cable
- ☐ BTT board with a logic analyzer interface cable
- ☐ Communications board
- ☐ RS-232C cable for connection between the XDS and a PC
- ☐ Trace-probe cable to connect the BTT board to the target system

### **16.3.3.2 Scan-Based Emulators (XDS510/XDS510WS)**

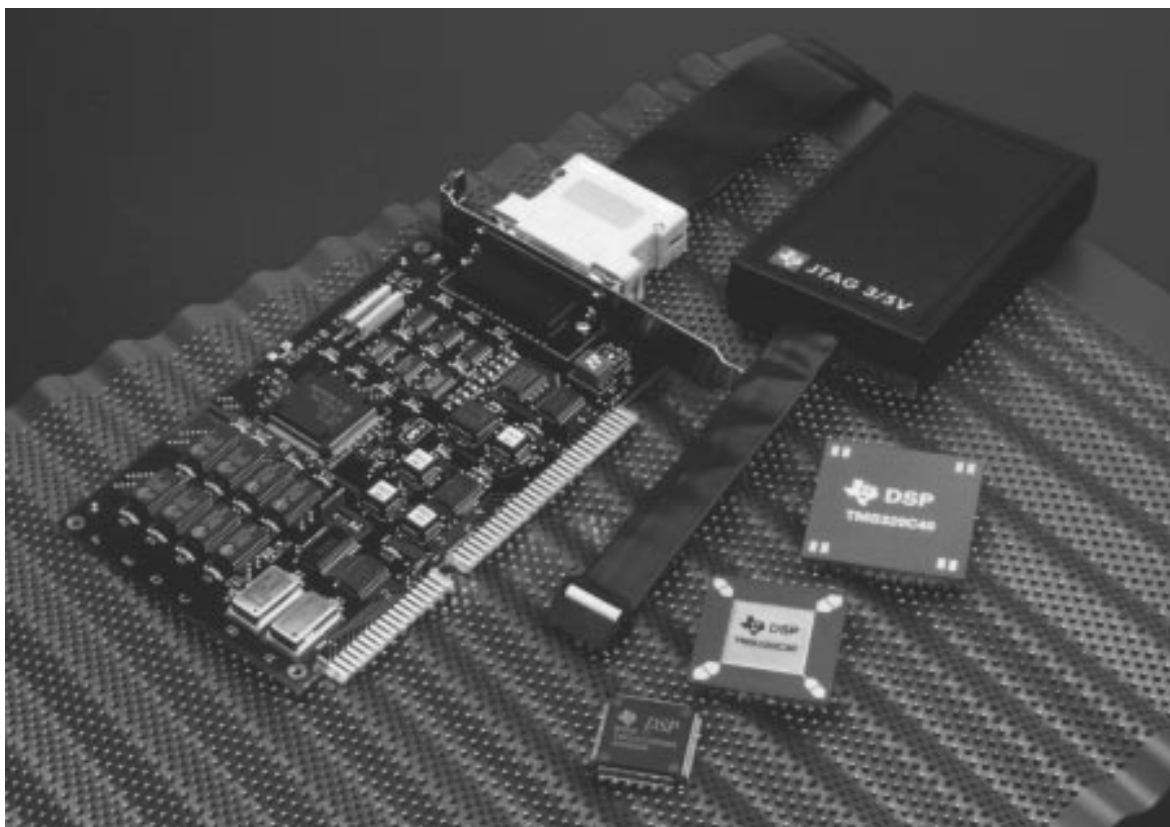
Scan-based emulation is a unique, nonintrusive approach to system emulation, integration, and debug. This approach was conceived and developed by TI to address hardware and software characteristics (reduced internal bus visibility, highly pipelined architectures, fast cycle times, and high-density packaging) that are inherent to sophisticated very-large-scale integration (VLSI) systems.

Scan-based emulation eliminates special bond-out emulation devices, target cable/buffer signal degradation, and the mechanical and reliability problems associated with target connectors and surface-mount packaging. With scan-based emulation, your program can execute in real time from internal or external target memory; no extra wait states are introduced by the emulator at any clock speed.

The TMS320 DSP device's architecture implements scan-based emulation through internal, shift-register scan paths accessed by a single serial interface. The scan paths provide access to internal device registers and state machines, allowing complete visibility and control. This nonintrusive approach even operates in a production environment where the DSP is soldered into a target system.

The XDS510/XDS510WS emulators are user-friendly, PC- or Sun-based development systems, that have all the features necessary to perform full-speed, scan-based emulation with the 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x DSPs. They are the first scan-based emulators that are capable of parallel processing. These emulators make it possible to develop hardware and software and to integrate the hardware and software with the target system. A revolutionary five-wire interface acts as a scan path to every memory and register location in the DSP device (see Figure 16–8). The XDS510WS offers the same functionality for the SPARC workstation.

*Figure 16–8. TMS320 XDS510 Scan-Based Emulators*



Key features of the XDS510 include:

- ☐ Full-speed execution and monitoring of the device within your target system through a 14-pin target connector (12-pin target to support MPSPD emulation on 'C3x)
- ☐ Global run/stop/breakpoint of parallel-processing DSPs
- ☐ HLL debugging interface
- ☐ Software breakpoint/trace and timing with up to 200 software breakpoints
- ☐ Hardware breakpoint/trace on all program and data addresses
- ☐ Single-step execution
- ☐ Interfacing and debugging with C/assembly source debugger
- ☐ Loading/inspection/modification of all registers and memory
- ☐ Benchmarking of execution time of clock cycles

Full-speed emulation and monitoring of the target system is performed serially through a cable that runs from the XDS510 to the target system. The scan path controls the device within the targeted application and provides access to all the registers, as well as to the internal and external memory of the device. Since program execution takes place in the DSP device of the target system, there are no timing differences during emulation. This new emulation technology offers significant advantages over traditional emulators. These advantages include:

- ☐ No cable-length-transmission-line problems
- ☐ Nonintrusive system
- ☐ No loading problems on signals
- ☐ No artificial-memory limitations
- ☐ Common-screen interface for easy usage
- ☐ Easy installation
- ☐ In-system emulation
- ☐ No variance from the device's data sheet specifications

Software breakpoints allow program execution to be halted at a specified instruction address. When a given breakpoint is reached, the program stops execution. At this point, the status of the registers and of the CPU is available.

Their contents are visible in the appropriate windows; to view the contents of other memory locations, only one command is required.

Software trace lets you view the state of the device when a breakpoint is reached. This information can be saved in a file for future analysis. Software timing allows you to track the clock cycles between breakpoints for benchmarking of time-critical code.

Single-step execution gives you the capability to step through the program one instruction at a time. After each instruction, the status of the registers and CPU is displayed. This provides greater flexibility during software debugging and helps reduce the development time.

Object code can be downloaded to any valid memory location (program or data) via the scan path interface. Downloading a 1K-byte object program typically takes 100 ms. In addition, by inspecting and modifying the registers while single-stepping through a program, you can examine and modify program code or parameters.

The XDS510 is supported by the TMS320 standard debugger's interface for fast, easy debugging of C and assembly source code.

The emulator's configurability gives your system flexibility. You can configure both memory and screen color. The address range, memory type, and access type assigned to each location can be configured also. The memory map, which may include EPROM, SRAM, DRAM, SDRAM, and on-chip memory and peripherals, can be configured to reflect the actual peripheral environment of the target system, including wait states and access privileges.

The 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x XDS510 emulator packages include:

- ☐ XDS510 emulator PC board
- ☐ IEEE Standard 1149.1 (JTAG<sup>†</sup>) or MPSD target cable
- ☐ 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, or 'C8x user interface software (sold separately)

All XDS510 systems use the IEEE 1149.1 target cable, except the 'C3x XDS510 which uses the MPSD cable.

The XDS510 emulator operates on a PC-AT system and requires one 16-bit slot.

<sup>†</sup> IEEE Std 1149.1-1990, IEEE Standard Test Access Port and Boundary-Seam Architecture



## 16.4 Code Composer™ –An Integrated Development Environment (IDE)

GO DSP Corporation's Code Composer is an alternate solution to the standard TMS320 debugger's interface described in Section 16.1, TMS320 Debugger's Interface (C/Assembly Source Debugger). Code Composer, a fully integrated development environment (IDE) for TI DSPs, offers, for the first time, features and productivity gains found only in mainstream software development environments (such as Microsoft's Visual C++™). Code Composer also includes features specifically tuned for the DSP software designers and is currently available for the 'C2xx, 'C3x, 'C4x, 'C5x, and 'C54x. Nearly all of Code Composer's main features are new to the DSP market and unite the environment functionality of high-

and low-level DSP debuggers, signal probes and scopes (as found in block diagram tools), and graphical profiling, all in a tightly integrated MS Windows™ (and Windows 95) application.

### 16.4.1 Primary Features

Code Composer includes all the major features provided by the HLL debugger (see Section 16.1). The following advanced features are also included in the Code Composer environment:

- ☐ **A fully integrated environment using TI's compiler (IDE).** Code Composer integrates a project management system, built-in editor, and full debugging and profiling capabilities in a single Windows environment.
- ☐ **Project management for C and DSP assembly files.** The project management system keeps track of all files and their dependencies. This allows Code Composer to save you compile time by recompiling only those files that have changed since the last compile.
- ☐ **Tightly integrated editor tuned for writing C and DSP assembly code.** The built-in editor of Code Composer supports dynamic syntax highlighting for both C and assembly files. Syntax highlighting makes your code easier to read and can help you spot critical syntax errors very easily.
- ☐ **Background compiling while editing and debugging.** There is no need to shell-out to a DOS environment to execute your compiler/assembler tools. Code Composer automatically launches these tools in its environment. Errors are highlighted in Code Composer's build window. You can double click on errors to go directly to the point where the error occurred.
- ☐ **Multiprocessor support under native MS Windows with floating PDM.** Code Composer supports full multiprocessing in Windows 3.1 and Windows 95. The parallel debug manager (PDM) allows you to broadcast commands to all (or the selected group) of processors.

- ☐ **Graphic window scope probes to watch signals at any algorithm point.** Graphical display windows allow the user to view signals in time domain or frequency domain. For frequency domain graphs, the FFT is performed on the host; this allows you to view the spectrum of the interested signal without any modification to its DSP code. Graphical displays can also be connected to a probe point. A probe point (when set at a particular location in the algorithm) specifies when the graphical display window should be updated. This allows you to take a snapshot of the signal when execution of the code reaches that point.
- ☐ **File probes to extract or inject signals/data at any algorithm point via files.** Instead of reading signals in real time, Code Composer allows you to stream signals from/to your PC. This allows you to simulate your algorithm (on the DSP target) with known samples.
- ☐ **Graphical profiling.** Code Composer's profiling capabilities are integrated within its environment.
- ☐ **Execution of user's DOS program in the background ("system" command).** You can execute any DOS programs from within Code Composer and have the output piped to Code Composer's output window. This allows you to integrate your own applications to Code Composer.
- ☐ **State-of-the-art watch window.** Code Composer's watch window allows you to enter any C expression or any variable of interest. Structures, arrays, and pointers can easily be recursively expanded or collapsed. This allows you to drill down complex structures.
- ☐ **Algebraic disassembly window.** The disassembly window gives you the option to view the disassembled opcodes in algebraic C format making the disassembled code much easier to read.
- ☐ **Help on the target DSP.** On-line help on the DSP instruction and registers means that you don't have to carry your User's Guide everywhere.
- ☐ **User extensible.** The GO DSP Corporation's Extension Language (GEL) allows you to add your own menu items to Code Composer's menu bar.

## **16.4.2 Using Code Composer as a Complete Development Environment**

Code Composer tightly integrates Texas Instruments compiler, assembler, and linker tools into its development environment. With Code Composer, users can launch TI's tools from the menu bar and see the compiler output, piped directly to a window, as it happens. Error messages are highlighted, and double clicking on the error message opens the source file and positions the cursor on the line in question. DOS-based TI tools are smoothly multitasked in the background under Windows so users can easily edit source files, debug programs, and compile, all at the same time. Code Composer keeps track of all files and file dependencies (C and assembly source) in a project. The user can choose to compile individual files, to build all files in the project, or to build the project incrementally. Easy-to-use dialog boxes are available for compiler, assembler, and linker options.

The Code Composer watch window allows the user to easily “drill down” through complex structures. Variables such as arrays, structures, and pointers can be expanded and collapsed recursively by simply placing the cursor on the variable of interest and pressing the ENTER key. In addition, variables added to the watch window can be edited by simply double clicking on the desired variable. Any C-expression as well as a GEL function can be added to the watch window. By adding a GEL function to the watch window, the GEL function is executed at every breakpoint. From within the called GEL function, more complex tasks can then be performed and the results piped to any output window.

Probe points allow you to observe signals or to inject or extract data at a certain point in the algorithm. Probe points can be connected to any instruction point and memory area. When a designated point in the algorithm is reached, the connected signal probe captures data from the target DSP and displays it appropriately. If a file is connected to the designated point, data is streamed between a specified memory area and a file. Once the operation is complete, execution continues. This feature allows the developer to take snapshots of the target memory and inject or extract data via files at particular points in their algorithm. Using the animation feature, the developer can observe signals and execution to any detail by using real signals from the PC's disk, all with no change to the source code.

# TMS320 Technical Support

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In addition to development tools, Texas Instruments provides extensive technical support to assist customers during product design. This support is detailed in the following sections.

<b>Topic</b>	<b>Page</b>
<b>17.1 DSP World Wide Web Site .....</b>	<b>17-2</b>
<b>17.2 Technical Documentation .....</b>	<b>17-3</b>
<b>17.3 DSP Application Reports .....</b>	<b>17-4</b>
<b>17.4 TMS320 DSP Designer's Notebook Pages .....</b>	<b>17-9</b>
<b>17.5 University Textbooks .....</b>	<b>17-12</b>
<b>17.6 Technical Articles Bibliography .....</b>	<b>17-15</b>
<b>17.7 TMS320 Newsletter, <i>Details on Signal Processing</i> .....</b>	<b>17-18</b>
<b>17.8 TMS320 DSP Bulletin Board Service .....</b>	<b>17-19</b>
<b>17.9 TMS320 DSP ftp Site .....</b>	<b>17-21</b>
<b>17.10 TMS320 DSP Technical Hotline .....</b>	<b>17-22</b>

## 17.1 DSP World Wide Web Site

TI DSP maintains a site on the World Wide Web where you can find technical information about TI digital signal processing solutions. The data presented covers TI DSPs, linear and mixed-signal devices, development tools, and products of TMS320 third-party developers, including both hardware and software. Also available are technical resources including the On-Line DSP Lab™ and the 320 Hotline On-Line™. The On-Line DSP Lab allows you to “test drive” DSP design tools for free, right from your PC. Currently, the lab features the 'C3x and the 'C54x software tools and evaluation module (EVM) with debugger. The 320 Hotline On-Line is a searchable database that allows you to research various topics and retrieve technical answers 24 hours a day.

Technical documentation including user's guides, application reports, Designer's Notebook pages, data sheets, reference guides, and publications are also available.

The world wide web site address is **<http://www.ti.com/dsps>**.

## 17.2 Technical Documentation

A wide variety of technical literature is available to assist you through the design cycle. These documents include product and preview bulletins, data sheets, user's and reference guides, over 2500 pages of application notes, and textbooks offered by Prentice-Hall, John Wiley & Sons, and Computer Science Press. The latest product and documentation updates are given in the TMS320 quarterly newsletter, *Details on Signal Processing*, the TMS320 DSP Bulletin Board Service (BBS), and on the Internet in the DSP Solutions world wide web home page. To inquire about available TMS320 literature, call the TI Literature Response Center at:

**(800) 477-8924**

The DSP Solutions world wide web site (<http://www.ti.com/dsps>) contains electronic versions of most of the TMS320 technical documentation, including all data sheets and application reports currently available.

The following list describes the general contents of each major category of technical documentation available through the TI Literature Response Center.

- ☐ **Product bulletins** and product briefs give an overview of the devices and of development support within the TMS320 family, presenting capabilities, diagrams, and hardware and software applications.
- ☐ **User's guides** for TMS320 processors provide detailed information regarding the architecture of the device, its operation, assembly language instructions, and hardware and software applications.
- ☐ **Data sheets** include features, electrical specifications, block diagrams, timing characteristics, and mechanical data for each device.
- ☐ **Application reports** describe the theory and implementation of selected TMS320 applications, including algorithms, code, and block, schematic, or logic diagrams. Currently, there are over 2500 pages of application reports to support the TMS320 family.
- ☐ **The TMS320 newsletter**, *Details on Signal Processing*, which is published quarterly, updates TMS320 customers on product information and industry trends. To receive a free subscription to this newsletter in the United States, call (800) 477-8924, x 3543.
- ☐ **Technology brochures** provide an overview of various implementations of DSP technology in applications such as wireless communications.

## 17.3 DSP Application Reports

There are many reports to assist customers in designing TMS320 DSP applications. Some are available through the TMS320 DSP BBS; others are published in the TMS320 application books. Table 17–1 lists the application reports available.

You can view most of these application reports electronically at the DSP Solutions www site (<http://www.ti.com/dsp>).

Source code, which can be used to reduce design time and to bring TMS320-based products to market faster, is available through the BBS. Refer to Section 17.8, TMS320 DSP Bulletin Board Service, for more information.

**Note:**

Please contact the TI Product Information Center at (800) 477–8924 to request this literature or see the DSP Solutions www site.

*Table 17–1. Application Reports*

Application	Topic	Location/ Literature No.	Device
Data Communications	<i>An All-Digital Automatic Gain Control</i>	SPRA016	TMS320C17
	<i>Implementation of an FSK Modem Using the TMS320C17</i>	SPRA016	TMS320C17
	<i>Viterbi Implementation on TMS320C5x for V.32 Modems</i> (Mansoor Chishtie)	SPRA033	TMS320C5x
	<i>Digital Line Echo Cancellation Implementation on TMS320C5x DSP</i> (Kevin McCoy and Mansoor Chishtie)	SPRA033	TMS320C5x
Digital Cellular	<i>Cellular Phone: A Functional Analysis</i> (B.I. Pawate and Mansoor Chishtie)	SPRA033	TMS320C5x
	<i>IS-54 Simulation Package</i> (John Crockett/Steve Popik/Elliot Hoole)	SPRA033	TMS320C5x
	<i>U.S. Digital Cellular Error Correction Coding Algorithm Implementation on TMS320C5x</i> (Mansoor Chishtie)	SPRA033	TMS320C5x
	<i>A Performance Study of Two TMS320C53-Based Viterbi Algorithms for U.S. Digital Cellular Radio</i> (Mansoor Chishtie)	SPRA033	TMS320C5x
	<i>A TMS320C53-Based Advanced FEC Scheme for U.S.D.C. Radio</i> (Mansoor Chishtie)	SPRA033	TMS320C5x
	<i>IS-54 Digital Cellular Modem Implementation on TMS320C5x</i> (Balaji Srinivasan)	SPRA033	TMS320C5x
	<i>Mobitex Modem Implementation Using the TMS320C6x</i> (Etienne Resweber)	SPRA033	TMS320C5x
	<i>Equalization Concepts</i> (David Smalley)	SPRA033	TMS320C5x
	<i>C5x-Based Equalizer Implementation for IS-54</i> (Elliot Hoole)	SPRA033	TMS320C5x

<sup>†</sup> Refer to *DFT/FFT and Convolution Algorithms* by C. S. Burrus and T. W. Parks, published by John Wiley & Sons.

Table 17–1. Application Reports (Continued)

Application	Topic	Location/ Literature No.	Device
Digital Control	<i>Implementation of PID and Deadbeat Controllers With the TMS320 Family</i>	SPRA016	TMS320
	<i>TMS320C31 Embedded Control</i>	SPRU083	TMS320C31
DSP Interface	<i>Interfacing the TMS320 Family to the TLC32040 Family</i>	SPRA016	TMS320
	<i>TMS320C17 and TMS370C0010 Serial Interface</i>	SPRA016	TMS320C17
	<i>Hardware Interfacing to the TMS320C2x</i>	SPRA016	TMS320C2x
	<i>I<sub>CC</sub> Requirements of the TMS320C25</i>	SPRA016	TMS320C25
	<i>An Implementation of a Software UART Using the TMS320C25</i>	SPRA016	TMS320C25
	<i>Interfacing the TMS320C3x to the TLC3204x Analog Interface Chip</i>	SPRA021	TMS320C3x
	<i>TMS320C30 Hardware Applications</i>	SPRA017	TMS320C30
	<i>TMS320C30 – IEEE Floating-Point Format Converter</i>	SPRA017	TMS320C30
	<i>A Low-Cost TMS320C30 Host Interface</i>	SPRA021	TMS320C30
	<i>Engine Knock Detection Using Spectral Analysis Techniques With a TMS320 DSP</i>	SPRA039	TMS320C30
	<i>Interfacing Memory to the TMS320C32 DSP</i>	SPRA040	TMS320C32
	<i>A DSP-Based PCMCIA Card Design (Raj Chirayil)</i>	SPRA033	TMS320C5x
	<i>Interfacing the TMS320C8x into SDRAM</i>	SPRA055	TMS320C8x
	<i>Interfacing the TMS320C8x into DRAM</i>	SPRA056	TMS320C8x

† Refer to *DFT/FFT and Convolution Algorithms* by C. S. Burrus and T. W. Parks, published by John Wiley & Sons.



Table 17–1. Application Reports (Continued)

Application	Topic	Location/ Literature No.	Device
DSP Routines	<i>Digital Filter Design Programs (FIR/IIR)</i>	BBS	TMS320
	<i>Minimizing Quantization Effects Using TMS320 Digital Signal Processor Family</i>	SPRA035	TMS320
	<i>EDN Magazine 1st-Generation (TMS320C1x) Benchmarks</i>	BBS	TMS320C1x
	<i>TMS320C10 FFT Routines</i>	BBS, JW†	TMS320C10
	<i>TMS320C14 Examples (from TMS320C14 User's Guide)</i>	BBS	TMS320C14
	<i>Self Test</i>	SPRA012	TMS320C1x/C2x
	<i>EDN Magazine 2nd-Generation (TMS320C2x) Benchmarks</i>	BBS	TMS320C2x
	<i>TMS320C2x-Based Adaptive Line Enhancer Design</i>	SPRA012	TMS320C2x
	<i>'C25 Complex 256-Point FFT</i>	BBS	TMS320C25
	<i>'C25 Real 256-Point FFT</i>	BBS	TMS320C25
	<i>TMS320C25 Examples (from TMS320C25 User's Guide)</i>	BBS	TMS320C25
	<i>Preliminary Documentation/Source Listing for C26 Boot ROM</i>	BBS, SPRA017	TMS320C26
	<i>An 8x8 Discrete Cosine Transform Implementation on the TMS320C25 or the TMS320C30</i>	SPRA017	TMS320C25/C30
	<i>Implementation of Adaptive Filters With the TMS320C25 or the TMS320C30</i>	BBS	TMS320C25/C30
	<i>EDN Magazine 3rd-Generation (TMS320C3x) Benchmarks</i>	BBS	TMS320C3x
	<i>'C30 Serial Port Example Program</i>	BBS	TMS320C30
	<i>C Callable Functions to Initialize TMS320C30 Cache and Wait State Control</i>	BBS	TMS320C30
	<i>C Callable Matrix Multiply Functions for the TMS320C30</i>	SPRA017	TMS320C30
	<i>A Collection of Functions for the TMS320C30</i>	SPRA017	TMS320C30
	<i>Doublelength Floating-Point Arithmetic on the TMS320C30</i>	BBS	TMS320C30
	<i>Example Programs for Operation of TMS320C30 Serial Ports</i>	BBS	TMS320C30
	<i>Fast (2.42 ms) Radix-2 1024-Point FFT Routine</i>	SPRA017	TMS320C30
	<i>An Implementation of FFT, DCT, and Other Transforms on the TMS320C30</i>	BBS	TMS320C30
	<i>TMS320C30 Echo Cancellation Program</i>	BBS	TMS320C30
	<i>TMS320C30 Examples (from TMS320C30 User's Guide)</i>	BBS	TMS320C30
	<i>TMS320C30 Matrix Multiply Benchmark Report</i>	BBS	TMS320C30
	<i>TMS320C30 Utility Programs</i>	SPRA031	TMS320C30
	<i>A Parallel Approach for Solving Matrix Multiplication on the TMS320C4x DSP</i>	BBS	TMS320C4x

† Refer to *DFT/FFT and Convolution Algorithms* by C. S. Burrus and T. W. Parks, published by John Wiley & Sons.

Table 17–1. Application Reports (Continued)

Application	Topic	Location/ Literature No.	Device
Image/Graphics	<i>A DSP-Based Three-Dimensional Graphics System</i>	SPRA017	TMS320C30
	<i>TMS320C3x DSPs Supercharge 3-D Graphics</i>	SPRA024	TMS320C3x
	<i>DSP-Based Handprinted Character Recognition</i> (Alan Josephson)	SPRA033	TMS320C5x
	<i>TMS320C8x Fundamental Graphic Algorithms</i>	SPRA069	TMS320C8x
Miscellaneous	<i>The TMS320 Family and Book Overview</i>	SPRA012, SPRA016, SPRA017	TMS320
	<i>The TMS320 Family of Digital Signal Processors</i>	SPRA016, SPRA017	TMS320
	<i>Implementation of the Kaish Circuit Lockout System</i> <i>With the TMS320 Family</i>	SPRA022	TMS320
	<i>The Texas Instruments TMS320C25 Digital Signal</i> <i>Microcomputer</i>	SPRA016	TMS320C25
	<i>The TMS320C30 Floating-Point Digital Signal Processor</i>	SPRA017	TMS320C30
	<i>Calculation of TMS320C30 Power Dissipation Software</i> <i>Coding Guidelines for 'C5x Developers</i> (Mansoor Chishtie)	SPRU031, SPRA033	TMS320C30, TMS320C5x
	<i>TMS320C8x Transform 3 Command</i>	SPRA069	TMS320C8x
	<i>TMS320C8x Transform 4 Command</i>	SPRA069	TMS320C8x
	<i>Fill Draw Colored Trapezoid Command</i>	SPRA069	TMS320C8x
	<i>TMS320C8x Draw Colored Line Commands</i>	SPRA069	TMS320C8x
	<i>TMS320C80 PP Integer and Floating-Point Math</i>	SPRA069	TMS320C80
Speech Coding/ Recognition	<i>Firmware-Programmable <math>\mu</math>C Aids Speech Recognition</i>	SPRA012	TMS320
	<i>A TMS320C30-Based LPC Vocoder</i>	SPRA021	TMS320C30
	<i>Calculation of TMS320C5x Power Dissipation Application</i> <i>Report</i>	SPRA030	TMS320C5x
	<i>Theory and Implementation of the Digital Cellular Standard</i> <i>Voice Coder: VSELP on the TMS320C5x</i> (Jason Macres)	SPRA033	TMS320C5x
	<i>Implementation of Speaker-Independent Speech Recognition</i> <i>on TMS320C2x/C5x</i> (Raj Pawate and Peter Robinson)	SPRA033	TMS320C5x
	<i>Automated Dialing of Cellular Telephones Using Speech</i> <i>Recognition</i>	SPRA033	TMS320C5x
	<i>Acoustic Echo Cancellation Algorithms and Implementation</i> <i>on TMS320C8x</i>	SPRA063	TMS320C8x

† Refer to *DFT/FFT and Convolution Algorithms* by C. S. Burrus and T. W. Parks, published by John Wiley & Sons.

Table 17–1. Application Reports (Continued)

Application	Topic	Location/ Literature No.	Device
Telecommunications	<i>General-Purpose Tone Decoding and DTMF Detection</i>	SPRA016	TMS320C17/E17
	<i>Implementation of a CELP Speech Coder for the TMS320C30 Using SPOX</i>	SPRA017	TMS320C30
	<i>Modified Goertzel Algorithm in DTMF Detection</i>	SPRA066	TMS320C8x
Tools	<i>TMS320 Algorithm Debugging Techniques</i>	SPRA016	TMS320
	<i>The TMS320C30 Applications Board Functional Description</i>	SPRA017	TMS320C30
	<i>C-Coding Tips for Application Specific Processors</i>	SPRA021	TMS320C30
	<i>TMS320C30 Evaluation Module Overview</i>	SPRA021	TMS320C30
	<i>How TMS320 Tools Interact with the TMS320C32's Enhanced Memory Interface</i>	SPRA048	TMS320C32

† Refer to *DFT/FFT and Convolution Algorithms* by C. S. Burrus and T. W. Parks, published by John Wiley & Sons.

## 17.4 TMS320 DSP Designer's Notebook Pages

The Designer's Notebook Pages (DNPs) are short application notes written by TI's engineering teams, customers, and TMS320 third parties. These application notes provide helpful tips for designing and programming with the TMS320 DSPs. The DNPs are available to download from the TMS320 BBS at (281) 274-2323, or from the DSP Solutions www site at <http://www.ti.com/dsps>, or from the Internet FTP site at <ftp.ti.com>. Table 17–2 lists the Designer's Notebook topics currently available. Also available is the TMS320 DSP Designer's Notebook, Volume 1 (SPRT125), which contains DNP numbers 1–60.

*Table 17–2. Currently Available Designer's Notebook Pages for TMS320 DSPs*

No.	Topic
1	'C3x Block Repeat
2	Avoiding False Interrupts on the 'C3x
3	Bit-Reversed Addressing Without Data Alignment on the 'C3x
4	Optimizing Control Algorithms on 'C5x
5	TMS320C30 Addressing up to 68 Gigawords
6	'C5x EVM Provides for Audio Processing
7	Circular Buffering in Second Generation DSPs
8	Bit-Reversed Addressing in C on the 'C3x
9	Sharing Header Files in C and Assembly
10	Initializing the Fixed-Point EVM's AIC
11	TMS320C25 Logical Shifts in Parallel With ALU Operations
12	TMS320C40 Boot Loader Selection
13	Reducing System Power Requirements
14	Interfacing the TMS320C31 to A/D and D/A Devices
15	Efficient Coding on the TMS320C5x
16	TMS320C40 DMS Memory Transfer Timing
17	Designing with TMS320C40 Comm Ports: Part 1
18	Creating a Delay Buffer on a TMS320C2x EVM
19	Dual-Access Into Single-Access RAM on a 'C5x Device
20	A Simple Way to Terminate Unused TMS320C40 Comm Ports
21	TMS320C5x Interrupts
22	Fast Logarithms on a Floating-Point Device
23	Switching from Bootloader to MP Mode With the TMS320C31

*Table 17–2. Currently Available Designer's Notebook Pages for TMS320 DSPs (Continued)*

<b>No.</b>	<b>Topic</b>
24	TMS320C5x Interrupt Response Time
25	TMS320C2x/'C5x EVM AIC Initialization and Configuration
26	A Novel Way of Using TMS320C40 Cache
27	Hardware UART for TMS320C3x
28	Using VRAMs and DSPs for System Performance
29	Using the RBIT on the TMS320E25
30	Addressing Peripherals as Data Structures in C
31	Interrupts in C on the TMS320C3x
32	TMS320C40 Emulator Tips
33	Floating-Point C Compiler: Tips and Tricks — Part 1
34	Guidelines for Decoupling Capacitors on DSP Designs
35	TMS320C5x Interrupts and the Pipeline
36	Improved Context Save/Restore Performance and Interrupt Latency for ISRs written in C
37	Serial ROM Boot
38	Mastering the 'C4x DMA
39	Bootload of C Code for the TMS320C5x
40	How to Convert a HEX30 Output File Into a Linkable Assembly File
41	Supporting External DMA Activity to Internal RAM for TMS320C5x Devices With the PZ Package
42	Binary Search Algorithm on the TMS320C5x
43	Random Number Generation on a TMS320C5x
44	Using a TMS320C80 Serial Port as an Asynchronous RS-232 Port
45	Fast TMS320C5x External Memory Interface
46	TMS320C5x Memory Paging (Expanding its Address Reach)
47	TMS320C5x Clock Modes
48	TMS320C5x Wait States
49	Clocking Options on the TMS320C5x
50	TMS320C5x DSK Analog I/O
51	Bootloading a 'C4x Network—Part 1: Direct Connect System
52	Emulator Processor Access Timeout
53	Extending Fixed-Point Math Dynamic Range With Minimum Cycles

Table 17–2. Currently Available Designer's Notebook Pages for TMS320 DSPs (Continued)

No.	Topic
54	Accessing TMS320C5x Memory-Mapped Registers in CC5XREGS.H
55	C Routines for Setting Up the AIC on the TMS320C5x EVM
56	How Can Comb Filters be Used to Synthesize Musical Instruments on a TMS320 DSP?
57	Initializing the TMS320C5x DSK Board
58	Debugging a Full-Duplex UART on the TMS320C3x
59	Designing Macros for the TMS320C5x
60	Accessing States and Control Fields and I/O Ports in the TMS320Cxx HLL Debugger
61	Multipass Linking
62	Linking C Data Objects Separate From the .bss Section
63	Shared Memory Interface With a TMS320C5x DSP
64	Accessing TMS320C54x Memory-Mapped Registers in C—C54XREGS.H
65	Interfacing External Memory to the TMS320C5x DSK
66	Interfacing a TMS320C2x, 'C2xx, or 'C5x DSP to a TLC548 8-Bit A/D Converter
67	Interfacing a TMS320C2x, TMS320C2xx, or TMS320C5x DSP to an 8-Bit Boot EPROM
68	Using the Circular Buffers on the TMS320C5x
69	Viewing TMS320C8x Register Bit Fields and Memory-Mapped Registers in the HLL Debugger
70	Parity Generation on the TMS320C54x
71	$\mu$ -Law Compression on the TMS320C54x
72	Interfacing Two Analog Interface Circuits to One TMS320C5x Serial Port
73	Writing TMS320C8x PP Code Under the Multitasking Executive
74	Reading a 16-Bit Bus With the TMS320C5x Serial Port
75	Interfacing a TMS320C3x DSP to the TLC320AD58C 18-Bit Stereo A/D Converter
76	Interfacing a 20-MSPS TLC5510 Flash A/D Converter to TMS320C2xx and TMS320C5x Fixed-Point DSPs
77	IDLE2 Instruction on a TMS320C51 DSP When Using a Divide-by-One Clock Option

## 17.5 University Textbooks

Numerous TMS320 textbooks have been published to support digital signal processing research and education. These textbooks (listed below according to publisher) are designed to aid in the understanding of DSP applications and implementations using the TMS320 family.

□ **Prentice-Hall**

College Technical and Reference Division  
Upper Saddle River, NJ 07458  
(201) 236-7000  
(800) 223-1360  
(800) 947-7700

■ ***Digital Signal Processing Applications With the TMS320 Family***, volume 1 (K.S. Lin, editor), is a reference guide for developing applications. The guide consists of application reports, published articles, and technical reports covering a wide range of DSP applications. Source code for the application algorithms is given in the text as well as on two floppy disks (included). ISBN #013212-4661, U.S. \$89.00

■ ***Digital Signal Processing Applications With the TMS320 Family***, volume 2 (P. Papamichalis, editor), contains additional TMS320C1x and TMS320C2x applications. Applications reports include DSP interface and algorithm debug techniques, as well as data communications, telecommunications, and digital control applications for the TMS320 family. Source code for application algorithms is given in the text as well as on floppy disks (included). ISBN #013212-9523, U.S. \$69.00

■ ***Digital Signal Processing Applications With the TMS320 Family***, volume 3 (P. Papamichalis, editor), focuses primarily on 'C3x applications, such as implementation of Fast Fourier Transforms (FFT), DCT, and other transforms, and on a wide range of floating-point algorithms. Source code for application algorithms is given in the text as well as on floppy disks (included). ISBN # 013212-9604, U.S. \$78.00

□ **John Wiley & Sons**

Professional Reference and Trade Group  
605 Third Avenue  
New York, NY 10158-0012  
(212) 850-6000

■ ***DFT/FFT and Convolution Algorithms*** (C.S. Burrus and T.W. Parks) completely covers the theory and computation of Discrete Fourier Transforms (DFT). The three main approaches to FFTs (Cooley-Tukey, prime-factor, and Winograd) are also described in detail. TMS320 coding examples are included. ISBN #0471-819328, U.S. \$64.95

- **Digital Filter Design** (T.W. Parks and C. S. Burrus) is a comprehensive guide to digital filter design methodologies, covering basic theory as well as working programs. Properties, design, approximations, and implementation of FIR and IIR filters are discussed in detail. Design examples using TMS320 DSPs are included. ISBN #0471-828963, U.S. \$75.95
- **Theory and Design of Adaptive Filters** (J.R. Treichler, C.R. Johnson, Jr., and M.G. Larimore) introduces the fundamental concepts, design techniques, and application guidelines of adaptive filters. This text discusses the analysis and design of the three basic classes of adaptive filters: FIR, IIR, and adaptive property restorative filters. Several TMS320 design examples are presented. ISBN #0471-832200, U.S. \$108.00
- **Digital Signal Processing With the TMS320C25** (R. Chassaing and D. Horning) describes the architecture and instruction set of the TMS320C25. Theoretical discussion is followed by practical examples supported by projects and applications. A disk containing all the programs used and a filter design package is included. ISBN #0471-510661, U.S. \$74.95
- **Digital Signal Processing With C and the TMS320C30** (Ralph Chassaing) describes the architecture and instruction set of the TMS320C30. Programming examples using both C and TMS320C30 are included throughout the text. A disk of programming examples is included. ISBN #0471-577774, U.S. \$59.95
- **A Simple Approach to Digital Signal Processing** (Craig Marven and Gillian Ewers) takes the reader step-by-step through the most basic signal processing concepts to more complex functions and devices, including sampling, filtering, frequency transforms, data compression, and even DSP design decisions. ISBN #0471-152439, U.S. \$39.95
- **Active Noise Control Systems — Algorithms and DSP Implementations** (Sen M. Kuo) emphasizes the practical aspects of active noise control (ANC) systems using a signal processing and DSP implementation perspective. The principles of adaptive signal processing are combined with experimental results and practical issues including the application of these structures and algorithms using C and assembly programs on the TMS320C25 and TMS320C30. ISBN #0-471-13424-4, U.S. \$79.95



❑ **Computer Science Press**

41 Madison Avenue  
New York, NY 10010  
(212) 349-8263

***Digital Signal Processing*** (Richard Haddad and Thomas Parsons) is a comprehensive guide to digital control theory and the design and implementation of digital control systems. This book is a collection of more than 40 application reports and papers from well-known industry experts. Many reports explore the advantages of implementing control algorithms with digital rather than analog techniques. Specific applications discussed include computer peripherals, motion control/robotics, power electronics, and automotive. ISBN #0710-782065, U.S. \$59.95

❑ **Plenum Publishing**

233 Spring Street  
New York, NY 10013-1578  
(800) 221-9369  
(212) 620-8000  
(212) 807-1047 (Fax)

***Communication System Design Using DSP Algorithms*** (Steven A. Tretter) is a comprehensive set of experiments used to explore digital signal processing and communication systems theoretical concepts by implementing them on actual hardware (TMS320C30) in real time. ISBN # 0-306-45032-1, U.S. \$55.00

## 17.6 Technical Articles Bibliography

This section lists key articles and papers that have been published about the TMS320 DSPs. Readers who are interested should be able to locate these articles/papers at their local public or university library.

For a complete listing of articles and papers, refer to the bibliographies in *Digital Signal Processing Applications With the TMS320 Family*, volume 1, volume 2, and volume 3 (literature numbers SPRA012, SPRA016, and SPRA017, respectively) and in *Digital Control Applications With the TMS320 Family* (SPRA019).

### ☐ cDSP Tools

- “DSP Design Takes Top-Down Approach,” Andy Fritsch and Kim Asal, *EE Times DSP Series Part III*, July 17, 1995.
- “The Growing Spectrum of Custom DSPs,” Gene Frantz and Kun Lin, *EE Times DSP Series, Part II*, April 18, 1994.

### ☐ Control

- “Real-Time Control,” Gregg Bennett, *Appliance Manufacturer*, May 1995.
- “DSPs Advance Low-Cost ‘Green’ Control,” Gregg Bennett, *EE Times DSP Series Part II*, April 17, 1995.
- “A Greener World Through DSP Controllers,” Panos Papamichalis, *DSP & Multimedia Technology*, September 1994.

### ☐ DSP Technology

- “Application Guide with DSP Leading-Edge Technology,” Y. Nishikori, M. Hattori, T. Fukuhara, R. Tanaka, M. Shimoda, I. Kudo, A. Yanagitani, H. Miyaguchi, and others, *Electronics Engineering*, November 1995.
- “Function-Focused Chipsets: Up the DSP Integration Core,” Panos Papamichalis, *DSP & Multimedia Technology*, March/April 1995.
- “On-Chip Multiprocessing Melds DSPs,” Karl Gutttag and Doug Deao, *EE Times DSP Series Part III*, July 18, 1994.

### ☐ DSP Tools/Development Support

- “Easing JTAG Testing of Parallel-Processor Projects,” Tony Coomes, Andy Fritsch, and Reid Tatge, *Asian Electronics Engineer*, Manila, Philippines, November 1995.
- “DSP Design Takes Top-Down Approach,” Andy Fritsch and Kim Asal, *EE Times DSP Series Part III*, July 17, 1995.

- "The Digital Signal Processor Development Environment," Greg Peake, *Embedded System Engineering*, United Kingdom, February 1995.
- "Third-Party Support Drives DSP Development for Uninitiated and Experts Alike," Panos Papamichalis, *DSP & Multimedia Technology*, December 1994/January 1995.

□ **DSP Solutions Applications**

- "Digital Signal Processing Solutions Target Vertical Application Markets," Ron Wages, *ECN*, September 1995.

□ **General-Purpose DSP**

- "Fixed or Floating? A Point Question in DSPs," Jim Larimer and Daniel Chen, *EDN*, August 3, 1995.
- "Toward an Era of Economical DSPs," John Cooper, *EE Times DSP Series Part I*, January 23, 1995.
- "The Wide World of DSPs," Jim Larimer, *Design News*, June 27, 1994.

□ **Graphics/Imaging**

- "High-Tech Copiers To Improve Images and Reduce Paperwork," Karl Gutttag, *Document Management*, July/August 1995.
- "A Single-Chip Multiprocessor DSP for Image Processing—TMS320C80," Dr. Ing. Dung Tu, *Industrie Elektronik*, Germany, March 1995.

□ **Hard Disk Drive**

- "Digital Signal Processors Boost Drive Performance," Tim Adcock, *Data Storage*, September/October 1995.

□ **Military**

- "Beware of BAT: DSPs Add Brilliance to New Weapons Systems," Panos Papamichalis, *DSP & Multimedia Technology*, October 1994.

□ **Multimedia**

- "DSPs Do Best on Multimedia App," Doug Rasor, *Asian Computer World*, October 9–16, 1995.
- "Host-Enabled Multimedia: Brought to You by DSP Solutions," Panos Papamichalis, *DSP & Multimedia Technology*, September/October 1995.
- "Choose DSPs for PC Signal Processing," Panos Papamichalis, *DSP & Multimedia Technology*, January/February 1995.

❑ **Power Dissipation**

- “Telecom Future Driven by Reduced Milliwatts per DSP Function,” Panos Papamichalis, *DSP & Multimedia Technology*, May/June 1995.
- “Approaching the No-Power Barrier,” Jon Bradley and Gene Frantz, *Electronic Design*, January 9, 1995.

❑ **Speech/Voice**

- “Speech Recognition,” P.K. Rajasekaran and Mike McMahan, *Wireless Design & Development*, May 1995.
- “DSPs: Speech Recognition Technology Enables,” Gene Frantz and Gregg Bennett, *I&CS*, May 1995.
- “DSP and Speech Recognition, An Origin of the Species,” Panos Papamichalis, *DSP & Multimedia Technology*, July 1994.

❑ **Telecommunications**

- “GSM: Standard Strategien, und Systemchips,” Edgar Auslander, *Elektronik Praxis*, Germany, October 6, 1995.
- “Developing Nations Take Shine to Wireless,” Russell MacDonald, Kara Schmidt, and Kim Higden, *EE Times*, October 2, 1995.
- “Integration Shrinks Digital Cellular Telephone Designs,” Fred Cohen and Mike McMahan, *Wireless System Design*, November 1994.
- “Telecom Future Driven by Reduced Milliwatts per DSP Function,” Panos Papamichalis, *DSP & Multimedia Technology*, May/June 1995.

## **17.7 TMS320 Newsletter, *Details on Signal Processing***

The TMS320 newsletter, *Details on Signal Processing*, is published quarterly to update TMS320 customers on product information and industry trends. It covers TMS320 DSP solutions, documentation, new third-party hardware and software support, new applications, technical information about TMS320 products, development tool updates, worldwide contacts for support, design workshops, seminars, conferences, and the TMS320 university program.

To be added to the mailing list, in the United States, write to:

**Texas Instruments Incorporated  
Attn: DSPS Newsletter Staff  
P.O. Box 1443, M/S 722  
Houston, Texas 77251-1443**

or call (800) 477-8924, x 3543.

## 17.8 TMS320 DSP Bulletin Board Service

The TMS320 DSP BBS is a telephone-line computer bulletin board that provides access to information about the TMS320 family. The BBS is an excellent means of communicating specification updates for current or new DSP application reports as they become available. It also serves as a means to trade programs with other TMS320 users. In addition, ROM-code algorithms may be submitted by secure electronic transfer via the TMS320 BBS.

The BBS contains TMS320 source code from the more than 2000 pages of application reports written to date. These programs include macro definitions, FFT algorithms, filter programs, ADPCM algorithms, echo cancellation, graphics, control, companding routines, and sine-wave generators.

You can access the BBS with a computer and modem. The modem must be able to communicate at a data rate of either 1200, 2400, 9600, 14,400, or 28,800 bps. A character length of eight bits is required, with one stop bit and no parity. The telephone number of the bulletin board is (281) 274-2323 for U.S.A. or for Europe. There is a 90-minute access limit per day, and it is open 24 hours.

To log onto the BBS, first connect your modem to the telephone line (or if you are using an external modem, connect the modem between the telephone and the computer), and then dial **(281) 274-2323**. Once the call has been established, the BBS responds by displaying a welcome message and asking for your first name, last name, and password (defined when you first access the BBS).

The first time you access the BBS, you have very limited capabilities. You must answer completely the questionnaire that is automatically displayed when your password is defined before the system operator (SYS OP) can upgrade your ID to higher access capabilities. Once the questionnaire has been completed, your ID will be upgraded for nonrestricted access to the BBS, which includes downloading of TMS320 application programs, updates, and device and development tool information. Additional help on any menu can be obtained by using the **?** (question mark) command.

To transfer a file from the BBS to your system, enter the **F** (Files Area) command from the main menu. This allows access to all available BBS files. To get a list and a brief description of the different files available, select the **L** (List file) command. To download a file, choose the **D** command. Select the default protocol by selecting *Your Setting* on the main menu. The BBS supports the most popular protocols, including ASCII, XMODEM, XMODEM-CRC, YMODEM, and ZMODEM. The BBS then asks for a filename. Enter the filename you are interested in. If you use the MS-DOS wildcard characters **\*** and **?** and you are using the YMODEM or ZMODEM protocols, you can download several files

sequentially. Refer to the MS-DOS manual for the details on wildcard characters. With the proper protocol, the BBS waits for you to start the file transfer.

To log off the BBS, enter the **G** (Goodbye) command. The BBS updates the log-in data and waits for the next BBS customer.

See page viii for other worldwide BBSs available.

## **17.9 TMS320 DSP ftp Site**

The TMS320 ftp site is an Internet mirror of the BBS located at [ftp.ti.com](ftp://ftp.ti.com). In this site, you can find most of the information available on the BBS.

To access the ftp site, fpt to [ftp.ti.com](ftp://ftp.ti.com) using anonymous login. The path is `/mirrors/tms320 bbs`. If you have a browser such as Netscape or Internet Explorer, you can type `ftp://ftp.ti.com/mirrors/tms320bbs` to access the ftp site. This site can also be accessed from the DSP solutions www site at <http://www.ti.com/dsps>.



## 17.10 TMS320 DSP Technical Hotline

Texas Instruments maintains a hotline that answers TMS320 technical questions. It responds to specific questions regarding TMS320 device problems, development tools, third-party support, consultants, documentation, upgrades, and new products. The hotline is open Monday from 9:30 a.m. to 6:00 p.m. central standard time, and Tuesday–Friday from 8:30 a.m. to 6:00 p.m. central standard time.

To obtain the most complete information regarding your product, first consult your product documentation then go to the DSP Solutions WWW at

**<http://www.ti.com/dsps>**

This site includes the 320 Hotline On-line™, a service that can help answer your questions.

If your question is not answered there, gather all the information that applies to your problem. With your information, manuals, and products close at hand, you can then call the TMS320 DSP Technical Hotline.

You can submit your information via facsimile machine, or you may submit information via electronic mail.

Telephone, fax numbers, and e-mail addresses are given on page viii.

Questions on pricing, delivery, and availability should be directed to the nearest TI field sales office or to the TI Semiconductor Product Information Center (PIC).

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**Note:**

For worldwide TMS320 DSP Hotline support, see page viii.

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# TMS320 Third Party Support



TI offers a worldwide network of over 250 third parties and consultants who support the TMS320 DSP family.

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18.2 TMS320 Software Cooperative Resource Guide .....	18-28
18.3 Third-Party Contacts at a Glance .....	18-65

## 18.1 TMS320 Third-Party Support Reference Guide

The *Third-Party Support Reference Guide* provides complete listings of the worldwide third-party development products available for TI DSPs. Consultants are also listed in this book. To receive the *TMS320 Third-Party Support Reference Guide*, request literature number SPRU052. This publication is also available on the TI World Wide Web site at

<http://www.ti.com/sc/docs/dsps/develop/3rdparty/contents.htm>

### 18.1.1 TMS320 Family Support Table

Table 18–1. TMS320 Family Device Modeling

Third-Party Company Name	DEC	HP	RS/6000	Sun	Other
Synopsys, Inc. (all generations)	•	•	•	•	•
Zeelan Technology, Inc. ('C4x, 'C5x)	•	•	•	•	•

### 18.1.2 TMS320C1x Support Tables

Table 18–2. Device Programmer

Third-Party Company Name	PC
Advin Systems, Inc.	•

Table 18–3. Motor Control System

Third-Party Company Name	PC	VMEbus	Other
Technology 80 Inc.	•	•	•

Table 18–4. High-Level Language Compiler

Third-Party Company Name	PC	Standalone	VMEbus	Other
DSP Control Group, Inc.	•	•	•	•

Table 18–5. *Algorithm Development Software*

Third-Party Company Name	HP	PC	Sun	Other
Momentum Data Systems, Inc.	•	•	•	•

Table 18–6. *Application Software*

Third-Party Company Name	Filter Design	Visual Programming	Other
Atlanta Signal Processors, Inc.	•		
DSP Control Group, Inc.		•	•
DSP Solutions	•		
Hyperception, Inc.		•	
Momentum Data Systems, Inc.	•		•
Poznan University of Technology	•		•
Signix Corporation	•		
Spectrum Digital, Inc.		•	

Table 18–7. *Development Hardware*

Third-Party Company Name	Multiprocessor Board	Standalone Board
DSP Control Group, Inc.	•	
Synetcom Digital, Inc.		•

Table 18–8. Emulator (In-Circuit)

Third-Party Company Name	HP	PC	Sun
Aptix Corporation	•	•	•
DEEMAX Technology, Inc.		•	
I.S.I.T.		•	
Tasking Software Italia, S.r.l.		•	

Table 18–9. Logic Analyzer

Third-Party Company Name	PC
digital logic instruments GmbH	•

### 18.1.3 TMS320AVxxx Support Table

Table 18–10. Development Hardware

Third-Party Company Name	Data Acquisition Board
Atlanta Signal Processors, Inc.	•

### 18.1.4 TMS320C2x Support Tables

Table 18–11. Device Programmer

Third-Party Company Name	PC
Advin Systems Inc.	•

Table 18–12. High-Level Language Compiler

Third-Party Company Name	PC	Standalone	VMEbus	Other
DSP Control Group, Inc.	•	•	•	•

Table 18–13. Algorithm Development Software

Third-Party Company Name	HP	PC	Sun	Other
Portescap		•		
Momentum Data Systems, Inc.	•	•	•	•
Signallogic, Inc.		•		

Table 18–14. Application Software

Third-Party Company Name	Debugging Tools	Filter Design	Operating System	Visual Programming	Other
Atlanta Signal Processors, Inc.		•			
DSP Control Group, Inc.				•	•
DSP Solutions		•			
Hyperception, Inc.				•	
Momentum Data Systems, Inc.		•			•
MultiDSP Inc.		•			•
Portescap					•
Poznan University of Technology		•			•
Signallogic, Inc.	•	•		•	
Signix Corporation		•			
Spectrum Digital, Inc.				•	
Tasking Software Italia, S.r.l.			•		

Table 18–15. Development Hardware

Third-Party Company Name	Data Acquisition Board	Multiprocessor Board	Plug-In Board/Module	Standalone Board	Other
Applied Signal Technology, Inc.			•		
Atlanta Signal Processors, Inc.			•		
Bridgenorth Signal Processing Inc.			•		
Dalanco Spry			•		
DSP Control Group, Inc.		•			
DEEMAX Technology, Inc.			•		
EPIX, Incorporated			•		
Instrumental Systems Corporation			•		
Loughborough Sound Images pic			•		
Portescap				•	
S.E.E.D.	•		•	•	•
Spectrum Signal Processing					•
Synetcom Digital, Inc.				•	
VisionSmart Inc.		•			

Table 18–16. Emulator (In-Circuit)

Third-Party Company Name	HP	PC	Sun
Aptix Corporation	•	•	•
Beetek, Inc.		•	
DEEMAX Technology, Inc.		•	
I.S.I.T.		•	
Tasking Software Italia, S.r.l.		•	

Table 18–17. Logic Analyzer

Third-Party Company Name	PC
digital logic instruments GmbH	•

Table 18–18. Motor Control System

Third-Party Company Name	PC
Spectrum Digital, Inc.	•
Portescap	•

### 18.1.5 TMS320C2xx Support Tables

Table 18–19. Application Software

Third-Party Company Name	Debugging Tools	Filter Design	Operating System	Visual Programming	Other
Atlanta Signal Processors, Inc.		•			
DSP Solutions		•			
GO DSP Corporation	•		•		
Hyperception, Inc.				•	
Momentum Data Systems, Inc.		•			•
Portescap					•
Signix Corporation		•			
Spectrum Digital, Inc.			•	•	
White Mountain DSP, Inc.	•		•		

Table 18–20. Development Hardware

Third-Party Company Name	Standalone Board
Spectrum Digital, Inc.	•



*Table 18–21. Emulator (In-Circuit)*

Third-Party Company Name	HP	PC	Sun
Aptix Corporation	•	•	•
I.S.I.T.		•	
White Mountain DSP, Inc.		•	•

*Table 18–22. Logic Analyzer*

Third-Party Company Name	PC
digital logic instruments GmbH	•
Macrochip Research, Inc.	•

*Table 18–23. Motor Control System*

Third-Party Company Name	PC
Spectrum Digital, Inc.	•
Portescap	•

### 18.1.6 TMS320C3x Support Tables

Table 18–24. Simulator

Third-Party Company Name	HP	PC	Sun
Alta Group	•	•	•

Table 18–25. High-Level Language Compiler

Third-Party Company Name	HP	PC	Sun	VAX VMS	VMEbus	Other
DSP Control Group, Inc.		•		•	•	•
dSPACE	•	•	•			
GSE Gesellschaft fuer Software Engineering mbH		•	•	•		
Mentor Graphics Corporation	•		•			
Tartan, Inc.		•	•	•		

Table 18–26. Algorithm Development Software

Third-Party Company Name	HP	PC	Sun	UNIX	Other
dSPACE	•	•	•		
Digisonix, Inc.		•			
Eonic Systems, Inc.		•	•		•
MultiDSP, Inc.		•			
Numerix Ltd.		•	•	•	•
Portescap		•			
Signalogic, Inc.		•			
Tartan, Inc.		•	•		

Table 18–27. Application Software

Third-Party Company Name	Debugging Tools	Filter Design	Operating System	Visual Programming	Other
Alta Group of Cadence Design Systems, Inc.	•	•			
Atlanta Signal Processors, Inc.		•			
The Athena Group, Inc.		•			
DSP Control Group, Inc.				•	•
DSP Solutions		•			
dSPACE	•				
Digisonix, Inc.					•
Domain Technologies, Inc.	•				
GO DSP Corporation	•				
Hyperception, Inc.				•	
Momentum Data Systems, Inc.		•			•
MultiDSP Inc.		•			•
Pentek, Inc.	•				
Signalogic, Inc.	•	•		•	
Signix Corporation		•			
Spectrum Digital, Inc.	•			•	•
Tasking Software Italia, S.r.l.			•		

Table 18–28. Development Hardware

Third-Party Company Name	Data Acquisition Board	Multiprocessor Board	PCMCIA Board	Plug-In Board/Module	Stand-alone Board	Other
Analogic Corporation				•		
Applied Signal Technology, Inc.				•		
Ariel Corporation				•		
Atlanta Signal Processors, Inc.				•		
Bridgenorth Signal Processing Inc.				•		
CHEOPS GmbH & Co. KG				•	•	
Communication Automation & Control, Inc.			•			
DGM&S				•		
DSP Control Group, Inc.		•				
DSP Research, Inc.				•		
DSP Tools, Inc.				•	•	
dSPACE	•	•		•	•	•
Dalanco Spry				•		
Dialogic Corporation				•		
Dicon Lab, Inc.				•		
Domain Technologies, Inc.				•		
Electronic Tools GmbH					•	
Innovative Integration, Inc.				•	•	
Instrumental Systems Corporation				•		
Kane Computing				•		
Loughborough Sound Images pic				•		
MEDAV Digitale Signalverarbeitung GmbH				•		
MicroLAB Systems Ltd.	•	•		•		

Table 18–28. Development Hardware (Continued)

Third-Party Company Name	Data Acquisition Board	Multiprocessor Board	PCMCIA Board	Plug-In Board/Module	Stand-alone Board	Other
Nova Engineering, Inc.				•		
Orsys GmbH					•	
Pentek, Inc.	•			•		
Portescap					•	
S.E.E.D.				•		•
Signalogic, Inc.				•		
SimPhonics, Inc.				•		
Sonitech International				•	•	•
Spectrum Signal Processing Inc.				•		•
SYNTECH			•	•		
TEIMA Audiotex				•		
Voice Processing Corporation		•				
Wintriss Engineering Corporation				•		

Table 18–29. Application Hardware

Third-Party Company Name	PC	Standalone
Acroloop Motion Control Systems, Inc.	•	•

Table 18–30. Emulator (In-Circuit)

Third-Party Company Name	HP	PC	Sun	Other
Aptix Corporation	•	•	•	
DSP Research, Inc.		•	•	
Domain Technologies, Inc.		•		
I.S.I.T.		•		
Innovative Integration Inc.		•		
Instrumental Systems Corporation		•		
Kane Computing		•	•	
MicroLAB Systems Ltd.		•		•
Sonitech International		•	•	
White Mountain DSP, Inc.		•	•	

Table 18–31. Logic Analyzer

Third-Party Company Name	PC	Sun	Other
digital logic instruments GmbH	•		
Tektronix Inc.	•	•	•

Table 18–32. Motor Control System

Third-Party Company Name	PC
Spectrum Digital, Inc.	•

### 18.1.7 TMS320C4x Support Tables

Table 18–33. Device Programmer

Third-Party Company Name	PC	Sun	VMEbus	Other
Spectrum Signal Processing	•	•	•	•

Table 18–34. Simulator

Third-Party Company Name	HP	PC	Sun
Alta Group	•	•	•
dSPACE		•	

Table 18–35. High-Level Language Compiler

Third-Party Company Name	HP	PC	Sun	VAX VMS	VMEbus
dSPACE	•	•	•		
GSE Gesellschaft fuer Software Engineering mbH		•	•	•	
Hunt Engineering		•	•		•
Mentor Graphics Corporation	•		•		
Tartan, Inc.		•	•	•	

Table 18–36. Algorithm Development Software

Third-Party Company Name	HP	PC	Sun	UNIX	VMEbus	Other
dSPACE	•	•	•			
Digisonix, Inc.		•				
Eonic Systems, Inc.		•	•			•
Numerix Ltd.		•	•	•		
Signalogic, Inc.		•				
Spectrum Signal Processing, Inc.		•	•		•	
Tartan, Inc.		•	•			

Table 18–37. Application Software

Third-Party Company Name	Debugging Tools	Filter Design	Operating System	Visual Programming	Other
Alta Group	•	•			
Atlanta Signal Processors, Inc.		•			
The Athena Group, Inc.		•			
DSP Solutions		•			
dSPACE	•				
Digisonix, Inc.			•		•
Epstein Associates		•			
GO DSP Corporation	•				
Hyperception, Inc.				•	
INRIA, Rocquencourt				•	
JOVIAN Systems, Inc.				•	
Momentum Data Systems, Inc.		•	•		•
ORINCRON Technologies, Inc.				•	
Pentek, Inc.	•				
Signalogic, Inc.	•	•		•	
Signix Corporation		•			
Spectrum Digital, Inc.	•		•	•	•
Spectrum Signal Processing	•				•
Tasking Software Italia, S.r.l.			•		
White Mountain DSP, Inc.	•				



Table 18–38. Development Hardware

Third-Party Company Name	Data Acquisition Board	Multi-processor Board	Plug-In Board/Module	Stand-alone Board	TIM Module	Other
AB-RoBioMat di Angelo Baronchelli			•			
ADAC Corporation			•			
Applied Signal Technology, Inc.			•			
Ariel Corporation			•		•	
Atlanta Signal Processors, Inc.			•			
Bridgenorth Signal Processing Inc.			•			
CHEOPS GmbH & Co. KG			•			
Coreco	•	•				
DSP Research, Inc.			•			
dSPACE	•	•	•	•		•
DY 4 Systems Inc.			•			
Daimler-Benz Aerospace AG			•			
Electronic Tools GmbH				•		
EPIX, Incorporated			•			
<i>hema</i> Elektronik Fertigungs-und Vertriebs GmbH			•			
High-Tech Services Partners	•		•		•	
Hunt Engineering			•		•	
Image & Signal Processing, Inc.				•		
Innovative Integration Inc.			•		•	
Instrumental Systems Corporation			•		•	
JOVIAN Systems, Inc.	•					
Kane Computing			•		•	
Loughborough Sound Images pic			•		•	

Table 18–38. Development Hardware (Continued)

Third-Party Company Name	Data Acquisition Board	Multi-processor Board	Plug-In Board/Module	Stand-alone Board	TIM Module	Other
MEDAV Digitale Signalverarbeitung GmbH			•			
MicroLAB Systems Ltd.	•	•	•			
Mizar, Inc.		•				
Orsys GmbH				•		
Pacific Cyber/Metrix Inc.		•				
Pentek, Inc.	•		•			
Prodrive B.V.					•	
S.E.E.D.			•			
SHAKTI			•			
Sonitech International	•	•	•			
Spectrum Digital, Inc.				•		
Spectrum Signal Processing Inc.	•	•	•		•	•
Sundance Multiprocessor Technology Ltd.			•		•	
SYNTECH		•				
TEIMA Audiotex			•			
Transtech Parallel Systems Corporation			•		•	
Traquair Data Systems, Inc.		•	•		•	
Wavelink Technology, Inc.			•			
White Mountain DSP, Inc.		•	•			

Table 18–39. Emulator (In-Circuit)

Third-Party Company Name	HP	PC	Sun	Other
Aptix Corporation	•	•	•	
DSP Research, Inc.		•	•	
I.S.I.T.		•		
Innovative Integration Inc.		•		
Instrumental Systems Corporation		•		
Kane Computing		•	•	
MicroLAB Systems Ltd.		•		•
Sonitech International		•	•	
White Mountain DSP, Inc.		•	•	

Table 18–40. Logic Analyzer

Third-Party Company Name	HP	PC	Sun	Other
Corelis Inc.	•			
digital logic instruments GmbH		•		
Tektronix Inc.		•	•	•

Table 18–41. Motor Control System

Third-Party Company Name	PC
Spectrum Digital, Inc.	•

### 18.1.8 TMS320C5x Support Tables

Table 18–42. Assembler/Linker

Third-Party Company Name	HP	PC	Sun	VMEbus	Other
2500AD Software, Inc.	•	•	•	•	•

Table 18–43. Simulator

Third-Party Company Name	HP	PC	Sun	UNIX	Other
Alta Group	•	•	•		
Synopsys, Inc.	•		•	•	•

Table 18–44. Algorithm Development Software

Third-Party Company Name	PC
MultiDSP Inc.	•
Signalogic, Inc.	•

Table 18–45. Application Software

Third-Party Company Name	Filter Design	Debugging Tools	Operating System	Visual Programming	Other
Alta Group	•	•			•
Atlanta Signal Processors, Inc.	•				
The Athena Group, Inc.	•				
D2 Technologies, Inc.					•
DSP Solutions	•				
GO DSP Corporation		•			
Hyperception, Inc.				•	
Momentum Data Systems, Inc.	•				•
MultidSP Inc.	•				•
Poznan University of Technology					•
Signalogic, Inc.	•	•		•	
Signix Corporation	•				
Spectrum Digital, Inc.				•	•
Tasking Software Italia, S.r.l.			•		
White Mountain DSP, Inc.		•			

Table 18–46. Development Hardware

Third-Party Company Name	Data Acquisition Board	Multi-processor Board	Plug-In Board/Module	Stand-alone Board	Other
Applied Signal Technology, Inc.			•		
D2 Technologies, Inc.	•		•		
DSP Control Group, Inc.		•			
DSP Research, Inc.			•		
Dalanco Spry			•		
Electronic Tools GmbH				•	
HotHaus Technologies				•	
Innovative Integration Inc.			•		
Instrumental Systems Corporation			•		
Kane Computing			•		
Loughborough Sound Images pic			•		
MicroLAB Systems Ltd.	•	•	•		
Momentum Data Systems, Inc.			•		
Nova Engineering, Inc.			•		
PHYTEC Meßtechnik GmbH				•	
S.E.E.D.					•
Spectrum Digital, Inc.				•	
Spectrum Signal Processing			•		
Synetcom Digital, Inc.				•	
VisionSmart Inc.			•	•	
White Mountain DSP, Inc.			•		
Xcom Multimedia Communications			•		

Table 18–47. Emulator (In-Circuit)

Third-Party Company Name	HP	PC	Sun	Other
Aptix Corporation	•	•	•	
DSP Research, Inc.		•	•	
DEEMAX Technology, Inc.		•		
Domain Technologies, Inc.		•		
I.S.I.T.		•		
Innovative Integration Inc.		•		
Instrumental Systems Corporation		•		
Kane Computing		•	•	
MicroLAB Systems Ltd.		•		•
White Mountain DSP, Inc.		•	•	

Table 18–48. Logic Analyzer

Third-Party Company Name	PC
digital logic instruments GmbH	•
Macrochip Research, Inc.	•

Table 18–49. Motor Control System

Third-Party Company Name	PC
Spectrum Digital, Inc.	•
Portescap	•

### 18.1.9 TMS320C54x Support Tables

Table 18–50. Simulator

Third-Party Company Name	HP	PC	Sun	UNIX	Other
Alta Group	•	•	•		
Synopsys, Inc.	•		•	•	•

Table 18–51. Application Software

Third-Party Company Name	Debugging Tools	Filter Design	Visual Programming	Other
Alta Group	•	•		
DSP Solutions		•		
GO DSP Corporation	•			
Momentum Data Systems, Inc.		•		•
Signix Corporation		•		
Spectrum Digital, Inc.			•	



Table 18–52. Development Hardware

Third-Party Company Name	Plug-In Board/Module
Applied Signal Technology, Inc.	•
DSP Research, Inc.	•
Xcom Multimedia Communications	•

Table 18–53. Emulator (In-Circuit)

Third-Party Company Name	HP	PC	Sun
Aptix Corporation	•	•	•
I.S.I.T.		•	
White Mountain DSP, Inc.		•	•

Table 18–54. Logic Analyzer

Third-Party Company Name	PC
digital logic instruments GmbH	•

Table 18–55. Motor Control System

Third-Party Company Name	PC
Spectrum Digital, Inc.	•

### 18.1.10 TMS320C8x Support Tables

*Table 18–56. Algorithm Development Software*

Third-Party Company Name	PC	Sun	UNIX	VMEbus	Other
General Imaging Corporation	•	•	•	•	•

*Table 18–57. Application Software*

Third-Party Company Name	Debugging Tools	Filter Design	Visual Programming	Other
Alta Group	•	•		•
DSP Solutions		•		
Epstein Associates		•		
General Imaging Corporation			•	
Signix Corporation		•		
Spectrum Digital, Inc.			•	

Table 18–58. Development Hardware

Third-Party Company Name	Multiprocessor Board	Plug-In Board/Module	Standalone Board
Alacron, Inc.		•	
Ariel Corporation		•	
CHEOPS GmbH & Co.		•	
DY 4 Systems Inc.		•	
ESSE-GI s.r.l.		•	
General Imaging Corporation	•	•	
High-Tech Services Partners		•	
IAT AG/IAT Deutschland GmbH		•	
Instrumental Systems Corporation		•	
Kane Computing		•	
Loughborough Sound Images pic		•	
Mizar, Inc.	•		
Precision Digital Images		•	
Primary Image Ltd.		•	
Spectrum Signal Processing		•	
Video Display Systems s.r.l.			•
VisionSmart Inc.		•	
Wintriss Engineering Corporation			•

Table 18–59. Emulator (In-Circuit)

Third-Party Company Name	HP	PC	Sun
Aptix Corporation	•	•	•
I.S.I.T.		•	
White Mountain DSP, Inc.		•	•

Table 18–60. Logic Analyzer

Third-Party Company Name	PC
digital logic instruments GmbH	•

Table 18–61. Motor Control System

Third-Party Company Name	PC
Spectrum Digital, Inc.	•

## 18.2 TMS320 Software Cooperative Resource Guide

The *TMS320 Software Cooperative Resource Guide* is designed to benefit TI customers and third parties by offering licensable application software. The *TMS320 Software Cooperative Resource Guide* provides quick access to DSP applications for customers who require short development time and fast time to market. The program provides marketing support and exposure to participating third parties.

The *TMS320 Software Cooperative Resource Guide* offers a collection of data sheets for each software algorithm available. Table 18–62 through Table 18–68 list the third-party algorithms currently available, and third-party company names and contact information is presented in Section 18.3. If you would like more information regarding the *TMS320 Software Cooperative Resource Guide* algorithms or how to become a third-party member, please e-mail [swco@micro.ti.com](mailto:swco@micro.ti.com). To receive the *TMS320 Software Cooperative Resource Guide*, request literature number SPRT111. This publication is also on the World Wide Web at

**<http://www.ti.com/sc/docs/dsps/softcoop/index.htm>**

The tables in this section list third parties according to their product for the TMS320C1x-, 'C2x-, 'C2xx-, 'C3x-, 'C4x-, 'C5x-, 'C54x-, and 'C8x-generation devices.

To locate a particular product with these tables, follow this sequence:

Locate the desired TMS320 generation ('C1x, 'C2x, etc.) in the table.

Identify the appropriate tool (for example, application hardware, emulator, etc.) in the title.

Table 18–62. Vocoder Algorithms Available From Third Parties

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>ADPCM</b>							
HLTP-CELP Full-Duplex Speech Coder	CNET	'C3x	6.9	7	3	14.7	Low bit rate with toll quality
High-Quality (HQ) ADPCM Voice Coder	D2	'C5x	32/24	1	25/port	2.4/2.1 <sup>‡</sup>	Equivalent or higher quality than G.726/32 kbps
High-Quality (HQ) ADPCM Voice Coder	D2	'C2xx (est)	32/24	1.2	30/port	2.6/2.3 <sup>‡</sup>	Equivalent or higher quality than G.726/32 kbps
Low-Complexity (LC) ADPCM Voice Coder	D2	'C5x	32	0.3	0.005/port	0.7/0.57 <sup>‡</sup>	Toll quality with extremely low complexity
Low-Complexity (LC) ADPCM Voice Coder	D2	'C2xx (est)	32	0.35	0.005/port	0.8/0.7 <sup>‡</sup>	Toll quality with extremely low complexity
<b>CELP</b>							
LL&H.smc250	L&H	'C25	1-4	7.5/5 <sup>‡</sup>	3/4 <sup>‡</sup>	20	Quality is estimated at 3.0 MOS
L&H.smc350	L&H	'C25	4.8	6/1.75 <sup>‡</sup>	2/1.25 <sup>‡</sup>	14/2.5 <sup>‡</sup>	Real-time compression and decompression
L&H.smc350	L&H	'C30	4.8/7.2/9.6	6.6/5.86 <sup>‡</sup>	1.53/0.99 <sup>‡</sup>	9–12/1.5 <sup>‡</sup>	Real-time compression and decompression

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/Decoder<sup>§</sup> Fixed-point DSP<sup>¶</sup> For both rates

Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>‡</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
L&H.smc350	L&H	'C50	4.8/7.2	4.15/1.3 <sup>‡</sup>	2.07/1.23 <sup>‡</sup>	10.25–14/1–2.62 <sup>‡</sup>	Real-time compression and decompression
Low-Delay CELP Vocoder	DSPSE	'C3x/'C4x	8	15.8	2.7	16.7	4.5-ms algorithmic delay
Low-Memory CELP Vocoder	DSPSE	'C2x/'C5x	4.87/7.46	5.6	1	13.6	Coding on a single fixed-point DSP, no external memory
Multi-Rate CELP Vocoder	DSPSE	'C5x	4.8/7.2/9.6	7.2	2.2	15.3/17.6/18.1	High-quality voice coding on a single fixed-point DSP
Variable-Rate CELP Coding	HotHaus	'C5x	4.2			17.8	
<b>Code-Excited Linear Prediction (CELP)-USFS 1016</b>							
FS1016 Speech Coder	SASL	'C5x	4.8 + 7.2	7.8 <sup>§</sup>	1.05	19	Narrowband speech
USFS 1016 CELP Vocoder	DSPSE	'C3x/'C4x	4.8/7.2/9.6	7.2	5.7	14.5	User-selectable codebook size
USFS 1016 CELP Vocoder	DSPSE	'C5x	4.8/7.2	9.2	5.6	17	Optimal postfiltering, dynamically selectable
<b>FR-GSM Speech Coder</b>							
	SASL	'C2x/'C5x	13	5.87	0.9	4.7	Narrowband speech with ETSI full-rate GSM

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/Decoder<sup>§</sup> Fixed-point DSP<sup>¶</sup> For both rates

Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>G.711 Compander Pulse Code Modulation</b>							
	ASPI	'C3x	64	0.13	0.016	0.48	Elf DSP Application Developer's Toolkit
<b>G.722 SB-ADPCM</b>							
G.722 Audio Coder	ASPI	'C3x	64	2.4	0.32	9.63	Full-duplex real-time on a single 'C3x
G.722 Audio Coder	SASL	'C2x/'C5x	48/56/64	1.1	0.17	9.5	Wideband audio H.32 videoconferencing
ITU G.722 SB-ADPCM Waveform Coder	DSPSE	'C3x/'C4x	48/56/64	1.9	0.5	10.3	User-selectable processing frame size
ITU G.722 SB-ADPCM Waveform Coder	DSPSE	'C5x	48/56/64	3.01	0.5	15.85	Videoconferencing, multimedia, telephony
G.722 With QMF Filter	CNET	'C5x	48/56/64	1	0.2/channel	10/channel	Full-duplex monophonic with 16-kHz sampling
ITU-T G.722 with QMF Filters	CNET	'C54x	48/56/64	6	1/channel	13/FIR	Full-duplex monophonic coder-decoder at 16 kHz

<sup>†</sup> Analysis/synthesis or transmit/receive

<sup>‡</sup> Coder/Decoder

<sup>§</sup> Fixed-point DSP

<sup>¶</sup> For both rates



Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>‡</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
ITU-T Fixed-Point G.722	CNET	'C3x	48/56/64	1.3/0.8 <sup>‡</sup>	1/0.8 <sup>‡</sup>	10.6/10	Half-duplex decoder+coder/ full-duplex at 16 kHz
ITU-T Fixed-Point G.722 with QMF Filter	CNET	'C3x	48/56/64	1.3/0.8 <sup>‡</sup>	1/0.8 <sup>‡</sup>	12.8/12	Half-duplex decoder+coder/ full-duplex at 16 kHz
<b>G.723 H.324 Coder</b>							
ITU-T G.723 Fixed-Point LBC Speech Coder	CNET	'C54x	5.3 & 6.3 <sup>2</sup>	6.5+8.5/ 3+8.5 <sup>‡</sup>	1/0.5	16/1.4 <sup>¶</sup>	Very-low bit rate, same speech quality as G.726
ITU G.723 CELP Vocoder	DSPSE	'C5x	5.3/6.4	19.5	4	28.9/30.28	Implementation on a single 'C5x
InvisiLink™ Telephony Codec	ViaDSP	'C3x	64 to 2.4–16	32	4		High-quality voice using G.723 and G.728
<b>G.726 ADPCM</b>							
G.726 Speech Coder	ASPI	'C3x	24/32/40	1.95	0.72	8.3	Full-duplex real-time on a single 'C3x
G.726 ADPCM	HotHaus	'C5x	32/40	1.5		8	Includes G.721 ADPCM
G.726 Audio Coder	SASL	'C5x	16/24/32/40	2	0.1	15.9	Passes ITU G.726 test vectors at all bit rates

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/Decoder<sup>§</sup> Fixed-point DSP<sup>¶</sup> For both rates

Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words)†	Data Memory (K words)†	Processor Loading (MIPS)†	Notes
G.726 ADPCM 1.00 4-bit format	SEED	'C2x					Real-time half duplex/14-bit linear I/O
ITU G.726 ADPCM Waveform Coder	DSPSE	'C3x/'C4x	16/24/32/40	1.8	8.8	8.5	User-selectable input and output format
ITU G.726 ADPCM Waveform Coder	DSPSE	'C5x	16/24/32/40	2.2	0.25	23	User-selectable input and output format
<b>G.728</b>							
G.728 Audio Coder	SASL	'C5x	16	5.36	1.38	33.5	Passes full ITU G.728 test vectors (fixed point)
G.728 CELP Speech Coder	SYN-TECH	'C3x	16	10	0.37	20	Full duplex
G.728 Low-Delay CELP Speech Coder	ASPI	'C3x	16 (12.8/14.4)				3K words at 40 MHz, 4K words at 50 MHz
ITU-T Fixed-Point LD-CELP G.728	CNET	'C54x	16	8	3.5	33	Full-duplex low delay
ITU-T Floating-Point LD-CELP G.728	CNET	'C3x	16	13	3	20	Full-duplex and toll quality

† Analysis/synthesis or transmit/receive

‡ Coder/Decoder

§ Fixed-point DSP

¶ For both rates

Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
ITU G.728 Low-Delay CELP Vocoder	DSPSE	'C3x/'C4x	12.8/14.4/16	16	2.7	17.5	Videoconferencing, digital telephony, multimedia
ITU G.728 LD-CELP Vocoder	DSPSE	'C5x	16	10.5	3.2	36.9	2.5-ms algorithmic delay
InvisiLink™ Telephony Codec	ViaDSP	'C3x	64 to 2.4–16	32	4		High-quality voice using G.723 and G.728
<b>G.729</b>							
G.729 CS-ACELP Speech Coder	ASPI	'C3x	8				Full-duplex real-time capability on a single 'C3x
G.729 CS-ACELP Voice Coder	D2	'C5x (est)	8	8	0.5/port	24/2 <sup>‡</sup>	Verified with G.729 test vector
G.729 CS-ACELP Voice Coder	D2	'C2xx (est)	8	10	0.5/port	30/2 <sup>‡</sup>	Verified with G.729 test vector
G.729 Audio Coder	SASL	'C5x	8	12.6	3.2	34	Including postfilter
ITU-T New 8-kbps G.729	CNET	'C54x	8	10/5 <sup>‡</sup>	1.2/0.8 <sup>‡</sup>	20/3 <sup>‡</sup>	Full duplex with equivalent G.726 quality

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/Decoder<sup>§</sup> Fixed-point DSP<sup>¶</sup> For both rates

Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words)†	Data Memory (K words)†	Processor Loading (MIPS)†	Notes
<b>LPC Linear Predictive Coding</b>							
FIRESS-LPC	Recosyst	'C3x	9.6	6	3	13.3	Signal-to-distortion ratio >20 dB
OROS-CD16 Speech Coders/Decoders	OROS	'C2x/'C5x	2.4–64	4	2	16 ('C25)	Half- or full-duplex also for G.721/G.722
USFS 1015 LPC10e Vocoder V52	DSPSE	'C3x/'C4x	2.4	3.9	4.9	8.7	Secure/tactical communication, voice storage
USFS 1015 LPC10e Vocoder V52	DSPSE	'C5x	2.4	7.4	5.53	8.7	Full-duplex, real-time LPC10e operation
<b>Mixed Excitation Linear Predictive MELP</b>							
	ASPI	'C3x	1.6–2.4	15.3	5.93	20.5	High quality at very low bit rates, C callable
<b>Residual Excited Linear Predictive (REL P)</b>							
Residual Excited Linear Predictive (REL P) VC	D2	'C5x	14.7 (10.7)	2.9	0.43/0.33‡/ port	3.4/0.87‡	Communication quality features at 10.7 Kbps
Residual Excited Linear Predictive (REL P) VC	D2	'C2xx (est)	14.7 (10.7)	3.2	0.45/0.35‡/ port	3.8/1‡	Communication quality features at 10.7 Kbps

† Analysis/synthesis or transmit/receive

‡ Coder/Decoder

§ Fixed-point DSP

¶ For both rates

Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>Self-Excited Vocoder (SEV)</b>							
Self-Excited Vocoder Speech Compression	ASPI	'C3x	4.8–9.6			15.77	128K word for program and data memory
<b>Subband Coder Speech Compression</b>							
	ASPI	'C1x/'C2x/'C3x/'C5x	9.6–19.2	1.67	0.96	6.4 ('C3x)	Four full-duplex or eight half-duplex on one 'C30
<b>Others</b>							
CVSD 16 kbps	ASPI	'C3x	16	0.49	0.215	1.8/1.72	Continuously-varying-slope delta modulation
VoiceWave Vocoder	DSPSE	'C3x/'C4x	4.8–13.2	5.1	2.21	12.2	Two full-duplex channels per 60-MHz 'C32
Wide-Band Speech Coder at Low Delay (10 ms)	CNET	'C3x	24	3.6/3.4 <sup>‡</sup>	4.6/7.0 <sup>‡</sup>	24/4 <sup>‡</sup>	Similar quality of G.722 at 56 Kbps, 16 kHz
<b>VSELP Digital Cellular</b>							
TIA IS-54 VSELP Vocoder	DSPSE	'C3x/'C4x	7.95	8.3	8.4	15	Digital telephony and voice storage
TIA IS-54 VSELP Vocoder	DSPSE	'C5x	7.95	8.7	1.7	18.6	Fully-optimized 'C5x assembly code

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/Decoder<sup>§</sup> Fixed-point DSP<sup>¶</sup> For both rates

Table 18–62. Vocoder Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>Vector Quantization Voice Coder VQ</b>							
Low-Delay Vector Quantization Voice Coder	D2	'C2xx (est)	16	4.5/2.2 <sup>‡</sup>	0.3/port	13.28/15.77	Toll quality with low delay of under 1.5 ms
Low-Delay Vector Quantization Voice Coder	D2	'C5x (est)	16	4/2 <sup>‡</sup>	0.3/port	10/5 <sup>‡</sup>	Toll quality with low delay of under 1.5 ms
Multi-Rate VQ Voice Coder (MRVQ)	D2	'C2xx (est)	5.2–9.6	6/2 <sup>‡</sup>	0.5/port	8/2.2 <sup>‡</sup>	Figures shown are for 9.6-Kbps data rates
Multi-Rate VQ Voice Coder (MRVQ)	D2	'C5x (est)	5.2–9.6	5–6/1.5–2 <sup>‡</sup>	0.5/port	7.5/2 <sup>‡</sup>	Figures shown are for 9.6-Kbps data rates

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/Decoder<sup>§</sup> Fixed-point DSP<sup>¶</sup> For both rates

Table 18–63. Speech Recognition/Synthesis Algorithms Available From Third Parties

Algorithm	Third Party	Device	Program Memory (K words)	Data Memory (K words)	Processor Loading (MIPS)	Notes
<b>Discrete Speaker-Dependent Recognition</b>						
VProPRL™	VPC	'C3x				21 languages
<b>Continuous Speaker-Independent Recognition</b>						
L&H.asr1000/T Automatic Speech Recognition ASR	L&H	'C2x/'C5x	64	28+16-370/ chan	12	Telephony; U.S. English, French, German, Spanish, Dutch, Italian
L&H.asr1000/T Automatic Speech Recognition ASR	L&H	'C3x	100†	28+16-370/ chan‡	8	Telephony; U.S. English, French, German, Spanish, Dutch, Italian
VProPRL™	VPC	'C3x				21 languages
<b>Continuous Speaker Independent and Language Independent</b>						
L&H.asr1500/M Automatic Speech Recognition ASR	L&H	'C2x/'C3x/'C5x				Sample 8+11 kHz; 7 languages
L&H.asr1500/T Automatic Speech Recognition ASR	L&H	'C2x/'C3x/'C5x				Telephony; 7 languages

† Approximate figures excluding drivers, kernels, DSP OS, etc.

‡ Approximate application-dependent figures

Table 18–63. Speech Recognition/Synthesis Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Program Memory (K words)	Data Memory (K words)	Processor Loading (MIPS)	Notes
<b>Text-to-Speech</b>						
ELOQUENS® 2000 Speech Synthesis	CSELT	'C3x	80	820	2.4	Multichannel; Italian
L&H.tts2000/T	L&H	'C31	110	370–560	4	Telephony; 7 languages
L&H.tts3000/A	L&H	'C25	64	220	5	Sample 10 kHz; 7 languages
L&H.tts3000/C	L&H	'C10	8	100	0.3	Sample 10 kHz; 7 languages
L&H.tts3000/T	L&H	'C3x	110	220–400	5	Telephony; 7 languages
<b>Speaker-Independent Recognition</b>						
AURIS® 1010	CSELT	'C3x	64	256	6.4	Telephony; Italian
AURIS® 2010	CSELT	'C3x	100	512	11.2	Telephony; Italian
FLEXUS® 1000	CSELT	'C3x	100	512	6.4	Telephony; Italian
L&H.asr200/A Automatic Speech Recognition ASR	L&H	'C25/'C5x	7	8+5+4.5/word	10	English

† Approximate figures excluding drivers, kernels, DSP OS, etc.

‡ Approximate application-dependent figures



Table 18–63. Speech Recognition/Synthesis Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Program Memory (K words)	Data Memory (K words)	Processor Loading (MIPS)	Notes
L&H.asr200/A Automatic Speech Recognition ASR	L&H	'C3x	12	16+5+4.5/word	8	English
VProPRL™	VPC	'C3x				21 languages

† Approximate figures excluding drivers, kernels, DSP OS, etc.

‡ Approximate application-dependent figures

Table 18–64. Audio Algorithms Available From Third Parties

Algorithm	Third Party	Device	Sampling Rate (kHz)	Program Memory (K words)	Data Memory (K words)	Processor Loading (MIPS)	Notes
<b>Audio Coders</b>							
4 SB ADPCM, High-Quality and Low-Delay Audio Coder	CNET	'C3x	128/120/112	4.3/4.8	1.4/1.1	24/20§	Half-duplex stereophonic audio codec, low delay
FM Stereo Coder with ITU-R BS.643-1 RDS, ARI, SCA	MB Int.	'C30/'C31	192/176/220/192	2/1.25†	1/0.27†		All standards including German ARI or US SCA
ITU-R BS.450-1 FM Stereo Coder	MB Int.	'C30/'C31	192/176/220/192	2	1		Pilot signal at 19-kHz and 38-kHz carrier modulation
MPEG Audio Decoder	ASPI	'C3x	32/44.1/48			6.6/8.3/9.1	Figures at 0-wait state/ 60 ns and different sample rate
MPEG Audio Decoder	ASPI	'C3x	32/44.1/48			6/8.78/9.45	Figures at 0-wait state/ 74 ns and different sample rate
MPEG Audio Coder	ASPI	'C3x	32/44.1/48			7/9/9	Figures at mono/ 50 ns and different sample rate
MPEG Audio Coder	ASPI	'C3x	32/44.1/48			12/17/18	Figures at stereo/ 50 ns and different sample rate

† First/second processor

‡ DASP Digital Audio Signal Processor

§ For both rates

Table 18–64. Audio Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Sampling Rate (kHz)	Program Memory (K words)	Data Memory (K words)	Processor Loading (MIPS)	Notes
<b>Sample Rate Conversion</b>							
Sample-Rate Conversion	ASPI	'C3x	8–48	3	4		Often used for DAT and CD players
<b>Equalizer</b>							
10 Band Graphic Equalizer	ASPI	'C3x		4	3	9.13	Figures at 35-kHz stereo
EQU-31B/M 1.00	SEED	57002/DASP‡	48				32K-words data + program, filter slope 24 db/oct.
XOVER-4W/M 1.00	SEED	57002/DASP‡	48				32K words data + program
<b>Others</b>							
AM Mono/Stereo Transmitter	MB Int.	'C3x	8000	5	1		Conforms to NRSC standard
Echo and Reverberation	ASPI	'C3x	35	0.665	8.19	16.6	Figures at 35-kHz stereo
ITU-R BS.645-2 Vu Meter	MB Int.	'C2x/'C3x/'C4x/'C5x	32/44.1/48	1.25	16.25	6–10	Input sampling rate mentioned

† First/second processor

‡ DASP Digital Audio Signal Processor

§ For both rates

*Table 18–64. Audio Algorithms Available From Third Parties (Continued)*

Algorithm	Third Party	Device	Sampling Rate (kHz)	Program Memory (K words)	Data Memory (K words)	Processor Loading (MIPS)	Notes
High-Quality Variable-Emphasis Limiter	MB Int.	'C3x	192	1.256			Conforms to ITU-R BS.642-1
WIN-REC 1.00	SEED	57002	5–48				Hard-disk recording of audio data into PC

† First/second processor

‡ DASP Digital Audio Signal Processor

§ For both rates

Table 18–65. Telecommunications Algorithms Available From Third Parties

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>Acoustic Echo Cancellation</b>							
Acoustic Echo Canceller	SASL	'C5x		10	7.6	28	Wideband/narrowband
Acoustic Echo Canceller Hands Free	CNET	'C5x		6	1.5	19	With a FIR (NLMS) of 300 coefficients
Acoustic Echo Canceller Hands Free	CNET	'C54x		6	1 <sup>‡</sup>	13	With a FIR (NLMS) of 300 coefficients
GAO Acoustical Echo Canceller	GAO	'C3x/'C5x/'C54x		0.7–2.5	0.3–2.0	4–30	Full-duplex speakerphone
IDEC™ Acoustic Echo Canceller	DSPSE	'C3x/'C4x		<5	<20	<7.2/10	Figures at 8-kHz/16-kHz operation
IDEC™-II Acoustic Echo Canceller	DSPSE	'C3x/'C4x		<7	<20	<8.4/11	Figures at 8-kHz/16-kHz operation
Low-Complexity Network Echo Canceller	D2	'C2xx		1	0.3	1.7	Meets or exceeds G.165 requirements
Low-Complexity Network Echo Canceller	D2	'C5x		0.8	0.3	1.5	Meets or exceeds G.165 requirements

<sup>†</sup> Analysis/synthesis or transmit/receive

<sup>‡</sup> Coder/decoder

<sup>§</sup> Transmitting/receiving

<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>ADSI (Analog Display Services Interface)</b>							
ADSI	D2	'C17		3.8	0.26	4	
ADSI	D2	'C2xx (est)		3.7	0.277	3.5	
ADSI	D2	'C5x (est)		3.5	0.277	3	
GAO Caller ID and ADSI Software	GAO	'C3x/'C5x/'C54x		0.4/1	0.2/0.4	1/1.5	Function caller ID/ADSI
<b>Call Progress Tone Generation/Detection</b>							
Call Progress Tone Detection	D2	'C2xx (est)		1.6	0.181	1.3	Meets Bellcore precise tone detection
Call Progress Tone Detection	D2	'C3x (est)		1.1	0.130	0.8	Meets Bellcore precise tone detection
Call Progress Tone Detection	D2	'C5x		1.41	0.181	1.1	Meets Bellcore precise tone detection
CPT Detector/Generator	DNA	'C3x		0.635	8.55/24 channel	0.16/0.46 <sup>§</sup>	Processor loading per channel
Dial Pulse or Click Detection	D2	'C5x		1.1	0.2	0.9	

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/decoder<sup>§</sup> Transmitting/receiving<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
FAX/CNG Tone Detection	D2	'C5x		0.9	0.138	1	Detects presence of FAX calling tone (CNG)
FAX/CNG Tone Detection	D2	'C2xx (est)		1	0.140	1.1	Detects presence of FAX calling tone (CNG)
GAO Call Progress Tone Detection	GAO	'C3x/'C5x/'C54x		0.3	0.08	8	Function detector
MF Detector/Generator	DNA	'C3x		0.565	1.03/24 channel	0.14/0.44 <sup>§</sup>	According to ITU-T recommendations Q.153/154
Multifrequency Tone Detection	D2	'C2xx (est)		1.1	0.045	1.4	
Multifrequency Tone Detection	D2	'C3x (est)		0.6	0.04	0.85	
Multifrequency Tone Detection	D2	'C5x (est)		1	0.045	1.2	
R2 Transceiver	DNA	'C3x		0.385	0.585/30 channel	0.12/0.34 <sup>§</sup>	Processor loading per channel
Tone Generation	D2	'C2xx (est)		0.55	0.02	0.35	Meets or exceeds EIA 464 requirements

<sup>†</sup> Analysis/synthesis or transmit/receive

<sup>‡</sup> Coder/decoder

<sup>§</sup> Transmitting/receiving

<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
Tone Generation	D2	'C3x (est)		0.45	0.02	0.3	Meets or exceeds EIA 464 requirements
Tone Generation	D2	'C5x		0.52	0.02	0.3	Meets or exceeds EIA 464 requirements
<b>Caller Identification Delivery (CID)</b>							
Bellcore Caller ID Detector	DSPSE	'C5x		1.3	0.51	5	Bit parser and data pump
Caller Identification Delivery	D2	'C17		0.3	0.023	1.2	Complies with Bellcore SR30/SR3004 test
Caller Identification Delivery	D2	'C2xx (est)		0.45	0.020	1	Complies with Bellcore SR30/SR3004 test
Caller Identification Delivery	D2	'C5x		0.4	0.02	1	Complies with Bellcore SR30/SR3004 test
Caller Identification Delivery on Call Waiting	D2	'C17		1.9	0.203	2	Complies with Bellcore SR30/SR3004 test
Caller Identification Delivery on Call Waiting	D2	'C2xx (est)		2.3	0.2	2	Complies with Bellcore SR30/SR3004 test

† Analysis/synthesis or transmit/receive

‡ Coder/decoder

§ Transmitting/receiving

¶ Slow-down/speed up



Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
Caller Identification Delivery on Call Waiting	D2	'C5x		2.1	0.2	1.7	Complies with Bellcore SR30/ SR3004 test
Caller ID, DTMF, and Call Progress Tone Detectors	ASPI	'C3x					
Caller ID Modem	HotHaus	'C5x	1.2	0.35		1	Compliant with Bellcore TR-NWT-001273
GAO Caller ID and ADSI Software	GAO	'C3x/'C5x/'C54x		0.4/1	0.2/0.4	1/1.5	Function caller ID/ADSI
<b>DTMF Generation/Decoder</b>							
GAO DTMF Detector/Generator/Remover	GAO	'C3x/'C5x/'C54x		0.15/0.08/0.55	0.18/0.03/0.39	0.8/0.4/0.8	Function generator/remover/decoder
DTMF Tx/Rx	SASL	'C5x				0.8/0.87 channel	Transmitter/receiver
Low-Complexity DTMF Digit Detection	D2	'C2xx (est)		1.1	0.04	1.3	Meets or exceeds all Bellcore/EIA464
Low-Complexity DTMF Digit Detection	D2	'C3x (est)		0.7	0.035	0.85	Meets or exceeds all Bellcore/EIA464

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/decoder<sup>§</sup> Transmitting/receiving<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words)†	Data Memory (K words)†	Processor Loading (MIPS)†	Notes
Low-Complexity DTMF Digit Detection	D2	'C5x		0.97	0.04	1.2	Meets or exceeds all Bellcore/EIA464
DTMF Digit Detection and Removal	D2	'C2xx (est)		2.4	0.218	2	Meets or exceeds Bellcore/EIA464 tone detection
DTMF Digit Detection and Removal	D2	'C3x (est)		2.7	0.218	1.5	Meets or exceeds Bellcore/EIA464 tone detection
DTMF Digit Detection and Removal	D2	'C5x		2.4	0.218	1.75	Meets or exceeds Bellcore/EIA464 tone detection
DTMF Detector/Generator	DNA	'C3x		0.514	1.032/24 channel	0.149/0.396 <sup>3</sup>	According to ITU-T recommendations Q.23/24
Telco DTMF Generator/ Detector	DSPSE	'C3x/'C4x		1.4	1.12	0.94	
Telco DTMF Generator/ Detector	DSPSE	'C25/'C5x		0.526	0.049	4.2	Function generate and detect
<b>Group 3 Fax (V.29, T.30, V.21, T.4, V.27ter)</b>							
Data Modem Data Pump for Floating-Point DSPs	Dallas SP	'C3x/'C4x	0.3–2.4	8	2.048	8.3	Implements notes V.22bis, BELL212A/103

† Analysis/synthesis or transmit/receive

‡ Coder/decoder

§ Transmitting/receiving

¶ Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
Fax Modem Data Pump for Fixed-Point DSPs	Dallas SP	'C2x/'C5x	0.3–9.6	7	0.512	5/9 <sup>†</sup>	CCITT notes V.29, V.27ter, V.21 notes implemented
Fax Modem Data Pump for Floating-Point DSPs	Dallas SP	'C3x/'C4x	9.6–0.3	8	1.02	2.5/4.7 <sup>†</sup>	CCITT notes V.29, V.27ter, V.21 notes implemented
GAO ITU Group 3 Fax	GAO	'C3x/'C5x/ 'C54x		3/1.5/1.3/0.8/ 2.4	3/1/0.8/0.6/1.2	11/7.5/6/3.4/ 2.5	Function V.17/V.29/V.27ter/V.21/T.30
Group 3 Fax Modem	SASL	'C5x	0.3–9.6	0.5/2/2.5	0.1/0.4/0.5	3.5/4/4.5	Function V.21/V.27ter/V.29
ITU Group 3 Fax Modem	DSPSE	'C3x/'C4x	0.3–9.6	20.9/23.7/ 30.2	10.1	12	Function V.21/V.27ter/V.29/T.30 (no ECM)
Release 1.00 ITU Group 3 Fax Modem	DSPSE	'C5x	2.4–9.6	18/20	14.7/15.2	13.1/18.6	Half duplex with worst/best figures
Modem Code for Group 3 Fax	ILLICO!	'C3x	64	0.54	8	6.5	
Modem Code for Group 3 Fax	ILLICO!	'C5x/'C25	0.3–9.6	0.66	8	9.5	
<b>Line Echo Canceller</b>							
Audio Line Hybrid Echo Canceller	DSPSE	'C3x/'C4x		1.2	1.4	7.5/1.4	Figures for noise generation and train/cancel

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/decoder<sup>§</sup> Transmitting/receiving<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
Audio Line Hybrid Echo Canceller	DSPSE	'C25/'C5x		0.2	0.076	1.4	
GAO Line Echo Canceller	GAO	'C3x/'C5x/ 'C54x		0.75	0.5	6	Canceller function
Network Echo Canceller	D2	'C5x		4.7	1.6	4.8	Exceeds B.165 and Deutsche Bundespost
QuiteQuiet™ Acoustic Echo Cancellation Software	ASPI	'C31				8/16	20/32K words program/data memory at 8/16 kHz
<b>Others</b>							
Audio Library	DSPSE	'C3x/'C4x		300/350/750	50/75/125	0.15/0.04/0.11	Voice-storage-type application, linear PCM
FAX Relay Control Software	ILLICO!	'C5x	2.4-14.4	12	1.76	12/channel	Support for rates up to 14.4 KBPS (V.17/V.33)
GAO Automatic Gain Control	GAO	'C3x/'C5x/ 'C54x		0.5	0.1	0.2	Function AGC

<sup>†</sup> Analysis/synthesis or transmit/receive

<sup>‡</sup> Coder/decoder

<sup>§</sup> Transmitting/receiving

<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>PSTN and POTS Phone Driver</b>							
HausWare	HotHaus	'C5x		6	0.1	0.1	Drivers include PSTN line, POTS/speakerphone
PSTN Driver	HotHaus	'C5x					Capabilities to reduce MIPS and ROM usage
POTS Phone Driver	HotHaus	'C5x					ROM size reduced when used with PSTN driver
<b>Speakerphone</b>							
Gain Variation for Hands-Free Situation	CNET	'C5x		0.8	0.1/port	0.7	8-kHz or 16-kHz sampling rate
Gain Variation for Hands-Free Situation	CNET	'C54x		0.8	0.1	0.7	8-kHz or 16-kHz sampling rate
Full-Duplex Speakerphone Algorithm	SigWorks	'C3x/'C4x		7	9 for 256 ms	12.5/14.5	Ideal for the 'C32 memory configuration
Full-Duplex Speakerphone	HotHaus	'C5x		1	1	15	Echo canceller up to 25 DB and echo path 64 ms

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/decoder<sup>§</sup> Transmitting/receiving<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>TDD</b>							
Telecommunications Device for the Deaf Modem	HotHaus	'C5x		1		1	Requires 8-kHz sampling rate
<b>Time Scaling</b>							
GAO Playback Speed Modification	GAO	'C3x/'C5x/'C54x		1.2	0.35	2.8	PSM function
Speech Time Scaler	DSPSE	'C3x/'C4x		1.4	1.3	2.0 to 8.6	Figures for time scaler
Time Scaling	D2	'C5x		0.6	1.3/port	3.4/1.7 <sup>¶</sup>	Speed-up or slow-down rate changeable
Time Scaling	D2	'C2xx (est)		0.7	1.5/port	3.7/1.9 <sup>¶</sup>	Speed-up or slow-down rate changeable
Time Scale Modification	ASPI	'C3x		36	6	16.6	50–200% pitch or speed changes at 8 kHz

<sup>†</sup> Analysis/synthesis or transmit/receive

<sup>‡</sup> Coder/decoder

<sup>§</sup> Transmitting/receiving

<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>Universal Tone Detection</b>							
Telco Call Progress Generator/ Detector	DSPSE	'C25/'C5x		0.5	0.045	2.2	Function detector
Universal Tone Detection	D2	'C2xx (est)		2.6	0.16	1.8	Detects and translates all US SIT
Universal Tone Detection	D2	'C3x (est)		2.2	0.16	1.4	Detects and translates all US SIT
Universal Tone Detection	D2	'C5x		2.4	0.16	1.75	Detects and translates all US SIT
<b>V.21, V.22, V.23, V.27, V.29</b>							
Centrex Modem	HotHaus	'C5x	1	1		0.5	Compliant with NT NIS 106-1
GAO Modem Library	GAO	'C3x/'C5x/ 'C54x	0.3–28.8	0.7–1.8	0.7–1.0	3.5–6.0	ITU V.21/V.22/V.22bis/ V.32/V.32bis/V.34/Bell
ITU V.22bis Modem	DSPSE	'C3x/'C4x	1.2–2.4	13.1	4.5	5	Full-duplex operation compatible V.22bis/V.22

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/decoder<sup>§</sup> Transmitting/receiving<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
Modem Code for V.22bis	ILLICO!	'C5x/'C25	1.2–2.4	0.38	6	7.5	Data RAM per full-duplex channel
V.21 Modem	SASL	'C5x	0.3	0.5	0.1	3.5	Function V.21 transmitter + receiver
V.22/V.22bis Modem	SASL	'C5x	0.6/1.2/2.4	2.7	0.3	4	Function V.22/V.22bis transmitter + receiver
V.22bis Data Modem	HotHaus	'C5x	2.4	5		4.5	Fallback support to V.22
V.23 Modem	SASL	'C5x	0.6/1.2	0.6	0.12	4.5	Function V.23 transmitter + receiver
V.27ter Fax Modem	HotHaus	'C5x	4.8	5		4	Fallback support to 2400 bps
V.29 Fax Modem	HotHaus	'C5x	9.6	7		3/8§	Fallback support to 4800 bps

<sup>†</sup> Analysis/synthesis or transmit/receive

<sup>‡</sup> Coder/decoder

<sup>§</sup> Transmitting/receiving

<sup>¶</sup> Slow-down/speed up



Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>V.32bis Modem</b>							
GAO Modem Library	GAO	'C3x/'C5x/'C54x	0.3–28.8	0.7–1.8	0.7–1.0	3.5–6.0	
ITU V.32bis Modem	DSPSE	'C3x/'C4x	4.8–14.4	21	11.2	18	Full-duplex operation compatible V.32bis/V.32
V.32/V.32bis Modem	SASL	'C25	4.8/7.2/12/14.4	8	6	9.5	Function V.32/V.32bis transmitter + receiver
V.32/V.32bis Modem	SASL	'C52	4.8/7.2/12/14.4	8	6	14.5	Function V.32/V.32bis transmitter + receiver
V.32bis Data Modem	HotHaus	'C5x	14.4	8		9.5	Fallback support to V.32 (9600 bps)
<b>V Series Modem Interface</b>							
	DSPSE	'C3x/'C4x		4	0.5	1.8	

<sup>†</sup> Analysis/synthesis or transmit/receive<sup>‡</sup> Coder/decoder<sup>§</sup> Transmitting/receiving<sup>¶</sup> Slow-down/speed up

Table 18–65. Telecommunications Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Data Rate (Kbps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>Voice Activity Detection and AGC</b>							
Voice Activity Detection and AGC	D2	'C2xx (est)		1/0.5	0.144/0.008	0.35/0.15	Figures shows speech detect/AGC
Voice Activity Detection and AGC	D2	'C3x (est)		0.7/0.3	0.12/0.008	0.3/0.1	Figures shows speech detect/AGC
Voice Activity Detection and AGC	D2	'C5x		0.9/0.4	0.144/0.008	0.3/0.125	Figures shows speech detect/AGC
μ-law/A-law Detector	DSPSE	'C3x/'C4x	48/56/64	0.4	0.4	0.48	

<sup>†</sup> Analysis/synthesis or transmit/receive

<sup>‡</sup> Coder/decoder

<sup>§</sup> Transmitting/receiving

<sup>¶</sup> Slow-down/speed up

Table 18–66. Image Algorithms Available From Third Parties

Algorithm	Third Party	Device	Frame Rate (fps)	Image Size (fps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>JPEG</b>								
JPEG (8-R8)	SYN-TECH	'C3x/'C4x		256 x 256				256 grayscales and 4K/6K words for encoder/decoder
JPEG Library	MultiDSP	'C3x		256 x 240	2.5/6.5	0.5	9/12	Figures for RGB encoder/decoder
JPEG Still Image Compression	DSPSE	'C3x/'C4x		256 x 240	9.3	2.5	26.2/21.5†	Figures at full-duplex 24-bit RGB
<b>Videoconferencing</b>								
iat320library	IAT	'C80	< 10		300	2000		Full ITU-H.320 compatible
<b>Video Coding</b>								
Video Coding	SASL	'C5x	10	144 x 176	10.54	47.55	83	Decoder complies with ITU H.261
Video Coding	SASL	'C5x	15	128 x 96	10.41	25.795	62	Decoder complies with ITU H.261

† Encoder/decoder

Table 18–66. Image Algorithms Available From Third Parties (Continued)

Algorithm	Third Party	Device	Frame Rate (fps)	Image Size (fps)	Program Memory (K words) <sup>†</sup>	Data Memory (K words) <sup>†</sup>	Processor Loading (MIPS) <sup>†</sup>	Notes
<b>Video Modulation</b>								
Analog TV Vestigial Side Band Modulator	MB Int.	'C80						Conforms to ITU-R BT.470-3

<sup>†</sup> Encoder/decoder

Table 18–67. Operating Systems Algorithms Available From Third Parties

Name	Third Party	Device	Maximum Memory (K words)	Minimum Memory (K words)	Host OS	Language	Notes
Advansis/RT40	Advansis	'C4x			PC, Sun	C	Simple and easy-to-use 'C4x-optimized real-time kernel
Helios® 'C40	Perihelion	'C40, TIM-40	1000-4000	16	PC, Sun	C, C++, Assembly	† RTOS for scalable parallel processing (SPP)
Nucleus Real-Time Software	Accelerated	'C25/'C30/'C40/'C50	18	4	PC, Unix	C	† RTOS for embedded system development
OSE Auric RTOS1	ENEA	'C50	2.0	1.3	PC, Sun		† RTOS for embedded system development
Precise/MQX	Precise	'C3x/'C4x	8	2	PC, Sun	C, C++	† RTOS for single embedded system development
Precise/MQX+m	Precise	'C3x/'C4x	8.2	2.2	PC, Sun	C, C++	† RTOS + comm port connection, VMEbus™ chips, FIFOs
SPOX®-DEBUG	Spectron	'C3x/'C4x/'C5x/'C8x			PC, Sun	C	Simplify development and debugging
SPOX-KNL	Spectron	'C3x/'C4x/'C5x/'C8x		1.5	PC, Sun	C	Deterministic real-time multitasking kernel
SPOX-LINK	Spectron	'C3x/'C4x/'C5x			PC	C, C++	PC/DSP communication interface

† RTOS Real Time Operating system

Table 18–67. Operating Systems Algorithms Available From Third Parties (Continued)

Name	Third Party	Device	Maximum Memory (K words)	Minimum Memory (K words)	Host OS	Language	Notes
SPOX-MP	Spectron	'C4x			PC, Sun	C	Single-processor programming model
Unison™ System	Multipro	'C3x/'C4x		200	PC, Sun	C	Heterogeneous multiprocessing OS
Unison/Embedded	Multipro	'C3x/'C4x/'C5x	200	12	PC, Sun	C	Embedded real-time operating system
Virtuoso® Nano /SP and /VSP	Eonic	'C3x/'C4x		0.2	PC, Sun	C, Assembly	Very small, superfast interruptible multitasking kernel
Virtuoso RTOS Board Porting Kit	Eonic	'C3x/'C4x/'C5x			PC, Sun	C, Assembly	Documented source code to port OS to specific board
Virtuoso's Multi-Threaded Host Server	Eonic	'C3x/'C4x			PC, Sun	C, Assembly	Provides tight integration between host and DSP target
Virtuoso Classico /VSP	Eonic	'C5x		4.5	PC, Sun	C, Assembly	VSP programming model with distributed semantics
Virtuoso Classico /VSP Technology License	Eonic	'C4x		4.5	PC, Sun	C, Assembly	Complete, comprehensive documentation at kernel level
Virtuoso Micro /SP and /MP	Eonic	'C3x/'C4x/'C5x		3.5	PC, Sun	C, Assembly	Fast, preemptive multitasking kernel
Virtuoso Synchro / VSP	Eonic	'C4x/'C80			PC, Sun	C, Assembly	Rapid prototyping and application dev. environment

† RTOS Real Time Operating system

Table 18–67. Operating Systems Algorithms Available From Third Parties (Continued)

Name	Third Party	Device	Maximum Memory (K words)	Minimum Memory (K words)	Host OS	Language	Notes
Virtuoso Nano RTOS	HSP	'C3x/'C4x			PC, Sun	C, Assembly	Very small, superfast interruptible multitasking kernel
Virtuoso Synchro	HSP	'C4x			PC, Sun	C, ASM, VHDL	Synchronous multirate, multi-processor system
Virtuoso Tools	HSP	'C3x/'C4x			PC, Sun		Multitool and multilevel
Virtuoso Classico RTOS	HSP	'C3x/'C4x		6.5	PC, Sun	C, Assembly	RTOS with integrated microkernel and nanokernel
Virtuoso Micro RTOS	HSP	'C4x		4.5	PC, Sun	C, Assembly	Code size in a single-processor implementation

† RTOS Real Time Operating system

Table 18–68. Run-Time Support Library Algorithms Available From Third Parties

Name	Third Party	Device	Host OS	Language	Notes
<b>DSP</b>					
Adaptive Filter Algorithms	MultiDSP	'C3x/'C4x			21 adaptive-filter algorithms
DSP/Veclib	Sinectonanalysis	'C3x/'C4x	8†	C, C++, ADA, Assembler	Hand coded for maximum performance, easy-to-use DSP functions
Optimized DSP Library	Wideband	'C3x/'C4x		C	250 assembly, C-callable, vector, scalar math, and DSP routines
<b>Mathematical</b>					
C_BLAS 123	Sinectonanalysis	'C3x/'C4x	8†	C, C++, ADA, Assembler	Matrix algorithms specially optimized for efficient memory access
C_EISPACK	Sinectonanalysis	'C3x/'C4x	8†	C, C++, ADA, Assembler	Eigen problem run-time support libraries
SPOX®-MATH	Spectron	'C3x/'C4x	PC, Sun 4	C, Assembly	Signal processing and mathematical functions for complete development
STD/Mathlib	Sinectonanalysis	'C3x/'C4x	8†	C, C++, ADA, Assembler	Optimized run-time library of 33 mathematical functions
Unison™ System	Multipro	'C3x/'C4x	PC, Sun	C	Heterogeneous multiprocessing OS

† PC, Sun, HP, DEC, RS6000, Mac, VAX, PowerPC, others

‡ PC, NEC PC, SPARC, VMEbus, VxWorks



Table 18–68. Run-Time Support Library Algorithms Available From Third Parties (Continued)

Name	Third Party	Device	Host OS	Language	Notes
Virtuoso® Modulo	Eonic	'C30/'C40	PC/Sun	C, Assembly	Assembly-optimized DSP function library especially designed for floating-point DSPs
Virtuoso Modulo Set of Libraries	HSP	'C3x/'C4x	PC/Sun	C, Assembly	Optimized DSP and mathematical library (I/O, development, C_BLAS, imaging)
<b>Multiprocessing</b>					
3L Parallel C	3L	'C4x	6†	C	Parallel-programming system for multiprocessor DSP
<b>Networking</b>					
Precise Embedded I/O Components	Precise	'C3x/'C4x		C, C++	Library of TCP/IP, Bootp, RPC, NFS, LAPB, SDLC, HDLC, MIL-STD1553, MS-DOS 3.1
<b>Image Processing</b>					
EYELIB	Sinectonalysis	'C30/'C40	8†	C, C++, ADA, Assembler	More than 400 hand-coded routines for image processing
University of Washington Image Comp.	UWICL	'C80/'C82			94 routines (convolution, morphology, wavelets, FFT, rotation, wrapping)

† PC, Sun, HP, DEC, RS6000, Mac, VAX, PowerPC, others

‡ PC, NEC PC, SPARC, VMEbus, VxWorks

### 18.3 Third-Party Contacts at a Glance

Table 18–69 through Table 18–71 provide the name, country, contact telephone number, and e-mail address for each of the referenced third parties.

*Table 18–69. TMS320 Third-Party Support Reference Guide Contacts*

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
2500AD Software, Inc.	Buena Vista, CO	(719) 395–8683	s2500ad@rmii.com
AB-RoBioMat di Angelo Baronchelli & Dott. Gábor Gulyás	Orzinuovi (BS), Italy	+30–943301/ +30–941264	gabor@galactica.it
Acroloop Motion Control Systems, Inc.	Chanhassen, MN	(612) 474–4500	
ADAC Corporation	Woburn, MA	(617) 935–3200	info@adac.com
Advin Systems Inc.	Sunnyvale, CA	(800) 627–2456, (408) 243–7000	ADVINSales@AOL.com
Alacron, Inc.	Nashua, NH	(603) 891–2750	sales@alacron.com
Alta Group of Cadence Design Systems, Inc.	Sunnyvale CA	(408) 733–1595	Fax: (408) 523–4601
Analogic Corporation	Peabody, MA	(508) 977–3000, x3521	tshugart@analogic.com
Applied Signal Technology, Inc.	Sunnyvale, CA	(800) 374–3560 (408) 522–3560	customer@appsig.com
Aptix Corporation	San Jose, CA	(408) 428–6200	sales@aptix.com
Ariel Corporation	Cranbury, NJ	(609) 860–2900	ariel@ariel.com
Atlanta Signal Processors, Inc.	Atlanta, GA	(404) 892–7265	info@aspi.com
The Athena Group, Inc.	Gainesville, FL	(352) 371–2567 (800) 741–7440	support@athena-group.com
Beetek, Inc.	Shin-Chu, 300, R.O.C.	+886–3–772772	beetek@pc35.hinet.net
Bridgenorth Signal Processing Inc.	Blaine, WA	(604) 538–0003	info@bridgenorth.com
CHEOPS GmbH & Co. KG	Schongau, Germany	+49 8861 7902	100541.3370@compuserve.com
Communication Automation & Control, Inc.	Allentown, PA	(800) 367–6735 (610) 776–6669	cac@silos.com

Table 18–69. TMS320 Third-Party Support Reference Guide Contacts (Continued)

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
Coreco Inc.	St. Laurent, Quebec, Canada	(514) 333–1301	info@coreco.com
D2 Technologies, Inc.	Santa Barbara, CA	(805) 564–3424	sales@d2tech.com
DGM&S	Mt. Laurel, NJ	(609) 866–1212	info@dgms.com
DSP Control Group, Inc.	Minneapolis, MN	(612) 831–9556	Fax: (612) 831–4697
DSP Research, Inc.	Sunnyvale, CA	(408) 773–1042	info@dspr.com
DSP Solutions	Oceanside, CA	(619) 941–3189	Fax: (619) 941–8912
DSP Tools, Inc.	Potomac, MD	(301) 424–5808	davejervis@aol.com
dSPACE	Paderborn, Germany Southfield, MI	+ 49 (0) 5251–1638–0 (810) 354–1694	info@dspace.de 75371,36@compuserve.com
DY 4 Systems Inc.	Nepean, Ontario, Canada	(613) 596 9911	sales@dy4.com
Daimler-Benz Aerospace AG	Munich, Germany	+(089) 607 27689	Fax: +(089) 607 28184
Dalanco Spry	Rochester, NY	(716) 473–3610	dalanco@vivanet.com
DEEMAX Technology, Inc.	Hsinchu, Taiwan, R.O.C.	+886–35–232548	deemax@shts.seed.net.tw
Dialogic Corporation	Parsippany, NJ	(800) 755–4444/ (201) 993–3030	sales@dialogic.com
Dicon Lab, Inc	Gainesville, FL	(904) 372–6160	diconlab@aol.com
Digisonix, Inc	Middleton, WI	(608) 836–3999	Fax: (608) 836–5583
dli digital logic instruments GmbH	Dietzenbach, Germany	+ 49 6074/4002–0	Fax: (+ 49) 6074/4002–24
Domain Technologies, Inc.	Plano, TX	(972) 985–7593	info@domaintec.com
Electronic Tools GmbH	Ratingen, Germany	+49 2102 8801–0	help@etools.de
Eonic Systems, Inc.	Linden, Belgium Silver Spring, MD	+32 16 62 15 85 (301) 572–5000	info@eonic.com
EPIX, Incorporated	Buffalo Grove, IL	(847) 465–1818	epix@epixinc.com

Table 18–69. TMS320 Third-Party Support Reference Guide Contacts (Continued)

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
Epstein Associates	Wilmette, IL	(847) 853–9292; (630) 698–9292	Fax: (847) 853–9293
ESSE-GI s.r.l.	Milan, Italy	+39 2 66017241	Fax: +39 2 6185492
GSE Gesellschaft fuer Software Engineering mbH	München, Germany	+49 89 140 09–265	elk@gse.de
General Imaging Corporation	Billerica, MA	(508) 262–2262	pcholakis@gicorp.com
GO DSP Corporation	Toronto, Ontario, Canada	(416) 599–6868	go-dsp.com
hema Elektronik Fertigungs und Vertriebs GmbH	Aalen, Germany	+7361/9495–0	info@hema.de
HotHaus Technologies	Delta BC Canada	(604) 946–0060	info@hothaus. wimsey.com
High-Tech Services Partners	Guyancourt, France	+33 –1–30 57 31 13	Fax: +33–1–30 43 51 17
Hunt Engineering	Somerset, UK	(+44) (0)1278 760188	sales@hunteng.demon. co.uk
Hyperception, Inc.	Dallas, TX	(214) 343–8525	info@hyperception.com
IAT AG IAT Deutschland GmbH	Vogelsang-Turgi, Switzerland Bremen, Germany	+41 56 223 50 22 +49 421 20 21–0	fmueller@iat.ch A.Fuetterer@ iat-gmbh.de
I.S.I.T.	L'isle Jourdain, France	(+33) 62 07 29 54	100627,2421@ compuserve.com
Image & Signal Processing, Inc.	Anaheim, CA	(714) 970–0700	isp@cerfnet.com
Innovative Integration Inc.	Westlake Village, CA	(818) 865–6150	techsprt@innovative- dsp.com
INRIA, Rocquencourt	Le Chesnay Cedex, France	+33–1–39–63–52–60	yves.sorel@inria.fr
Instrumental Systems Corporation	Moscow, Russia	+7 (095) 274–9118	insys@instrum.msk.su
JOVIAN Systems, Inc.	Woburn, MA	(617) 937–6300	info@jovian.com

Table 18–69. TMS320 Third-Party Support Reference Guide Contacts (Continued)

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
Kane Computing	Cheshire, UK	+44 (0)1606 351006	100417.256@compuserve.com
Loughborough Sound Images plc	Leicestershire, UK	+44 (0)1509 634300	sales@lsi-dsp-co.uk
Macrochip Research, Inc.	Plano, TX	(972) 578 5635	mkt@macrochip.com
MEDAV Digitale Signalverarbeitung GmbH	Uttenreuth, Germany	+49–9131/583–0	Fax: +49–9131/583–11
Mentor Graphics Corporation	Wilsonville, OR	(800) 547–3000	www: <a href="http://www.mentorg.com">http://www.mentorg.com</a>
MicroLAB Systems Ltd.	Moscow, Russia	+7–(095)–485–6332, +7–(095)–488–8744	mlabsys@sovam.com
Mizar, Inc.	Carrollton, TX	(972) 277–4600, (800) 635–0800	info@mizarinc.com
	Bristol, UK	+44 (0) 1454 614584	Fax: +44 (0) 1454 617731
Momentum Data Systems, Inc.	Costa Mesa, CA	(714) 557–6884	dsp@mds.com
MultIDSP Inc.	Cypress, CA	(714) 527–8086	multidsp@aol.com
Nova Engineering, Inc.	Cincinnati, OH	(513) 860–3456, (800) 341–NOVA	sales@novaengr.com
Numerix Ltd.	Leics, UK	+44 (0)1509 413195	johned@cix.compulink.co.uk
ORINCON Technologies, Inc.	San Diego, CA	(619) 455–5025, (800) 4–RIPPEN	rippen@orincon.com
Orsys GmbH	Markdorf, Germany	+49 (0) 7544 73962	Fax: +49 (0) 7544 73952
Pacific Cyber/Metrix Inc. (PC/M Inc.)	Dublin, CA	(510) 829–8700	pcm@ix.netcom.com
Pentek, Inc.	Norwood, NJ	(201) 767–7100	info@pentek.com
PHYTEC Meßtechnik GmbH	Mainz, Germany	+06131–95883–0	info@phytec.de
Portescap	La Chaux-de-Fonds, Switzerland Bucharest, Romania	+41 39 256.111	Portescap @ ping.ch
		Tel/Fax: +40 1 77 8 66 66	

Table 18–69. TMS320 Third-Party Support Reference Guide Contacts (Continued)

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
Poznan University of Technology Institute of Electronics and Telecommunication	Poznan, Poland	+ 48 61 782 745	dabrow@et.put.poznan.pl
Precision Digital Images	Redmond, WA	(800) 678–6505, (206) 882–0218	info@precisionimages.com
Primary Image Ltd.	Surrey, UK	+44 (0) 181 339 9669	contact@pimage.demon.co.uk
Prodrive B.V.	Eindhoven, The Netherlands	+31 40 2461268	Fax: +31 40 2462362
S.E.E.D.	Massa, Italy	(+39) 585 792990	mc4453@mclink.it
SHAKTI	Marseille, France	+(33)–91–90–04–39	Fax: +(33)–91–91–43–34
Siemens AG Österreich	Vienna, Austria	+43 1 1707 37610	Stefan.Rohringer@siemens.at
Signalogic, Inc.	Dallas, TX	(214) 343–0069	dspinfo@signalogic.com
Signix Corporation	Wayland, MA	(508) 358–5955	71662.337@compuserve.com
SimPhonics, Inc.	Tampa, FL	(813) 623–9917	info@simphonics.com
Sonitech International	Wellesley, MA	(617) 235–6824	infoti3@sonitech.com
Spectrum Digital, Inc.	Houston, TX	(281) 561–6952	specdig@ix.netcom.com
Spectrum Signal Processing Inc.	Burnaby, B.C., Canada	(604) 421–5422	Fax: (604) 421–1764
Sundance Multiprocessor Technology Ltd.	Bucks, UK	+44 (0)1494 431203	sales@sundance.com
Synetcom Digital, Inc.	Redondo Beach, CA	(310) 379–2000	73122,1112@compuserve.com
Synopsys, Inc	Mountain View, CA	1–800–34MODEL COSSAP: 1–800–388–9125	modelinfo@synopsys.com designinfo@synopsys.com
SYNTECH	Valbonne, France	+(33) 93 65 28 66	syntech@slnet.mc
Tasking Software Italia, S.r.l.	Milano, Italy	+39 (2) 6698 2207	sales_it@tasking.nl

*Table 18–69. TMS320 Third-Party Support Reference Guide Contacts (Continued)*

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
Technology 80 Inc.	Minneapolis, MN	(800) 545–2980, (612) 542–9545	73304.3301@compus- erve.com
TEIMA Audiotex	Madrid, Spain	+34 1 311–3878	Fax: +34 1 311 –2819
Tektronix Inc.	Beaverton, OR	(800) 426–2200, ext. 483	
Transtech Parallel Systems Corporation	Ithaca, NY	(607) 257–6502	transtech@trans- tech.com
Traquair Data Systems, Inc.	Ithaca, NY	(607) 266–6000	traquair@traquair.com
V.D.S. Video Display Systems s.r.l.	Firenze, Italy	+39–55–4378831	mc5083@mcmlink.it
VisionSmart Inc.	Edmonton, Alberta, Canada	(403) 435–7082	carl@planet.eon.net
Voice Processing Corporation	Cambridge, MA	(617) 494–0100	Fax: (617) 494–4970
Wavelink Technology Inc.	Taipei, Taiwan	+886–2–2995994	wavelink@c2.hinet.net
White Mountain DSP, Inc.	Nashua, NH	(603) 883–2430	info@wmdsp.com
Wintriss Engineering Corp.	San Diego, CA	(800) 550–7300, (619) 550–7300	weco@weco.com
Xcom Multimedia Communications	Montbonnot, France	+(33) 76 52 00 46	Fax: (33) 76 52 03 97
Zeelan Technology, Inc.	Beaverton, OR	(503) 520–1000	zeelan@netcom.com

Table 18–70. TMS320 Third-Party Consultant Contacts

Consultant	Location	Phone Number	E-mail Address/Fax
AB-RoBioMat di Angelo Baronchelli & Dott. Gábor Gulyás	Orzinuovi (BS), Italy	+30–943301 / +30–941264	gabor@galactica.it balazs@krypton77.nf.ki.se aszilvas@bih.harvard.edu
CHEOPS GmbH & Co. KG	Schongau, Germany	+ 49 8861 7902	100541.3370@compuserve.com
Czech Scientific and Technical Society	Prague, Czech Republic	+42 2 24310773	SIMAK@FELD.CVUT.CZ
D2 Technologies, Inc.	Santa Barbara, CA	(805) 564–3424	sales@d2tech.com
Dicon Lab, Inc.	Gainesville, FL	(904) 372–6160	diconlab@aol.com
Digital MultiWave Processing Inc.	Los Altos, CA	(415) 988–WAVE (9283)	digiwave@ix.netcom.com
DNA Enterprises, Inc.	Richardson, TX	(972) 644–3301	info@dna.metronet.com
Doctor Design Inc.	San Diego, CA	(619) 457–4545	boba@doctord.com
DSP Tools, Inc.	Potomac, MD	(301) 424–5808	davejervis@aol.com
Eberwein & Associates, Inc.	Houston, TX	(713) 784–1226	Fax: (713) 784–3651
Electronic Tools GmbH	Ratingen, Germany	+49 2102 8801–0	akohl@etools.de
Engineering Bureau	Munich, Germany	+(49) 89–5806137	Fax: +(49) 89–5806137
Eonic Systems Inc.	Linden, Belgium Silver Spring, MD	+32 16 62 15 85 (301) 572 5000	info@eonic.com eonic@bix.com
Epstein Associates	Wilmette, IL	(847) 853–9292	Fax: (847) 853–9293
ESSE–GI s.r.l.	Milan, Italy	+39 2 66017241	Fax: +39 2 6185492
Fraunhofer Institut Integrierte Schaltungen (IIS)	Erlangen, Germany	+49 9131 776 340	popp@iis.fhg.de
Genesis Engineering, Inc.	Ellicott City, MD	(410) 418–5410	klassen@access.digex.net
hema Elektronik Fertigungs und Vertriebs GmbH	Aalen, Germany	+7361/9495–0	info@hema.de
InnovaSystems, Inc.	Pennsauken, NJ	(609) 486–0030	76231.1053@compuserve.com
Innovative Integration Inc.	Westlake Village, CA	(818) 865–6150	techsprt@innovative-dsp.com
Institute for Integrated Circuits at the Technical University of Munich	Munich, Germany	+49–89–2105–3862	Fax: +49–89–2105–8323
JKJ Associates	Mt. Laurel, NJ	(609) 985–3068	kresse@waterw.com



Table 18–70. TMS320 Third-Party Consultant Contacts (Continued)

Consultant	Location	Phone Number	E-mail Address/Fax
M.B. International srl	Milano, Italy	+39 2 4091 0570	100522.2272@compuserve.com
MEDAV Digitale Signalverarbeitung GmbH	Uttenreuth, Germany	+49–9131/583–0	Fax: +49–9131/583–11
Miguel Chin	Cupertino, CA	(408) 252–5109	mca@cup.portal.com
Momentum Data Systems, Inc.	Costa Mesa, CA	(714) 557–6884	dsp@mds.com
MultiDSP Inc.	Cypress, CA	(714) 527–8086	multidsp@aol.com
MVP Development Group, Inc.	Lowell, MA	(508) 446–9166	Fax: (508) 446–9167
New World Systems	Westford, MA	(508) 692–4529	nuworld@world.std.com
Nova Engineering, Inc.	Cincinnati, OH	(513) 860–3456	sales@novaengr.com
OBJECTIF S.A.	Chatillon Cedex, France	+(1) 47 35 30 31	100117.1356@compuserve.com
Onyx Systems Limited	Bath, UK	+44 (0)1225 481173	Fax: +44 (0)1225 484025
Poznan University of Technology Institute of Electronics and Telecommunication	Poznan, Poland	+ 48 61 782 745	dabrow@et.put.poznan.pl
Primary Image Ltd.	Surbiton Surrey, UK Maitland, FL	+44 (0) 181 339 9669 (407) 667 4818	contact@pimage.demon.co.uk
Prodrive B.V.	Eindhoven, The Netherlands	+31 40 2461268	Fax: +31 40 2462362
QSD Sistemi SRL	Milan, Italy	+39 2 95741699	Fax: +39 2 9504773
Questa Consulting	Rochester, NY	(800) 785–6359	rhecht@questa.com
RECO SYST Research & Development	Emmerich, Germany	+49–2822–18731	Fax: + 49–2822–18744
Samjung Co., Ltd. Mediacom, Inc.	Seoul, Korea	+82–2–958–3386	kckim@speech.kaist.ac.kr
Sample Rate Systems, Inc.	Tampere, Finland	+358–31–3165 045	info@samplerate.fi
S.E.E.D.	Massa, Italy	+39 335 372256	mc4453@mclink.it
Signal-Data	Holte, Denmark	+45 3042 6054	sigdat@login.dknet.dk

Table 18–70. TMS320 Third-Party Consultant Contacts (Continued)

Consultant	Location	Phone Number	E-mail Address/Fax
Signals and Software Limited (SASL)	Middlesex, UK	+44 181 426 9533	davem@sasl.demon.co.uk
SIMONYI Kft. (SE&SE Ltd.)	Budapest, Hungary	+361 1416–421	Fax: 361 250–2249
Sinectonalysis, Inc.	Reno, Nevada	(702) 345–0148	sinecto@clark.net
Sonitech International	Wellesley, MA	(617) 235–6824	info@sonitech.com
Synetcom Digital, Inc.	Redondo Beach, CA	(310) 379–2000	73122,1112@Compuserve.Com
SYNTECH–CENTRE of Competence	Valbonne, France	(33) 93 65 28 66	syntech@slnet.mc
Systems Technology Associates	Cary, NC	(919) 460–0020	guerreri@nando.net
Tadpole Technology, Inc.	Austin, TX	(800) 232–6656	oem-sales@tadpole.com
Technical University of Wroclaw/Breslau	Wroclaw, Poland	+(48) 71–203032	KRZYK@ita.pwr.wroc.pl
Technosoft Ltd.	Bucharest, Romania	+(40) 1 772 0848	amotion@tag.vsat.ro
Tornado Software	Norco, CA	(909) 736–9655	senko@deltanet.com
University of Miskolc Department of Electrical and Electronic Engineering	Egyetemvaros, Hungary	+36 46 366–111/1218	elkadam@gold.uni-miskolc.hu
V.D.S. Video Display Systems s.r.l.	Firenze, Italy	+39–55–4378831	mc5083@mcLink.it
White Mountain DSP, Inc.	Nashua, NH	(603) 883–2430	info@wmdsp.com
Wintriss Engineering Corp.	San Diego, CA	(800) 550–7300	weco@weco.com
Zeidman Consulting	Cupertino, CA	(408) 255–9279	Zeidman@aol.com

Table 18–71. TMS320 Software Cooperative Resource Guide Contacts

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
3C	Herzogenrath, Germany	+49 2407 96056	portz@westend.com
3L Ltd.	Edinburgh, Scotland	+44 131 662 4333	threeL@threeL.co.uk
AB Nyvalla DS	Stockholm, Sweden	+468 790 9760	info@nyvalla-dsp.se
Accelerated Technology	Mobile, AL Worchire, UK	(334) 661–5770 +44–1527–6663	atisales@aticom geoffatuk@cityscape.co.uk
Advansis Software	River Edge, NJ	(201) 489–6018	tkl@ios.com
Atlanta Signal Processors, Inc.	Atlanta, Georgia	(404) 892–7265	aspi@aspi.com
CSELT	Torino, Italy	Fax: +39 11 228 620	Alberto.Ciaramella@cse.lt.stet.it
D2 Technologies, Inc.	Santa Barbara, CA	(805) 564–3424	sales@d2tech.com
Dallas Signal Processing, Inc.	Plano, TX	(972) 867–1739	Fax: (972) 985–5131
Digisonix, Inc.	Middleton, WI	(608) 836–3999	Fax: (608) 836–5583
DNA Enterprises, Inc.	Richardson, TX	(972) 644–3301	info@dna.metronet.com
DSP Software Engineering, Inc.	Bedford, MA	(617) 275–3733	sales@dspse.com
Elics	Paris, France	+33 14419 65 80	Fax: +33 1 44 19 65 89
ENEA DATA	Täby, Sweden	+46 8 638 50 00	ose@enea.se
Eonic Systems	Linden, Belgium Silver Spring, MD	+32 16 62 15 85 (301) 572 5000	info@eonics.com
France Telecom CNET	Lannion-Cedex, France	33–96–05–39–41	petitjp@lannion.cnet.fr
Inform Software Corporation	Oak Brook, IL Aachen, Germany	(708) 268–7550 +49–2408–9456	Fax: (708) 268–7554 Fax: +49–2408–6090
GAO Research & Consulting Ltd.	Toronto, Ontario, Canada	(416) 292–0038	gao@io.org
High-Tech Services Partners	Guyancourt, France	+33–1–30 57 31 13	Fax: +33–1–30 43 51 17
HotHaus Technologies	Delta, BC, Canada	(604) 946–0060	Fax: (604) 946–5811
IAT AG	Vogelsang-Turgi, Switzerland Bremen, Germany	+41 56 223 50 22 +49 421 20 21–0	fmueller@iat.ch A.Fuetterer@iat-gmbh.de

Table 18–71. TMS320 Software Cooperative Resource Guide Contacts (Continued)

Third-Party Contact	Location	Phone Number	E-mail Address/Fax
ILLICO!	Santa Clara, CA	(408) 980–8179	Fax: (408) 980–9327
Lernout & Hauspie Speech Products	Ieper, Belgium Woburn, MA SanChung, Taipei Hsien	+32–2–456–0500 (617) 932–4118 +886–2–999–2415	Fax: 32–2–460–0172 Fax: (617) 932–9209 www@lhs.com
M.B. International S.r.l.	Milano, Italy	+39 2 4091 0570	100522.2272@compuserve.com
Multiprocessor Toolsmiths Inc.	Kanata, Ontario, Canada	(800) 263–4377, x 224	answers@toolsmiths.on.ca
MultiDSP Inc.	Cypress, CA	(714) 527–8086	multidsp@aol.com
OROS	Meylan, France	+33.76.90.62.36	
Perihelion Distributed Software	Somerset, UK	+44 1749 344	sales@perihelion.co.uk
Precise Software Technologies Inc.	Boxborough, MA Nepean, Ont., Canada	(800) 628–8631 (800) 265–9833	info@psti.com
Recosyst R&D	Emmerich, Germany	+49 (2822) 18731	Fax: +49 (2822) 18744
Signals and Software Ltd.	Middlesex, UK	+44 (0) 181 426 9533	davem@sasl.demon.co.uk
S.E.E.D.	Massa, Italy	(+39) 335 372256	mc4453@mcLink.it
SignalWorks Inc.	Mountain View, CA	(415) 254–0186	70474.252@compuserve.com
Sinectonalysis, Inc.	Reno, NV	(702) 345–0148	sinecto@clark.net
Spectron Microsystems	Santa Barbara, CA Dublin, Ireland	(805) 968–5100 +353 1 676 1291	www: <a href="http://www.spectron.com">http://www.spectron.com</a>
SYNTECH	Valbonne, France	+ (33) 93 65 28 66	syntech@slnet.mc
Image Computing Systems Laboratory of the University of Washington	Seattle, WA	(206) 685–2271	kim@ee.washington.edu
ViaDSP, Inc.	Concord, MA	(508) 369–0048	viadsp@ix.netcom.com
Voice Processing Corporation	Cambridge, MA	(617) 494–0100	Fax: (617) 494–4970
Wideband Computers, Inc.	Mountain View, CA	(415) 962–8722	seth@wideband.com

# **TMS320 Seminars and Workshops**

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Texas Instruments offers a wide array of up-to-date technical product seminars and design workshops through its Technical Training Organization (TTO) to assist designers in developing the skills needed to implement their ideas quickly, produce a quality product, and shorten time to market. Applications assistance is also offered through local Customer Design Centers.

The DSP design workshops give design engineers hands-on experience using the latest TMS320 products, development tools, and design techniques. These workshops go beyond the standard lecture format. The exercises and lab experiments start with the basics and move quickly into hands-on exercises. In these workshops, the student learns by doing, not just listening or observing. The workshops are designed to help customers shorten the design cycle, control development costs, and solve design challenges.

<b>Topic</b>	<b>Page</b>
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## 19.1 TTO Services

The TTO offers 3- or 4-day DSP design workshops to assist users in the development of TMS320-based designs. These workshops are held at a TTO location or at a customer-selected site. Six different DSP design workshops are available, each covering a different generation of the TMS320 DSP family (see Table 19–1).

The main objective of each workshop is to demonstrate hardware and software techniques for implementing current DSP algorithms using a TMS320 digital signal processor. Exercises provide hands-on experience with the development tools needed for a quick start in designing with the TMS320 family.

*Table 19–1. Texas Instruments Technical Workshops*

Workshop Titles	Length, days
TMS320C2xx Family Digital Signal Processor Workshop	4.0
TMS320C3x Family Digital Signal Processor Workshop	3.5
TMS320C4x Family Digital Signal Processor Workshop	3.5
TMS320C5x Family Digital Signal Processor Workshop	4.0
TMS320C54x Family Digital Signal Processor Workshop	4.0
TMS320C8x Family Digital Signal Processor Workshop	4.0

### 19.1.1 Introduction to Technical Training

Success today means meeting competitive standards of quality, variety, customization, convenience, and timeliness. No longer is productivity the single measure of success. At Texas Instruments, your success in the design process is foremost on our minds.

Technological advancement and stiff competition are constantly driving the need to shorten the cycle time from design concept to market availability. State-of-the-art skills and practical application techniques are required in order to implement ideas quickly with a high degree of quality and value.

To help you meet these challenges, TI offers you the latest training and consultation on advanced technologies. Lectures led by skilled instructors and hands-on lab exercises using the latest TI development tools accelerate your learning experience. Real-world examples help you apply TI's advanced technology to your system. You will discover more productive ways of gaining that competitive edge.

TI workshops help you successfully:

- ☐ Solve design challenges
- ☐ Shorten the design cycle
- ☐ Control development costs

### 19.1.2 Registration and General Information

TI encourages early registration at least four weeks in advance. To register for a workshop within the United States, or for schedule information on courses in North America, call the TTO Central Registration office at (972) 644-5580 or (972) 917-3894 or a TI-authorized distributor. Workshops in Europe and Asia are offered through local Customer Workshops; for more information, contact the nearest Customer Design Center (see Section 19.3). For information on courses outside the United States, contact the nearest Customer Design Center.

Workshop enrollment is normally limited to 12 per class. All classes begin at 8:30 a.m.; full-day classes end at 5:00 p.m., and half-day classes end between 12:00 and 2:00 p.m. Tuition fees charged for our courses include study materials, use of facilities, personal copies of product documentation, design aids, continental breakfast, and lunch. Cancellation within 14 days before a workshop's start date incurs a \$500 cancellation fee.

#### **Additional Information:**

- ☐ If you have specific dietary constraints, please contact your training location.
- ☐ Smoking is not permitted in Texas Instruments facilities.
- ☐ The suggested attire is business casual.

### 19.1.3 TI Technical Training Locations

- ☐ **Boston**  
950 Winter Street, Suite 2800  
Waltham, MA 02154  
(617) 895-9185
- ☐ **Dallas**  
7839 Churchill Way  
Dallas, TX 75251  
(972) 917-3894

- ☐ **Irvine**  
1920 Main Street, Suite 900  
Irvine, CA 92714  
(408) 383–2363
- ☐ **San Jose**  
2825 North First Street, Suite 200  
San Jose, CA 95134  
(408) 383–2363

#### **19.1.4 TI Technical Training Design Workshops**

Texas Instruments Design Workshops provide the background and experience necessary for you to complete a TI microprocessor-based design. These workshops are valuable to engineers in any size company or project. They are of benefit in any of the following design stages:

- ☐ System design
- ☐ Processor evaluation/selection
- ☐ Hardware/software design

##### **19.1.4.1 Who Should Attend**

These workshops are targeted to any engineer with a basic knowledge of microprocessor design. Familiarity with basic assembly coding and embedded system design are helpful.

##### **19.1.4.2 What You Will Learn**

Design workshops focus on the architecture and instruction set. The courses cover the following information:

- ☐ System-level considerations
- ☐ Techniques for optimizing assembly and C code
- ☐ Coding algorithms to take advantage of the processor's architecture, buses, and special hardware features
- ☐ Writing a program from start to finish
- ☐ Hardware interface issues



#### **19.1.4.3 Hands-On Learning**

Using PC-based development tools, you will spend about 40 percent of the time writing code and solving problems. Numerous labs provide practice in such areas as using various addressing modes, implementing DSP algorithms, and working with peripherals.

### **19.1.5 Fixed-Point DSP Workshops**

The fixed-point DSP workshops are designed for individuals using the 'C2xx, 'C5x, and 'C54x family processors. Workshops are similar in structure and style, and topics cover the features and application issues for the included generations.

#### **19.1.5.1 TMS320C2xx Workshop**

This workshop covers the currently available 'C2xx products, which include the 'C203, 'C209, and the 'C2xLP core architecture (for use in developing cDSP designs). The material can be customized depending on your needs.

Topics covered include:

- ☐ Architectural overview
- ☐ Assembly language tools
- ☐ Data addressing modes
- ☐ Basic programming techniques
- ☐ Advanced programming techniques
- ☐ Numerical issues
- ☐ DSP fundamentals
- ☐ Logical operations
- ☐ Interrupts
- ☐ Logic/memory interfacing, special peripherals
- ☐ cDSP/ASIC design considerations
- ☐ Using the C compiler
- ☐ Design support

#### **19.1.5.2 TMS320C5x Workshop**

This workshop covers the 'C5x CPU architecture which is common between all the 'C5x device variations. The specific features of each device are compared and discussed.

Topics covered include:

- ☐ Architectural overview
- ☐ Assembly language tools
- ☐ Data addressing modes
- ☐ Basic programming techniques
- ☐ Advanced programming techniques
- ☐ Numerical issues
- ☐ DSP fundamentals
- ☐ Logical operations
- ☐ Interrupts
- ☐ Hardware interfacing
- ☐ Serial ports and multiprocessor features
- ☐ Using the C compiler

### **19.1.5.3 TMS320C54x Workshop**

Along with the 'C54x architecture and programming, you will learn to use the special hardware on this device, such as the Viterbi accelerator and buffered serial port. A study is made of the special (hardware supported) instructions useful for implementing standard telecom algorithms.

Topics covered include:

- ☐ Introduction to the 'C54x architecture
- ☐ Assembly language tools
- ☐ Data addressing modes
- ☐ Basic programming techniques
- ☐ Advanced programming techniques and pipeline issues
- ☐ Advanced mathematics
- ☐ Numerical issues
- ☐ DSP fundamentals
- ☐ Advanced DSP and specialized DSP hardware
- ☐ Interrupts
- ☐ Hardware interface
- ☐ Serial ports and special interface features

### **19.1.6 Floating-Point DSP Workshops**

The floating-point DSP workshops are designed for individuals using the 'C3x and 'C4x family processors. Workshops are similar in structure and style, and topics cover the features and application issues for the included generations.

#### **19.1.6.1 TMS320C3x Workshop**

The 'C3x represents the first generation of TI's 32-bit floating-point devices.

Topics covered include:

- ☐ Introduction to the 'C3x architecture
- ☐ Assembly language tools
- ☐ Data memory addressing
- ☐ CPU operations and floating point
- ☐ Enhanced CPU operations
- ☐ Pipeline and cache
- ☐ Direct memory access
- ☐ Interrupts
- ☐ Special addressing modes
- ☐ Memory interface
- ☐ Timers and serial ports
- ☐ Using the C compiler

### 19.1.6.2 TMS320C4x Workshop

The second family in TI's floating-point DSP lineup, the 'C4x workshop expands on the basic 32-bit DSP architecture by covering the advanced communication ports and DMA coprocessor.

Topics covered include:

- ☐ Introduction to the 'C4x architecture
- ☐ Assembly language tools
- ☐ Data memory addressing
- ☐ Basic CPU operations
- ☐ Floating-point and parallel instructions
- ☐ Pipeline and cache
- ☐ Interrupts
- ☐ Special addressing modes
- ☐ Memory interface
- ☐ Bootloader
- ☐ Communication ports
- ☐ DMA coprocessor
- ☐ Using the C compiler
- ☐ Parallel application development
- ☐ Design support

### 19.1.7 TMS320C8x Workshop

This workshop focuses on designing with the 'C80 multimedia video processor. The workshop covers device architecture, how the on-chip CPUs and resources function and interact, and programming with the parallel processors (PPs) and master processor. You also will learn how to use the development tools, including C compilers, assemblers, source-level debuggers, and the parallel debugging environment.

What you will learn:

- ☐ 'C80 architecture
- ☐ Functional block interaction
- ☐ Programming the PPs
- ☐ Programming the executive and master processor, calling library routines, and partitioning tasks
- ☐ Using development tools

**Outline**

- ☐ Introduction to 'C80 systems
- ☐ Introduction to C source debugger
- ☐ Crossbar and on-board memory organization
- ☐ Parallel processors (PP)
- ☐ Transfer controller (TC)
- ☐ Master processor (MP)
- ☐ 'C80 software architecture
- ☐ Video controller (VC)
- ☐ System design

**19.1.8 Course and Workshop Information**

For further information on courses and schedules in North America, call the Product Information Center at (972) 644-5580 or go to the TI semiconductor home page on the Internet: [www.ti.com/sc/docs/pic/home.htm](http://www.ti.com/sc/docs/pic/home.htm). Workshops in Europe, Asia, and other locations outside the United States are offered through local Customer Design Centers; for more information, contact the nearest Customer Design Center (see Section 19.3).

## **19.2 Design Services**

The TI technical staff can offer applications assistance with customer designs through local Customer Design Centers (see Section 19.3). Services include:

- ☐ Design assistance
- ☐ Simulation
- ☐ Emulation

Each Customer Design Center uses up-to-date development systems, including workstations and personal computers, plus demonstration, test, and evaluation equipment. TI staff designers use fully equipped laboratories to provide efficient design assistance.

The first step in a successful design is an explanation of the project's parameter: production requirements, design function(s), and price. The results of these discussions allow TI and a customer to explore:

- ☐ Design/cost trade-offs
- ☐ Product implementation options

After the various trade-offs/options are selected and approved, Texas Instruments can provide further assistance in the design of a customer's product, sharing a mutual goal of bringing a successful product to market as quickly as possible.

## 19.3 Customer Design Center Locations

Table 19–2 and Table 19–3 give the worldwide locations of the TI Customer Design Centers.

*Table 19–2. Customer Design Center North American Locations*

North American Locations	
<b>ATLANTA</b> Texas Instruments 5515 Spalding Drive Norcross, GA 30092 (404) 662–7950	<b>NORTHERN CALIFORNIA</b> Texas Instruments 2825 North First Street, Suite 200 San Jose, CA. 95134 (408) 383–2363
<b>BOSTON</b> Texas Instruments 950 Winter Street, Suite 2800 Waltham, MA 02154–1263 (617) 895–9196	<b>SOUTHERN CALIFORNIA</b> Texas Instruments 1920 Main St., Suite 900 Irvine, CA 92714 (714) 660–8140
<b>CHICAGO</b> Texas Instruments 515 W. Algonquin Road Arlington Heights, IL 60005 (708) 640–2909	<b>OTTAWA</b> Texas Instruments Canada, Ltd 301 Moodie Drive, Suite 102 Nepean, Ontario Canada, K2H 9C4 (613) 726–1970
<b>DALLAS</b> Texas Instruments 7839 Churchill Way Park Central V, MS 3984 Dallas, TX 75251 (972) 917–3881	<b>MEXICO CITY</b> Texas Instruments de Mexico Alfonso Reyes 115 Col. Hipodromo Condesa Mexico, D.F., Mexico 06170 (52) (5) 515–6081 (52) (5) 515–6249
<b>INDIANAPOLIS</b> Texas Instruments 550 Congressional Blvd., Suite 100 Carmel, IN 46032 (317) 573–6400	

Table 19–3. Customer Design Center International Locations

International Locations	
<b>AUSTRALIA</b> Texas Instruments Australia Ltd. 6–10 Talavera Road, North Ryde New South Wales, Australia 2113 (61) (2) 8789000	<b>JAPAN (Tokyo)</b> Texas Instruments Japan Ltd Ms Shibaura Building 9F 4–13–23 Shibaura Minato-Ku, Tokyo, JAPAN 108 (81) (3) 3769–8700
<b>BRAZIL</b> Texas Instruments Electronicos Rua Paez Leme, 524–7 Andar 05424 Sao Paulo, Brazil (55) (11) 815–6166	<b>JAPAN (Osaka)</b> Texas Instruments Asia LTD Osaka Branch Nissho-Iwai Bldg 5F 2–5–8 Imabashi Chuou-Ku Osaka, Japan 541 (81) (6) 204–1881
<b>FEDERAL REPUBLIC OF GERMANY</b> Texas Instruments Deutschland GMBH Kirchhorster Strasse 2 3000 Hannover 51, FR Germany (49) (511) 648021	<b>KOREA</b> Texas Instruments Korea Ltd. 28th Floor, Trade Tower 159 Samsung-Dong Kangnam-Ku, Seoul Trade Center P.O. Box 45 Seoul, Korea 135–729 (82) (2) 5512800
<b>FEDERAL REPUBLIC OF GERMANY</b> Texas Instruments Deutschland GMBH Haggertystrasse 1 8050 Freising, FR Germany (49) (8161) 80–0	<b>SINGAPORE</b> Texas Instruments Singapore (Pte) Ltd. Asia Pacific Division 101 Thomson Road #23–01 United Square Singapore 1130 (65) 2519818
<b>FRANCE (Paris)</b> Texas Instruments France 8–10 Avenue Morane Saulnier Boîte Postale 67 Velizy Villcoublay Cedex, France (33) (13) 0701001	<b>SWEDEN</b> Texas Instruments International Trade Corporation Box 30 S–164 93 Kista Isafjordsgatan 7, Sweden (8) 752–5800



Table 19–3. Customer Design Center International Locations (Continued)

International Locations	
<b>HONG KONG</b> Texas Instruments Hong Kong Ltd. 8th Floor, World Shipping Centre 7 Canton Road Kowloon, Hong Kong (852) 7351223	<b>TAIWAN</b> Texas Instruments Taiwan Ltd. Taipei Branch 10 Floor, Bank Tower 205 Tung Hua N. Road Taipei, Taiwan 105 Republic of China (886) (2) 7139311
<b>ITALY (Milan)</b> Texas Instruments Italia S.P.A. Centro Direzionale Colleoni Palazzo Perseo Via Paracelso, North 12 20041 Agrate Brianza, MI, Italy (39) (39) 63221	<b>UNITED KINGDOM</b> Texas Instruments Ltd. Regional Technology Center Manton Lane Bedford, England MK41 7PA (44) (234) 270111

Table 19–4. European Customer Training Infolines

Country	Contact	Telephone Number
France/Israel/Turkey/S. Africa	Sylviane Huguet	+33 1 30 70 11 57
Nordic	Marja Kinos	+46 87 52 58 36
United Kingdom	Claudia Dolente	+44 16 04 66 31 10
Benelux	Anne Marie Van Lint	+32 2 745 55 30
Italy/Spain/Portugal	Vanda Tomasi	+39 39 68 4 22 19
Central Europe	Martina Luther Beatrix Szeleczy	+49 81 61 80 44 86 +36 1 3 19 28 14

# TMS320 University Program

Texas Instruments believes it is important to train future engineers and encourages universities to do advanced research in the area of digital signal processing. TI has established the TMS320 University Program to make its resources available to universities and to assist in the incorporation of the TMS320 family information into engineering research and course curricula. The program provides considerable cost savings and expert technical assistance. Hundreds of universities are already taking advantage of this program.

Through the TMS320 University Program, TI offers discounts on development tools, software donations, expert engineering assistance for university research, and third-party contacts. TMS320 documentation and technical hot-line assistance can be found on the DSP Solutions World Wide Web (WWW) home page at:

**<http://www.ti.com/dsps>**

In addition, numerous TMS320 textbooks, including lab manuals and user's guides, are published to support digital signal processing research and education at the graduate and undergraduate levels (refer to Section 17.5, *University Textbooks*, for a description of the TMS320 textbooks).

**Note:**

Texas Instruments reserves the right to make changes at any time in its TMS320 University Program policies.

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## 20.1 Development Tools Available to Universities

TMS320 DSPs including the 'C1x, 'C2x, 'C2xx, 'C3x, 'C4x, 'C5x, 'C54x, and 'C8x and associated development tools are available to universities at a discount. For purchase, contact any of TI's authorized distributors.

The code-generation tools include the TMS320 macro assembler, linkers, and C compiler packages (includes assembler/linker).

The system integration and debug tools include XDS™, emulators, simulators, EVMs, DSP Starter Kits (DSKs), and adapters.

The DSP Teaching Kit (EDSKIT-DSP/DTK) includes the following in one box:

- ☐ Five lectures on the basics of DSP
- ☐ 'C5x DSK card
- ☐ Power supply
- ☐ Connectors and cables
- ☐ Demonstration program, including source code
- ☐ Overhead transparencies
- ☐ Test material
- ☐ Student notes
- ☐ Lecturer's Guide
- ☐ Supporting textbook: *"A Simple Approach to DSP"* by Craig Marven and Gillian Ewers (Wiley)

## 20.2 DSP Lab Workstation Recommendations

The DSP lab workstation, designed for use at the undergraduate and first-year graduate levels, allows students to practice the theory learned in an associated DSP course. Students can design DSP systems using practical examples and perform real-time DSP simulations. A DSP lab usually consists of four or five workstations. Workstations typically include the following:

☐ **'C2x Lab Workstation**

- PC or Sun/SPARC
- 'C2x simulator
- 'C2x EVM (or 'C2x DSK)
- 'C2x/'C5x optimizing ANSI C compiler package
- 'C2x/'C5x assembler/linker

☐ **'C2xx Lab Workstation**

- PC or Sun/SPARC
- 'C2xx simulator
- 'C5x EVM (or 'C5x DSK)
- 'C2xx optimizing ANSI C compiler/assembler/linker package

☐ **'C3x Lab Workstation**

- PC or Sun/SPARC
- 'C3x simulator
- 'C3x EVM (or 'C3x DSK)
- 'C3x/'C4x optimizing ANSI C compiler package
- 'C3x/'C4x assembler/linker

☐ **'C4x Lab Workstation**

- PC or Sun/SPARC
- 'C4x simulator
- 'C3x/'C4x optimizing ANSI C compiler
- 'C3x/'C4x assembler/linker

☐ **'C5x Lab Workstation**

- PC or Sun/SPARC
- 'C5x simulator
- 'C5x EVM (or 'C5x DSK)
- 'C2x/'C5x optimizing ANSI C compiler package
- 'C2x/'C5x assembler/linker

☐ **'C54x Lab Workstation**

- PC or Sun/SPARC
- 'C54x simulator
- 'C54x EVM
- 'C54x optimizing ANSI C compiler/assembler/linker package

☐ **'C8x Lab Workstation**

- PC
- 'C8x SDB
- 'C8x PC software toolset

The following textbooks are recommended for the indicated workstation environments:

☐ **'C2x Workstation**

- *TMS320C2x User's Guide* from Texas Instruments (literature number SPRU014C) (Prentice-Hall)
- *Digital Signal Processing With C and the TMS320C25*, by Chassaing and Horning (John Wiley & Sons)

☐ **'C2xx Workstation**

*TMS320C2xx User's Guide* from Texas Instruments (literature number SPRU127A) (Prentice-Hall)

☐ **'C3x Workstation**

- *TMS320C3x User's Guide* from Texas Instruments (literature number SPRU031D)
- *Digital Signal Processing Applications With the TMS320C30 Evaluation Module* from Texas Instruments (literature number SPRA021)
- *Communication System Design Using DSP Algorithms*, by Steven A. Tretter (Plenum Publishing)

☐ **'C4x Workstation**

*TMS320C4x User's Guide* from Texas Instruments (literature number SPRU063A)

☐ **'C5x Workstation**

*TMS320C5x User's Guide* from Texas Instruments (literature number SPRU056B)

❑ **'C54x Workstation**

*TMS320C54x User's Guide* from Texas Instruments (literature number SPRU131B)

Additional TMS320 DSP textbooks are available (refer to Section 17.5, *University Textbooks*, for a complete listing).

## 20.3 DSP Research Workstations

A DSP research lab workstation is created by adding the following equipment to the DSP lab workstation:

☐ **'C2x Research Workstation**

- TMS320C2x XDS/22 emulator
- DSP software library

☐ **'C2xx Research Workstation**

- XDS510™ emulator (PC or Sun/SPARC)
- 'C2xx HLL Debugger (PC or Sun/SPARC)

☐ **'C3x Research Workstation**

- XDS510 emulator (PC or Sun/SPARC)
- 'C3x HLL Debugger (PC or Sun/SPARC)

☐ **'C4x Research Workstation**

- XDS510 emulator (PC or Sun/SPARC)
- 'C4x HLL Debugger (PC or Sun/SPARC)
- 'C4x Parallel Processing Development System (PPDS)

☐ **'C5x Research Workstation**

- XDS510 emulator (PC or Sun/SPARC)
- 'C5x HLL Debugger (PC or Sun/SPARC)

☐ **'C54x Research Workstation**

- XDS510 emulator (PC or Sun/SPARC)
- 'C54x HLL Debugger (PC or Sun/SPARC)

☐ **'C8x Research Workstation**

- XDS510 emulator (Sun/SPARC)
- 'C8x HLL Debugger (PC or Sun/SPARC)
- 'C8x Software Toolkit (Sun/SPARC)

After the DSP lab workstation or DSP research workstation is set up, Texas Instruments provides continued support to the university in the form of suggestions for DSP projects, up-to-date documentation, TMS320 WWW site and BBS, and a hotline. Third-party companies offer special workstation packages and development tools that support the TMS320 digital signal processors.

For more information about the TMS320 University Program and associated pricing, write or e-mail to:

Texas Instruments Incorporated  
University Program  
P.O. Box 1443, M/S 722  
Houston, TX 77251-1443  
e-mail: univ@msg.ti.com

In Europe, contact:

Texas Instruments Ltd.  
University Programme  
800 Pavilion Drive  
Northhampton Business Park  
Northhampton  
NN4 7YJ  
England (United Kingdom)  
e-mail: epic@ti.com

In the Asia/Pacific region, contact:

Texas Instruments Hong Kong Ltd.  
University Program  
15/F., Tower II, The Gateway  
24-27 Canton Road  
Kowloon, Hong Kong

In Japan, contact:

Texas Instruments Japan Ltd.  
University Program  
MS-Shibaura Bldg. 4-13-23, Shibaura  
Minato-ku, Tokyo 108  
Japan



# Factory Repair and Exchange Instructions

The Microprocessor Development Systems' Factory Repair Center in Houston, Texas (and other locations worldwide), offers warranty repair or exchange at no charge (except shipping) and nonwarranty repair at standard labor and material rates for all current products. You can receive expedited service on exchanges at an additional cost.

**Note:**

If TI accepts your unit for repair and you ask for return of the same serial-numbered unit, TI will repair that specific unit. If you do not ask for return of the specific serial-numbered unit, TI reserves the option to repair your returned unit or to exchange it for an equivalent unit.

Exchanged products will be replaced with refurbished units that meet TI workmanship standards for refurbished products.

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A.5 Charges and Method of Payment .....	A-6

## A.1 Normal Warranty Exchange or Repair

TI repairs or exchanges products free of charge, provided:

- ☐ You notify Texas Instruments of the problem within ninety (90) days of shipment from Texas Instruments or an authorized distributor.
- ☐ Factory Repair Center's inspection shows that the problem(s) was not caused by accident, alteration, improper installation, improper testing, misuse, neglect, or unauthorized repair.

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**Note:**

Texas Instruments does not accept responsibility for customer-installed changes, including, but not limited to, customer-generated software in programmable devices. Texas Instruments also reserves the right to refuse to repair and the right to return, at the customer's expense, any product that cannot be tested to its specifications because of the customer's modifications.

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## **A.2 Nonwarranty Exchange or Repair**

Nonwarranty factory repair or exchange is available on all current and repairable Microprocessor Development Systems products. TI accepts your product as repairable if the cost of repair does not exceed the cost of replacement. Otherwise, you will be notified that the product cannot be classified as repairable and the product will be promptly returned to you.

## **A.3 System Updates**

The standard TI practice is to update each Microprocessor Development Systems product that is returned for repair to the current revision of the make and model. Extra charges may apply to some updates.

## A.4 Shipping Instructions

For any factory repair or upgrade, follow these instructions:

- 1) If you reside within the United States or Canada, contact the Factory Repair Center at (281) 274–2285 and ask for a *Return Material Authorization* (RMA) number.

If you reside outside of the United States or Canada, contact the nearest RTC or local sales office for instructions.

**Note:**

TI cannot be responsible for any product returned without prior authorization.

- 2) Fill out the *Factory Repair and Exchange Questionnaire* card that came with the warranty papers. Provide the following information:
  - The RMA number; note that Texas Instruments will not accept your equipment without this number
  - Your name, contact name (if applicable), and telephone number
  - Purchase order number (if applicable)
  - Proof of date of purchase (required for warranty repair)
  - Model number
  - Serial number
  - *Ship To* information, including address, amount of insurance, and shipping method; note that Texas Instruments ships by UPS or its equivalent and insures for the minimal amount, unless you specify otherwise
  - *Bill To* address
  - If desired, request for return of same serial-numbered unit
  - Description of symptoms—please be as detailed as possible
- 3) Make a copy of the waybill and the *Factory Repair and Exchange Questionnaire* card for your records in case tracing of your shipment becomes necessary.
- 4) Pack the unit carefully and securely, preferably with the packing material from its original shipping box. If the original packing material is not available, be sure to use an antistatic packing material where needed to prevent electrostatic discharge damage to board assemblies, components, and target cables. Before sealing, enclose the original copies of the waybill and the *Factory Repair and Exchange Questionnaire*.

- 5) Return your product (freight prepaid) to the appropriate Factory Repair Center. Within the United States and Canada, send the unit to:

Texas Instruments Incorporated  
Microprocessor Development Systems  
Factory Repair Center, M/S 730  
12203 Southwest Freeway  
Stafford, Texas 77477

Outside of the United States and Canada, your local contact will provide shipping instructions.

## **A.5 Charges and Method of Payment**

Most products are repaired on a fixed-price repair basis, provided that the returned product is repairable. Fixed repair prices do not include the cost of repairing items damaged through accident, alteration, improper installation, misuse, neglect, or unauthorized repair. Certain factory upgrades may also incur an extra charge.

You will be notified if the cost of repair exceeds the standard fixed-price rate. You may request return of the same serial-numbered product or may exchange it for a refurbished product.

You may request expedited exchange service at an extra cost, subject to product inventory. The requested product will be shipped within one (1) working day from receipt of the returned product. Product is returned (F.O.B.) to the customer by the Factory Repair Center. Transportation and insurance charges are added to the customer's invoice.

# Program License Agreement

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Software programs included with TI Microprocessor Development Systems products are distributed subject to the terms of the license agreement included with the program package, unless a separate written agreement is executed.

A typical TI program license agreement is reproduced on the following page for your reference (note that some Microprocessor Development Systems products include third-party software programs distributed under license by TI, under the terms of the specific agreement packaged with them).

The license terms give you the right to use the program on a single-host computer system. You may move these programs from machine to machine, providing that you do not violate the copyright by making unauthorized copies and/or installing the program on more than one host computer at a time.

Programs on floppy-disk media are typically limited to single-user computer systems. Use of these programs on multiuser host systems requires the payment of additional fees. All other programs may be used on either single- or multiple-user systems, including those with remote log-on capability.

Installation of a program on a server for transmission over a network requires that a network-extension license be obtained (payment of additional fees required) for the program in question.

Some software may be identified as runtime libraries or application software in the user documentation. The terms of the license normally allow you to modify this software and otherwise derive programs from it. When this software is supplied in source-code format, the source-code versions are subject to the terms of the agreement, but the object-code versions are not.

---

## PROGRAM LICENSE AGREEMENT

This document is displayed for you to read prior to using the software and documentation. By using the software and documentation, you agree to abide by the following provisions. If you choose not to agree with these provisions, promptly return the unopened package to the place you obtained it for a refund.

- 1) **License**—Texas Instruments Incorporated ("TI"), grants you a license to use the software program and documentation in this package ("Licensed Materials") on a single-user computer in the case of software on floppy disc media or a single computer in the case of all other software. You may not use the Licensed Materials on more than one computer at the same time or otherwise network the Licensed Materials. Use of the Licensed Materials on a network requires payment of additional fees.
- 2) **Restrictions**—You may not reverse-assemble or reverse-compile the Licensed Materials provided in object code format. You may not sublicense, transfer, assign, rent, or lease the Licensed Materials or this Agreement without written permission from TI.
- 3) **Copyright**—The Licensed Materials are copyrighted. Accordingly, you may either make one copy of the Licensed Materials for backup and/or archival purposes or copy the Licensed Materials to another medium and keep the original Licensed Materials for backup and/or archival purposes. Additionally, if this package contains multiple versions of the Licensed Materials, then you may only use the Licensed Materials in one version on a single computer. In no event may you use two copies of the Licensed Materials at the same time. You must reproduce the copyright notice on each copy or partial copy of the software.
- 4) a. **Runtime and Applications Software**—You may create modified or derivative programs of software identified as Runtime Libraries or Applications Software, which in source code form remain subject to this Agreement, but object code versions of such derivative programs are not subject to this Agreement.  
b. **Operating System and Device Driver Software**—Certain products may contain operating system and device driver software. The license granted is for applications development only. A separate license must be obtained from TI to distribute copies.
- 5) **Warranty**—TI warrants the media to be free from defects in material and workmanship and that the software will substantially conform to the related documentation for a period of ninety (90) days after the date of your purchase. TI does not warrant that the Licensed Materials will be free from error or will meet your specific requirements.
- 6) **Remedies**—If you find defects in the media or that the software does not conform to the enclosed documentation, you may return the Licensed Materials along with the purchase receipt, postage prepaid, to the following address within the warranty period and receive a refund.

Texas Instruments Incorporated  
Microprocessor Development Systems MS 730  
12203 Southwest Freeway  
Stafford, Texas 77477

- 7) **Limitations**—***TI makes no warranty or condition, either expressed or implied, including but not limited to any implied warranties of merchantability and fitness for a particular purpose, regarding the licensed materials.***

Neither TI nor any applicable licensor will be liable for any incidental or consequential damages, including but not limited to lost profits.

Because some states do not allow the exclusion or limitation of incidental or consequential damages or limitation on how long an implied warranty lasts, the above limitations or exclusions may not apply to you.

- 8) **Export Control** — The re-export of United States origin software and documentation is subject to the Export Administration Act of 1969 as amended. Compliance with such regulations is your responsibility.

2547316-9791 revision B



# ROM Codes



This appendix defines the scope of code-customized DSPs and describes the procedures for developing prototype and production units. Information on submitting object code and on ordering customer ROM-coded devices is also included.

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## C.1 Scope

A repetitive routine (for example, boot code) or an entire system algorithm can be embedded (programmed) into the on-chip ROM of a TMS320 DSP. With external memory expansion still available, this reduces the total chip count and allows for more flexibility in program design. Multiple functions are easily implemented by a single device, thus enhancing the system's capabilities. In many instances, embedded ROM code can reduce the bulk and mechanical size of the end application.

The embedded device, due to its customer-specific code, can only be offered for sale as such to that customer or the customer's formally designated representative. The customer's intellectual property (that is, his unique embedded code level) within the device is protected by a unique part number, as well as customer copyright indicated by device symbolization.

Code-customized DSP processors offer these advantages:

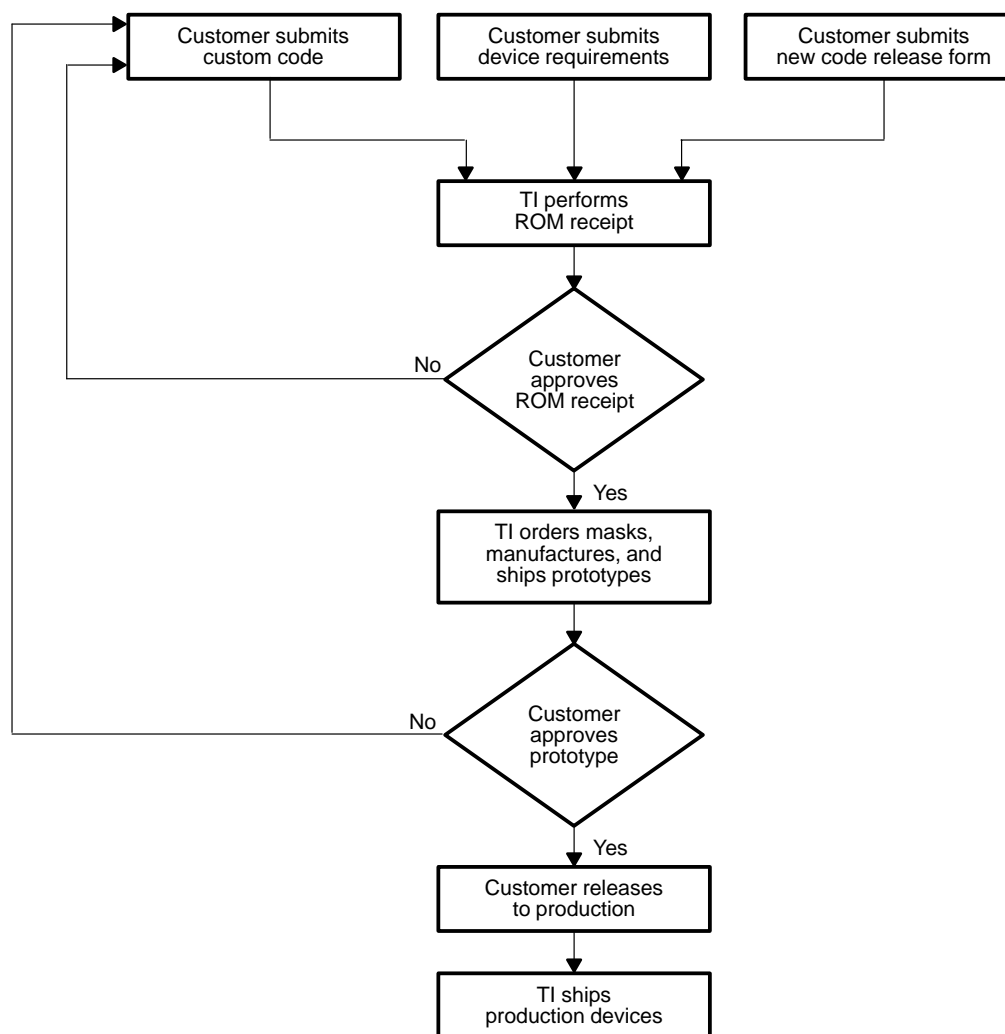
- ☐ Lower system cost for volume-driven applications
- ☐ Extended system memory expansion capability
- ☐ Reduced system hardware and wiring
- ☐ More compact/less expensive PCB
- ☐ Enhanced security for proprietary software implementations

Standard TMS320 development tools are used to develop, test, refine, and finalize the algorithms. The microprocessor/microcomputer mode ( $\overline{MC}/\overline{MP}$  for 'C1x, 'C3x, and 'C4x;  $\overline{MP}/\overline{MC}$  for 'C2x, 'C2xx, and 'C5x) is available on all ROM-coded TMS320 DSP devices when accessing either on-chip or off-chip memory is required. The microprocessor mode is used to develop, test, and refine a system application. In this mode of operation, the TMS320 acts as a standard microprocessor by using external memory only. When the algorithm has been finalized, you may submit the code to Texas Instruments for masking into the on-chip program ROM. At that time, the TMS320 becomes a microcomputer that executes a customized program out of the on-chip ROM. Should the code need changing or upgrading later, the TMS320 may once again be used in the microprocessor mode for development to manage the transition to the revised ROM code. This simplifies the upgrade process by allowing for a "rolling (code) change," and reduces the possibility of finished and work-in-process inventory obsolescence, while affording an orderly continuation of end-product output.

## C.2 Procedure

Figure C–1 illustrates the procedural flow for TMS320 masked parts. When ordering, there is a one-time nonrefundable (NRE) charge for mask tooling and related one-time engineering costs. This charge also covers the costs for a finite number of supplied prototype units. A minimum production order per year is required for any masked-ROM device, and assurance of that order is expected at the time of NRE order acceptance.

Figure C–1. TMS320 ROM Code Prototype and Production Flowchart



### C.2.1 Customer Required Information

For TI to accept the receipt of a customer ROM algorithm, each of the following three items must be received by the TI factory.

- 1) The customer completes and submits a New Code Release Form (NCRF—available from TI Field Sales Office) describing the custom features of the device (for example, customer information, prototype and production quantities and dates, any exceptions to standard electrical specifications, customer part numbers, and symbolization, package type, etc.).
- 2) If nonstandard specifications are requested on the NCRF, the customer submits a copy of the specification for the DSP in the customer's system, including functional description and electrical specification (including absolute maximum ratings, recommended operating conditions, and timing values).
- 3) When the customer has completed code development and has verified this code with the development system, the standard TMS320 tagged object code is submitted to the TI factory via any of the following.
  - ☐ EPROM devices (currently supported: TMS27C64, TMS27C128, and TMS77C82)
  - ☐ MS-DOS formatted disk compatible with IBM PC
  - ☐ Electronic ROM transfer: PC-to-PC via Xmodem, Ymodem, Zmodem, or Microsoft's Crosstalk protocol

The completed NCRF, customer specification (if required), and ROM code should be given to the TI Field Sales Office or sent to:

Texas Instruments Digital Signal Processor Products  
ATTN: TMS320 DSP Marketing Manager-ROM Receipt, M/S 704  
P.O. Box 1443  
Houston, Texas 77251-1443

### C.2.2 TI Performs ROM Receipt

Code review and ROM receipt is performed on the customer's code and a unique manufacturing ROM code number (such as Dxxxxx) is assigned to the customer's algorithm. All future correspondence should indicate this number. The ROM receipt procedure reads the ROM code information, processes it, reproduces the customer's ROM object code on the same media on which it was received, and returns the processed and the original code to the customer for verification of correct ROM receipt.

### C.2.3 Customer Approves ROM Receipt

The customer then verifies that the ROM code received and processed by TI is correct and that no information was misinterpreted in the transfer. The customer must then return written confirmation of correct ROM receipt verification or resubmit the code for processing. This written confirmation of verification constitutes the contractual agreement for creation of the custom mask and manufacture of ROM verification prototype units.

### C.2.4 TI Orders Masks, Manufactures, and Ships Prototypes

TI generates the prototype photomasks, processes, manufactures, and tests microcomputer prototypes containing the customer's ROM pattern for shipment to the customer for ROM code verification. These devices have been made using the custom mask but are for the purposes of ROM verification only. For expediency, the prototype devices are tested only at room temperatures (25°C). **Texas Instruments recommends that prototype devices not be used in production systems.** Prototype devices are symbolized with a **P** preceding the manufacturing ROM code number (for example, PDxxxxx) to differentiate them from production devices.

### C.2.5 Customer Approves Prototype

The customer verifies the operation of these prototypes in the system and responds with written customer prototype approval or disapproval. This written customer prototype approval constitutes the contractual agreement to initiate volume production using the verified prototype ROM code.

### C.2.6 Customer Release to Production

With customer algorithm approval, the ROM code is released to production and TI begins shipment of production devices according to the customer's final specifications and order requirements.

Two lead times are quoted in reference to the preceding flow:

- ☐ **Prototype lead time** is the elapsed time from the receipt of written ROM receipt verification to the delivery of the prototype devices.
- ☐ **Production lead time** is the elapsed time from the receipt of written customer prototype approval to the delivery of production devices. For the latest TMS320 family lead times, contact the nearest TI Field Sales Office.

### **C.3 Code Submittal**

The customer's object code can be submitted on either 3.5-inch or 5.25-inch disk, EPROM, or via electronic transmittal (that is, modem, Internet, other). For 'C1x or 'C2x family codes, Intel Hex or TI-tagged format is required; for all other families, COFF format from the cross-assembler/linker is needed.

When a code is submitted to Texas Instruments for masking, the code is reformatted by TI to accommodate the TI mask-making and test program generation systems. Application-level verification by the customer is, therefore, necessary. Although the code has been reformatted, it is important that the changes remain transparent to the user and do not affect the execution of the algorithm submitted. Those formatting changes consist essentially of adding ease-of-manufacturing code in reserved and not used (customer) locations only. Resulting code has the code address beginning at the base address of the ROM in the TMS320 device and progressing without gaps to the last address of the ROM on the TMS320 device. Note that because these changes have been made, a checksum comparison is not a valid means of verification. Upon satisfactory verification of the TI returned code, the customer advises TI in writing that it is verified, and this enables release to manufacturing and acceptance of initial orders.

## C.4 Ordering

Customer embedded-code devices are user-specified, and thus, each is an unreleased new product until prototype approval and formal release to production. With each initial order of a ROM-coded device, the customer must include written recognition that he understands the following:

**The units to be shipped against this order were assembled, for expediency purposes, on a prototype (that is, nonproduction qualified) manufacturing line, the reliability of which is not fully characterized. Therefore, the anticipated reliability of these prototype units cannot be defined.**

Sometimes to shorten time to market and upon mutual agreement, the customer may order (and TI will accept) a Risk Production order prior to prototype approval. Under this noncancellable order arrangement, the customer agrees to accept delivery of product containing his code as initially verified and TI agrees to ship to that requirement. The customer is, in effect, agreeing to not change the originally submitted code for the Risk Production order units. He must use the term "Risk Production" in a letter or in a note on the order as a matter of record.

TI does reserve the right to sell excess customer ROM-coded devices as standards to reduce the financial liability incurred through premature ordered quantity reductions or overbuilds. Units thus marketed by TI have all original customer custom symbols or other means of external identification, removed and replaced by a standard product symbol to mask the custom die presence. It is standard practice to require a one-time statement from the customer stating that the customer knows and concurs.

Your local TI Field Sales Office and/or TI Authorized Distributor can be of further assistance on embedded ROM procedure questions and in actually processing your code.

## TMS320 PROM Programming

The programmable read-only memory (PROM) versions of the TMS320 family include a 4K-word  $\times$  16-bit PROM implemented with an industry-standard PROM cell. These devices can be used for prototyping, early field testing, low-volume production (windowed versions), or high-volume production (one-time programmable versions). The CMOS counterparts of the TMS320 family with a 4K-word masked ROM offer a migration path for cost-effective/higher-volume production. PROM adapter sockets are available that provide 40-pin-to-28-pin conversion for programming the TMS320P15 and TMS320P17. Adapter sockets are also available to provide the 68-pin-to-28-pin conversion required for programming the TMS320P14. Refer to Table 2–14 in Chapter 2, *Selection Guide*, for part numbers.

Key features of the PROM cell include standard programming and verification. The PROM cell also includes a code protection feature that allows code to be protected against copyright violations. The protection feature can be used to prevent the reading of the PROM contents. This appendix describes programming, version verification, and PROM security.

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D.2 Fast and SNAP! Pulse Programming .....	D-4
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## D.1 Programming

The TMS320 PROM cell is programmed using the same family and service codes as the TMS27C64  $8K \times 8$ -bit EPROM uses. The TMS27C64 EPROM series are ultraviolet-light erasable, electrically programmable read-only memories. They are fabricated using HVCMOS technology. The TMS27C64 is pin compatible with existing 28-pin ROMs and EPROMs.

The TMS320 PROM family, like the TMS27C64, operates from a single  $5-V_{DC}$  supply in the read mode. In the programming mode, an additional  $12.5-V_{DC}$  supply is required. All programming signals are TTL level. Memory locations can be programmed individually, in blocks, or at random. Many of the commercial EPROM programmers can be used for programming outside of the resident system.

In **block programming**, data is loaded into the TMS320 PROM one byte at a time. From the programmer's point of view, data for each memory location is loaded high byte first, low byte second.

The PROM versions of the TMS320 family do not support the **signature** mode available with some EPROM programmers. The signature mode on these programmers places a high voltage ( $12.5 V_{DC}$ ) on address pin **A9**. The TMS320 PROM cell is not designed for this feature and will be damaged if subjected to this voltage. A  $3.9\text{-k}\Omega$  resistor is standard on the TI programmer socket between address pin **A9** and the programmer. This protects the device from unintentional use of the signature mode.

Each ROM version of a TMS320 DSP device has a reserved area for TI internal use. When developing a ROM code for release on a TI DSP, do not use this portion of the ROM.

The reserved areas that cannot be used for ROM code development are listed in Table D–1.

Table D–1. TMS320 DSP ROM-Based Devices

Device	On-Chip ROM	No. of Words Reserved for Testing	Address of Reserved ROM
TMS320C1x			
C14	4K	96	0FA0 – 0FFFh (4000–4095)
C15	4K	96	0FA0 – 0FFFh (4000–4095)
LC15	4K	96	0FA0 – 0FFFh (4000–4095)
C16	8K	80	1FB0 – 1FFFh (8112–8191)
C17	4K	96	0FA0 – 0FFFh (4000–4095)
LC17	4K	96	0FA0 – 0FFFh (4000–4095)
TMS320C2x			
C25	4K	80	0FB0 – 0FFFh (4016–4095)
TMS320C2xx			
C204	4K	96	0FA0 – 0FFFh (4000–4095)
TMS320C5x			
C51	8K	256	1F00 – 1FFF (7936–8191)
C52	4K	256	0F00 – 0FFF (3840–4095)
C53	16K	256	3F00 – 3FFF (16128–16383)
C56	32K	256	7F00 – 7FFF (32512–32767)
C57	32K	256	7F00 – 7FFF (32512–32767)
TMS320C54x			
C541	28K	128	FF00 – FF7Fh (65280–65407)
C545	48K	128	FF00 – FF7Fh (65280–65407)
C546	48K	128	FF00 – FF7Fh (65280–65407)

## D.2 Fast and SNAP! Pulse Programming

Two programming algorithms are available for TMS320 PROM devices. The *fast programming* algorithm is normally used to program the entire PROM contents, although individual locations may be programmed separately. Fast programming is supported on the TMS320P14, TMS320P15, and TMS320P17. The other TI algorithm, *SNAP! pulse programming*, can reduce the programming time to a nominal duration of one second. Note that actual programming time varies as a function of the programmer being used. SNAP! pulse programming is supported on the TMS320P14. For more information on these two programming algorithms, consult the appropriate TMS320 user's guide.

### **D.3 Version Verification**

Information on verification of the PROM versions of the TMS320 family is contained in the appropriate TMS320 user's guide.

### **D.4 PROM Security**

The PROM protection mechanism completely disables a TMS320 device and prevents reading of the PROM contents. This guarantees the security of proprietary algorithms. This facility is implemented through a unique PROM cell called the ROM-protect bit (RBIT) cell. Once the contents are programmed into the PROM, the RBIT can be programmed, preventing access to the PROM contents and disabling the microprocessor mode on the TMS320 device. Once programmed, the RBIT can be cleared only by erasing the entire EPROM array with ultraviolet light, thus maintaining security of the proprietary algorithm. Information on programming and verification of the RBIT is available in the appropriate TMS320 user's guide.

# Glossary

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**A0–A15:** External address pins for data/program memory or I/O devices.

**ACC:** See *accumulator (ACC)*.

**accumulator (ACC):** A 32-bit register that stores the results of an arithmetic logic unit (ALU) operation and provides an input for subsequent ALU operations. The ACC is accessible in two halves: accumulator high (ACCH) and accumulator low (ACCL).

**active window:** The window that is currently selected for moving, sizing, editing, closing, or some other function.

**ADC:** See *analog-to-digital converter*.

**address:** The logical location of program code or data stored in memory.

**addressing mode:** The method by which an instruction calculates the location of its required data.

**ADTR:** *Asynchronous data transmit and receive register*. An 8-bit register in the asynchronous serial port that writes the data to transmit and reads the data received. See also *ARSR*.

**aliasing:** A method of customizing debugger commands; aliasing provides a shorthand method for entering often-used command strings.

**ALU:** See *arithmetic logic unit*.

**analog-to-digital converter (ADC):** A successive-approximation converter with internal sample-and-hold circuitry used to translate an analog signal to a digital signal.

**ANSI C:** A version of the C programming language that conforms to the C standards defined by the *American National Standards Institute*.

**AR0–AR7:** *Auxiliary Registers 0–7*. Eight 16-bit registers that are used as pointers to an address within the data space address range. The registers are operated on by the auxiliary register arithmetic unit (ARAU) and are selected by the auxiliary register pointer (ARP).

**ARAU:** See auxiliary-register arithmetic unit.

**ARB:** See *auxiliary register pointer buffer*. A 3-bit field in status register ST1 that holds the previous value of the auxiliary register pointer (ARP).

**archive library:** A collection of individual files that have been grouped into a single file.

**archiver:** A software program that allows you to collect several individual files into a single file called an archive library. The archiver also allows you to delete, extract, or replace members of the archive library, as well as to add new members.

**arithmetic logic unit (ALU):** The part of the CPU that performs arithmetic and logic operations.

**ARP:** *Auxiliary register pointer*. A 3-bit field in status register ST1 used as a pointer to the currently selected auxiliary register.

**ARSR:** *Asynchronous receive shift register*. An 8-bit register in the asynchronous serial port that receives data from the TX pin one bit at a time and, when ARSR is full, it transfers its data to the ADTR. See also *ADTR*.

**ASCII:** American Standard Code for Information Interchange. A standard computer code for representing and exchanging alphanumeric information.

**assembler:** A software program that creates a machine-language program from a source file that contains assembly language instructions, directives, and macro directives. The assembler substitutes absolute operation codes for symbolic operation codes, and absolute or relocatable addresses for symbolic addresses.

**assembly mode:** A debugging mode that shows assembly language code in the DISASSEMBLY and doesn't show the FILE window, no matter what type of code is currently running.

**asynchronous data transmit and receive register (ADTR):** An 8-bit register in the asynchronous serial port that writes the data to transmit and reads the data received. See also *ARSR*.

**asynchronous serial port control register (ASPCR):** A 16-bit register in the asynchronous serial port that controls signals IO0–IO3, breaks, stop bits, auto baud alignment, reset, and emulation mode.

**asynchronous transmit shift register (AXSR):** An 8-bit register in the asynchronous serial port that receives data from the ADTR and transfers it one bit at a time to the TX pin. See also *ADTR*.

**autoinitialization:** The process of initializing global C variables (contained in the .cinit section) before beginning program execution.

**auxiliary-register arithmetic unit (ARAU):** An arithmetic logic unit (ALU) used to calculate indirect addresses using the auxiliary registers as inputs and outputs.

**auxiliary register (AR):** Eight 16-bit memory-mapped registers (AR0–AR7) that are used for indirect data address pointers, temporary storage, or integer arithmetic processing through the auxiliary register arithmetic unit (ARAU). Each AR is selected by the auxiliary register pointer (ARP).

**auxiliary register pointer (ARP):** A field in the status register used as a pointer to the currently selected auxiliary register.

**auxiliary register pointer buffer (ARB):** A field in the status register that holds the previous value of the auxiliary register pointer (ARP).

**auxiliary registers:** Registers that are used as pointers to an address within the data-space address range. The registers are operated on by the auxiliary register arithmetic unit (ARAU) and are selected by the auxiliary register pointer (ARP).

**AXSR:** *Asynchronous transmit shift register.* A register in the asynchronous serial port that receives data from the ADTR and transfers it one bit at a time to the TX pin. See also *ADTR*.

## B

**benchmark:** A test of performance of a computer or peripheral device.

**bit-reversed addressing:** Addressing in which several bits of an address are reversed in order to speed processing of algorithms, such as Fourier transforms.

**bit-reversed index addressing:** A method of indirect addressing that allows efficient I/O operations by resequencing the data points in a radix-2 FFT program. The direction of carry propagation in the ARAU is reversed.

**boot:** The process of loading a program into program memory.

**boot loader:** A built-in segment of code that transfers code from an external source to memory at power up.

**BOOT port:** A port that enables the boot loader. When BOOT is held low, the processor executes the boot loader program after a hardware reset. When BOOT is held high, the processor skips execution of the boot loader.

**breakpoint:** A point within a program where execution halts because of a previous request.

**BRI:** Basic rate service of ISDN, providing two B channels and one 16-Kbps D channel.

**BSP:** See *buffered serial port (BSP)*.

**buffered serial port (BSP):** An on-chip module that consists of a full-duplex, double-buffered serial port interface and an autobuffering unit (ABU).

**burst mode:** A synchronous serial port mode in which a single word is transmitted following a frame synchronization pulse (FSX and FSR).

**byte:** A sequence of eight adjacent bits operated upon as a unit.

## C

**C:** A high-level, general-purpose programming language useful for writing compilers and operating systems and for programming microprocessors.

**C compiler:** A program that translates C source statements into assembly language source statements.

**CAD:** Computer-aided design.

**CALU:** *Central arithmetic logic unit.*

**CAM:** Computer-aided manufacturing.

**carry bit:** A bit in the status register ST1 used by the ALU for extended arithmetic operations and accumulator shifts and rotates. The carry bit can be tested by conditional instructions.

**central arithmetic logic unit (CALU):** The 32-bit wide, main arithmetic logic unit that performs arithmetic and logic operations.

**central processing unit (CPU):** The module that controls and interprets the machine-language program and its execution.

**circular addressing:** An addressing mode in which an auxiliary register is used to cycle through a range of addresses to create a circular buffer in memory.

**CLK register:** Bit 0 of this register turns the CLKOUT1 signal on or off.

**CLKIN:** *Input clock signal.*



**CLKR:** *Receive clock input pin.* A pin that receives an external clock signal to clock data from the DR pin in to the serial port receive shift register.

**clock modes:** Options used by the clock generator to change the internal CPU clock frequency to a fraction or multiple of the frequency of the input clock signal.

**code:** A set of instructions written to perform a task.

**COFF:** *Common Object File Format.* An implementation of the object file format of the same name developed by AT&T. The TMS320 fixed-point DSP compiler, assembler, and linker use and generate COFF files.

**command file:** A file that contains options, filenames, directives, or commands for the linker or hex conversion utility.

**comment:** A source statement (or portion of a source statement) that is used to document or improve readability of a source file. Comments are not compiled, assembled, or linked; they have no effect on the object file.

**common object file format (COFF):** A binary object file format that promotes modular programming by supporting the concept of *sections*. *See also COFF.*

**configuration control bit (CNF):** A bit in status register ST1 used to determine whether the on-chip RAM block B0 is mapped to program space or data space.

**constant:** A numeric value that can be used as an operand.

**continuous mode:** A synchronous serial port mode in which only one frame synchronization pulse is necessary to transmit several packets at maximum frequency.

**CPU:** *Central processing unit.* The unit that coordinates the functions of a processor.

**CPU cycle:** The time it takes the CPU to go through one logic phase (during which internal values are changed) and one latch phase (during which the values are held constant).

**current auxiliary register:** The auxiliary register pointed to by the auxiliary register pointer (ARP).

## D

**D0–D31:** External data-bus pins that transfer data between the processor and external data/program memory or I/O devices. *See also* LD0–LD31.

**DAB:** *See* *direct-address bus (DAB)*.

**DARAM:** *Dual-access RAM*. Memory that can be accessed twice in a single clock cycle.

**data-address generation logic:** Logic circuitry that generates the addresses for data-memory reads and writes. This circuitry can generate one address per machine cycle. *See also* *program-address generation logic*.

**data bus:** A group of connections used to route data.

**data-display windows:** Windows for observing and modifying various types of data. This category includes the MEMORY, CPU, DISP, and WATCH windows.

**data memory:** A memory region used for storing and manipulating data.

**data-page pointer (DP):** A field in the status register that specifies what is currently selected for direct address generation.

**data-read address bus:** A 16-bit bus that provides the address for data read operations and is driven by the 'C2cLP CPU.

**data-write bus:** A 16-bit bus that provides data for a data memory write and is driven by the 'C2xLP CPU.

**data-write address bus:** A 16-bit bus that provides the address for data write operations and is driven by the 'C2xLP CPU.

**decode phase:** The phase of the pipeline in which the instruction is decoded (identified).

**debugger:** A window-oriented software interface that helps to debug 'C2xx programs running on a 'C2xx emulator or simulator.

**DIE:** *See* DMA interrupt-enable register.

**DIM:** *Delta-interrupt mask bit*. Bit 9 of the ASPCR, which enables and disables delta-detect. The delta-detect function allows or prevents interrupts from being generated by changes on the I/O pins.

**direct address bus (DAB):** A 16-bit bus that provides the data address used by the central processing unit (CPU).

**direct memory access (DMA):** A mode where a device other than the host processor contends for, and receives, mastership of the memory bus so that data transfers may take place independent of the host.

**directives:** Special-purpose commands that control the actions and functions of a software tool (as opposed to assembly language instructions, which control the actions of a device).

**disassembly window:** A window that displays the disassembly of memory contents.

**DMA:** See *direct memory access (DMA)*.

**DMA coprocessor:** A peripheral that transfers the contents of memory locations independently of the processor (except for initialization).

**DMA-interrupt enable register (DIE):** A register (in the CPU register file) that controls to which interrupts the DMA coprocessor responds.

**DP:** *Data-page pointer.* A field in the status register that specifies what is currently selected for direct address generation

**DR bit:** *Data ready indicator for the receiver.* A bit that is automatically reset to zero when the receive register is read, or when the device is reset.

**DR pin:** *Serial-data-receive pin.* A pin that receives serial data into the serial port receive shift register.

**DRAB:** *Data-read address bus.* A 16-bit bus that provides data for a data-memory read and is driven by the memories or the logic interface.

**DRAM:** Dynamic random-access memory.

**dual-access RAM (DARAM):** Memory space that can be read from and written to in the same clock cycle.

**DWAB:** *Data-write address bus.* A 16-bit bus that provides the address for data-write operations and is driven by the 'C2xLP CPU.

**DWEB:** *Data-write bus.* A 16-bit bus that provides data for a data-memory write and is driven by the 'C2xLP CPU.

## E

**EMI:** Electromagnetic interference.

**emulator:** A device that is built to work like another.

**emurst:** A utility that reads the emulator.

**EVM:** Evaluation module.

**EVRC:** Enhanced variable-rate coder.

**expression:** A statement that describes data and processing as part of a program. The statement usually includes a constant, a symbol, or a series of constants and symbols separated by arithmetic operators.

**extended-precision floating-point format:** A 40-bit representation of a floating-point number with a 32-bit mantissa and an 8-bit exponent.

**extended-precision register:** A 40-bit register used primarily for extended-precision floating-point calculations. Floating-point operations use bits 39–0 of an extended-precision register. Integer operations, however, use only bits 31–0.

**external interrupt:** A hardware interrupt triggered by a pin.

**external symbol:** A symbol that is used in the current program module but is defined in a different program module.

## F

**fast Fourier transform (FFT):** An efficient method of computing the discrete Fourier transform, which transforms functions between the time domain and frequency domain. The time-to-frequency domain is called the forward transform, and the frequency-to-time domain is called the inverse transformation.

**FFT:** See *fast Fourier transform (FFT)*.

**FIFO buffer:** *First-in, first-out buffer.* A portion of memory in which data is stored and then retrieved in the same order in which it was stored. Thus, the first word stored in this buffer is retrieved first.

**FIR:** Finite impulse response.

**FMV:** Full motion video.

**framing error:** An error that occurs when a data character received by the asynchronous serial port does not have a valid stop bit.

**G**

**general-purpose input/output pins:** Ports that can be used to supply input signals from an external device or output signals to an external device. These pins are not linked to specific uses; rather, they provide input or output signals for a variety of purposes.

**global-data memory space:** One of four memory spaces. The global-data memory space can either share data with other processors within the system or serve as additional data-memory space.

**global-memory allocation register (GREG):** An 8-bit memory-mapped register that specifies the size of the global memory space. At reset, the GREG is cleared.

**GP:** General purpose.

**GREG:** See *global memory allocation register (GREG)*.

**GSM:** Global System for Mobile Communications.

**H**

**hardware interrupt:** An interrupt triggered through physical connections with on-chip peripherals or external devices.

**hex conversion utility:** A program which accepts COFF files and converts them into one of several standard ASCII hexadecimal formats suitable for loading into an EPROM programmer.

**hardware interrupt:** An interrupt triggered through physical connections with on-chip peripherals or external devices.

**high-level language debugging:** The ability of a compiler to retain symbolic and high-level language information (such as type and function definitions) so that a debugging tool can use this information.

**host-port interface (HPI):** An on-chip module consisting of an 8-bit parallel port that interfaces a host processor to the TMS320C57. The HPI has two modes of operation, shared-access mode (SAM) and host-only mode (HOM). Status and control of the HPI is specified in the HPI control register (HPIC). See also *shared-access mode (SAM)* and *host-only mode (HOM)*.

**HPI:** See *host port interface (HPI)*.

# I

**I/O switches:** Hardware switches on the emulator or EVM board that identify the PC I/O memory space used for emulator–debugger or EVM-debugger communications.

**$\overline{\text{IACK}}$ :** *Interrupt acknowledge signal.* An output signal that indicates that an interrupt has been received and that the program counter is fetching the interrupt vector that will force the processor into an interrupt service routine.

**IFR:** See *interrupt flag register (IFR)*.

**IFR:** *Interrupt flag register.* A 16-bit memory-mapped register used to flag pending interrupts. The IFR may be read from for identifying pending interrupts and written to for clearing selected interrupts.

**IIE:** See *internal-interrupt-enable register*.

**IIF:** See *IIOF flag register*.

**IIOF flag register (IIF):** Controls the function (general-purpose I/O or interrupt) of the four external pins ( $\overline{\text{IIOF0}}$  to  $\overline{\text{IIOF3}}$ ). It also contains timer/DMA interrupt flags.

**IMR:** *Interrupt mask register.* A 16-bit memory-mapped register used to mask external and internal interrupts. you can read from or write to the IMR. A 1 written to any IMR bit position enables the corresponding interrupt (when INTM=0).

**index registers:** Two registers (IR0 and IR1) that are used by the ARAU for indexing an address.

**Input clock signal (CLKIN):** A clock source signal supplied to the on-chip clock generator via the CLKIN/X2 pin.

**input data-scaling shifter:** A 16- to 32-bit barrel left shifter that shifts incoming 16-bit data from 0 to 16 positions left relative to the 32-bit output within the fetch cycle with no cycle overhead.

**input/output status register (IOSR):** A register in the asynchronous serial port that provides status information about signals IO0–IO3 and about transfers in progress.

**instruction register (IR):** A 16-bit register that contains the instruction being executed.

**instruction:** The basic unit of programming that causes the execution of one operation; it consists of an opcode and operands along with optional labels and comments.

**internal interrupt:** A hardware interrupt caused by an on-chip peripheral.

**internal interrupt-enable register:** A register (in the CPU register file) that determines whether or not the CPU will respond to interrupts from the communication ports, the timers, and the DMA coprocessor.

**interrupt:** A signal sent to the CPU that (when not masked) forces the CPU into a subroutine called an interrupt service routine. This signal can be triggered by an external device, an on-chip peripheral, or an instruction (INTR, NMI, or TRAP).

**interrupt acknowledge ( $\overline{IACK}$ ):** A signal that indicates that an interrupt has been received, and that the program counter is fetching the interrupt vector location.

**interrupt-flag register (IFR):** A 16-bit memory-mapped register used to flag several hardware and software interrupts. The IFR may be read to identify pending interrupts and written to clear selected interrupts.

**interrupt mask register (IMR):** A 16-bit memory-mapped register used to mask several external and internal interrupts. You can read from the IMR to determine which interrupts are masked/unmasked. A write to any IMR bit enables a corresponding interrupt (when INTM = 0).

**interrupt service routine (ISR):** A module of code that is executed in response to a hardware or software interrupt.

**IR:** *Instruction register.* A 16-bit register that contains the instruction being executed.

**ISA:** *Industry Standard Architecture.* A subset of the EISA standard.

**ISR:** *Interrupt service routine.* A module of code that is executed in response to a hardware or software interrupt.

## J

**JTAG:** *Joint Test Action Group.* A group of 200 members that designed a testability standard sanctioned by IEEE (IEEE Standard 1149.1).

## L

**LA0–LA30:** External address pins for data/program memory or I/O devices. These pins are on the local bus. *See also* A0–A30.

**LD0–LD31:** External data bus pins that transfer data between the processor and external data/program memory or I/O devices. *See also* D0–D31.

**linker:** A software tool that combines object files to form an object module that can be allocated into TMS320C6200 system memory and executed by the device.

**listing file:** An output file, created by the assembler, that lists source statements, their line numbers, and their effects on the SPC.

## M

**MAC:** Multiply and accumulate.

**macro:** A user-defined routine that can be used as an instruction.

**mantissa:** A component of a floating-point number consisting of a fraction and a sign bit. The mantissa represents a normalized fraction whose binary point is shifted by the exponent.

**map file:** An output file, created by the linker, that shows the memory configuration, section composition, and section allocation, as well as symbols and the addresses at which they were defined.

**maskable interrupt:** A hardware interrupt that can be enabled or disabled through software.

**master clock output signal (CLKOUT1):** The output signal of the on-chip clock generator. The CLKOUT1 high pulse signifies the CPU's logic phase (when internal values are changed), while the CLKOUT1 low pulse signifies the CPU's latch phase (when the values are held constant).

**memory map:** A map of target system memory space, which is partitioned into functional blocks.

**memory-mapped register:** One of the on-chip registers mapped to addresses in memory. Some memory-mapped registers are mapped to data memory, and some are mapped to input/output memory.

**MFLOPS:** *Million floating-point operations per second.* A measure of floating-point processor speed that counts of the number of floating-point operations made per second.



**microcomputer mode:** A mode in which the on-chip ROM (boot loader) is enabled. This mode is selected via the  $MP/\overline{MC}$  pin.

**microprocessor mode:** A mode in which the on-chip ROM is disabled. This mode is selected via the  $MP/\overline{MC}$  pin.

**MIPS:** Million instructions-per-second.

**multiplier:** A device that generates the product of two numbers.

## N

**next auxiliary register:** The register that will be pointed to by the auxiliary register pointer (ARP) when an instruction that modifies ARP is finished executing.

**nonmaskable interrupt (NMI):** A hardware interrupt that uses the same logic as the maskable interrupts but cannot be masked.

**NTSC:** National Television Standards Committee.

## O

**object file:** A file that has been assembled or linked and contains machine-language object code.

**off-chip:** A device external to the device.

**on-chip:** An element or module of the device.

**opcode:** *operation code*. In most cases, the first byte of the machine code that describes the type of operation and combination of operands to the central processing unit (CPU).

**operand:** The part of an instruction that designates where the central processing unit (CPU) will fetch or store data. The operand consists of the arguments, or parameters, of an assembly language instruction, assembler directive, or macro directive.

**operands:** The arguments, or parameters, of an assembly language instruction, assembler directive, or macro directive.

**options:** Command parameters that allow you to request additional or specific functions when you invoke a software tool.

**output data-scaling shifter:** 32- to 16- bit barrel left shifter. Shifts the 32-bit accumulator output from 0 to 7 bits left for quantization management, and outputs either the 16-bit high or low half of the shifted 32-bit data to the data write bus.

**output module:** A linked, executable object file that can be downloaded and executed on a target system.

**overflow:** A condition in which the result of an arithmetic operation exceeds the capacity of the register used to hold that result.

**overflow mode:** A condition in which the result of an arithmetic operation exceeds the capacity of the register used to hold that result.

## P

**PAB:** *Program-address bus.* A 16-bit bus that provides the address for program memory reads and writes.

**PAR:** *Program-address register.* A register that holds the address currently being driven on the program address bus for as many cycles as it takes to complete all memory operations scheduled for the current machine cycle.

**parallel logic unit (PLU):** A 16-bit logic unit that executes logic operations from either long immediate operands or the contents of the dynamic bit manipulation register (DBMR) directly upon data locations without affecting the contents of the accumulator (ACC) or product register (PREG).

**PC:** Personal computer or program counter, depending on the context and use in this book: 1) In installation instructions or information relating to hardware and boards, *PC* means *personal computer* (as in IBM PC). 2) In general debugger and program-related information, *PC* means *program counter*, which is the register that identifies the current statement in a program.

**PDM:** *Parallel debug manager.* A program used for creating and controlling multiple debuggers for the purpose of debugging code in a parallel-processing environment.

**peripheral bus:** A bus that is used by the CPU to communicate the DMA coprocessor, communication ports, and timers.

**pipeline:** A method of executing instructions in an assembly-line fashion.

**pipelining:** A design technique for reducing the effective propagation delay per instruction operation by partitioning the operation into a series of four independent stages, each of which performs a portion of the operation.

**PLL:** Phase-locked loop.

**PLU:** See *parallel logic unit (PLU)*.

- pma:** *Program memory address.* A register that provides the address of a multiplier operand that is contained in program memory.
- port address:** The PC I/O memory space that the debugger uses for communicating with the emulator or EVM. The port address is selected via switches on the emulator or EVM board and communicated to the debugger with the `-p` debugger option.
- PRD:** *Timer period register.* A 16-bit memory-mapped register that specifies the period for the on-chip timer. When the timer counter register (TIM) is decremented past zero, the TIM is loaded with the value in the PRD.
- PRDB:** *Program-read data bus.* A 16-bit bus that provides data for program memory reads and is driven by the memories or the logic interface.
- PREG:** *Product register.* A 32-bit register that holds the results of a multiply operation. See also *product register (PREG)*.
- PRESCALER:** *prescaling shifter.* A 0- to 16-bit left barrel shifter used to prescale data coming into the arithmetic logic unit (ALU). This shifter is also used as a 0- to 16-bit right barrel shifter of the accumulator (ACC). The shift count is specified by a constant in the instruction or by the value in temporary register 1 (TREG1).
- product register (PREG):** A 32-bit register that holds the output from the multiplier. The high and low words of the PREG can be accessed individually. See also *multiplier (MULT)*.
- product-scaling shifter:** A 32-bit shifter that performs a 0, 1, or 4-bit left shift, or a 6-bit right shift of the multiplier product. The left-shift options are used to manage the additional sign bits resulting from the 2s-complement multiply. The right-shift option is used to scale down the number to manage the overflow of product accumulation in the CALU.
- product shift mode:** One of four modes (`-0`, `-1`, `-4`, or `61-bit`) used by the product-scaling shifter.
- program address bus:** A 16-bit bus that provides the address for program memory reads and writes.
- program address generation logic:** Logic circuitry that generates the address for program memory reads and writes, and the address for data memory in instructions that require two data operands. This circuitry can generate one address per machine. See also *data address generation logic*.
- program controller:** Logic circuitry that decodes instructions, manages the pipeline, stores status of operations, and decodes conditional operations.

**program counter:** A register that contains the address of the next instruction to be executed.

**program-read data bus (PRDB):** A 16-bit bus that provides data for program memory reads and is driven by the memories or the logic interface.

**P-SCALER:** *Product shifter.* A 0-, 1-, or 4-bit left shifter that removes extra signed bits (gained in the multiply operation) when fixed-point arithmetic is used; or a 6-bit right shifter that scales the products down to avoid overflow in the accumulation process. The shift mode is specified by the product shift mode (PM) bits.

**pulse code modulation (PCM):** A technique for digitizing speech by sampling the sound waves and converting each sample into a binary number.

## R

**READY:** *Data ready input.* A memory control signal indicating that an external device is prepared for a bus transaction to be completed.

**register:** A group of bits used for temporarily holding data or for controlling or specifying the status of a device.

**repeat counter (RPTC):** A 16-bit register that counts the number of times a single instruction is executed.

**repeat counter register:** A register (in the CPU register file) that specifies the number of times minus one that a block of code is to be repeated when a block repeat is performed.

**repeat mode:** A zero-overhead method for repeating the execution of a block of code.

**reset:** A means to bring the central processing unit (CPU) to a known state by setting the registers and control bits to predetermined values and signaling execution to start at a specified address.

**RSR:** *Receive shift register.* One of two registers that perform shift operations in and out of the serial port. The other register is the transmit shift register (XSR).

**run address:** The address where a section runs.

**S**

**SAM:** *Shared-access mode.*

**SARAM:** *Single-access RAM.* Memory that can be read from or written to only in a single clock cycle.

**scalar type:** A C type in which the variable is a single variable, not composed of other variables.

**SDTR:** *Synchronous serial port transmit/receive register.* The SDTR is an I/O-mapped read/write register that sends data to the transmit FIFO buffer, and extracts data from the receive FIFO buffer.

**serial-port-control register (SPC):** A 16-bit memory-mapped register that contains status and control bits for the serial-port interface. The SPC is identical to the time-division multiplexed serial-port control register (TSPC), except that bit 0 is reserved for the TDM bit.

**serial-port interface:** An on-chip full-duplex serial port interface that provides direct serial communication to serial devices with a minimum of external hardware, such as codecs and serial analog-to-digital (A/D) converters. Status and control of the serial port is specified in the serial port control register (SPC).

**simulator:** A development tool that simulates the operation of the device for executing and debugging applications programs by using the device debugger.

**single-access RAM (SARAM):** Memory space that only can be read from or written to in a single clock cycle.

**single-precision floating-point format:** A 32-bit representation of a floating-point number with a 24-bit mantissa and an 8-bit exponent.

**single-step:** A form of program execution that allows you to see the effects of each statement. The program is executed statement by statement; the debugger pauses after each statement to update the data-display windows.

**software interrupt:** An interrupt caused by the execution of an INTR, NMI, or TRAP instruction.

**source file:** A file that contains C code or assembly language code that will be compiled or assembled to form an object file.

**ST:** See status register.

**ST0/ST1:** Two 16-bit registers that contain status and control bits.

**stack:** A block of memory used for storing return addresses for subroutines and interrupt service routines or for storing data. The 'C2xLP stack is 16 bits wide and eight levels deep.

**status register:** A register in the CPU register file that contains global information related to the CPU.

**string table:** A table that stores symbol names that are longer than eight characters (symbol names of eight characters or longer cannot be stored in the symbol table; instead, they are stored in the string table). The name portion of the symbol's entry points to the location of the string in the string table.

**symbol:** A string of alphanumeric characters that represents an address or a value.

**symbolic debugging:** The ability of a software tool to retain symbolic information so that it can be used by a debugging tool such as a simulator or an emulator.

**symbol table:** A portion of a COFF object file that contains information about the symbols that are defined and used by the file.

**synchronous serial port control register (SSPCR):** The 16-bit memory-mapped SSPCR controls the operation of the synchronous serial port.

**synchronous serial port transmit/receive register (SDTR):** *Transmit interrupt bit.* This maskable bit (bit 4) of the interrupt mask register is tied to a transmit interrupt for the synchronous serial port.

**synchronous serial port receive interrupt:** *Receive-interrupt pin.* Bit 3 of the interrupt mask register is tied to the receive interrupt for the synchronous serial port.

## T

**T320C2xLP:** *Texas Instruments cDSP core.*

**TCR:** *Timer control register.* A 16-bit register that controls the operation of the on-chip timer.

**TEC:** *Texas Instruments embedded gate array.* A gate array embedded with a hardware macro.

**TGC:** *Texas Instruments gate array.*

**temporary register (TREG):** A 16-bit register that holds a temporary data value. See also *TREG0*, *TREG1*, and *TREG2*.

**time-division multiplexing (TDM):** The process by which a single serial bus is shared by devices with each device taking turns to communicate on the bus.

**timer:** A programmable peripheral that can generate pulses or time events.

**timer-control register (TCR):** A 16-bit register that controls the operation of the on-chip timer.

**timer-period register:** A 32-bit memory-mapped register that specifies the period for the on-chip timer.

**transmit shift register (XSR):** One of two registers that perform shift operations in and out of the serial port. The other register is the receive shift register (RSR).

**TREG:** *Temporary register.* A register that holds a temporary data value.

**TREG0:** *temporary register 0.* A 16-bit memory-mapped register that holds an operand for the multiplier. See also *multiplier (MULT)*.

**TREG1:** *temporary register 1.* A 5-bit memory-mapped register that holds a dynamic prescaling shift count for data inputs to the arithmetic logic unit (ALU). See also *PRESCALER*.

**TREG2:** *temporary register 2.* A 4-bit memory-mapped register that holds a dynamic bit pointer for the BITT instruction.

## U

**UART:** *Universal asynchronous receiver/transmitter.* Used as another name for the asynchronous serial port.

**URST:** *Reset asynchronous serial port bit.* Bit 13 of the ASPCR resets the asynchronous port.

## V

**VGA:** *Video Graphics Array.* An industry standard for video cards.

## W

**wait state:** A period of time that the CPU must wait for external program, data, or I/O memory to respond when reading from or writing to that external memory. The CPU waits one extra cycle for every wait state.

**wait-state generator:** A program that can be modified to generate a limited number of wait states for a given off-chip memory space (lower program, upper program, data, or I/O).

**wait-state generator-control register (WSGR):** This register, which is mapped to I/O memory, controls the wait-state generator.

**WATCH window:** A window that displays the values of selected expressions, symbols, addresses, and registers.

**WD:** Watchdog.

**word:** A 16-bit addressable location in target memory.

**word:** A word, as defined in this document, consists of a sequence of 16 adjacent bits (two bytes).

**WSGR:** *Wait-state generator-control register.* This register, which is mapped to I/O memory, control the wait-state generator.

**WWW:** World Wide Web

## X

**XDS:** Extended development system



# Acronyms and Abbreviations

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## A

**ACC:** accumulator  
**A/D:** analog-to-digital  
**ADC:** analog-to-digital converter  
**ADPCM:** adaptive differential pulse code modulation  
**ADTR:** asynchronous data transmit and receive register  
**AIB:** analog interface board  
**AIC:** analog interface circuit  
**ALU:** arithmetic logic unit  
**APLL:** ASIC PLL  
**AR:** auxiliary register  
**ARAM:** audio random-access memory  
**ARAU:** auxiliary register arithmetic unit  
**ARB:** auxiliary register pointer buffer  
**ARP:** auxiliary register pointer  
**ARSR:** asynchronous receive shift register  
**ASCII:** American standard code for information interchange  
**ASIC:** application-specific integrated circuit  
**ASPCR:** asynchronous serial port control register  
**ATM:** asynchronous transfer mode  
**AXSR:** asynchronous transmit shift register

## B

**BGA:** ball grid array  
**BOPS:** billion operations per second  
**BRI:** basic rate service (of ISON)  
**BSP:** buffered serial port  
**BSR:** bank-select register  
**BTT:** breakpoint, trace, and time-stamping

## C

**CAD:** computer-aided design  
**CALU:** central arithmetic logic unit  
**CAM:** computer-aided manufacturing  
**CBCR:** circular buffer control register  
**CD:** computer disk  
**cDSP:** customizable digital signal processor  
**CELP:** code excited linear prediction  
**codec:** coders and decoders  
**COFF:** common object file format  
**CPGA:** ceramic pin grid array  
**CPU:** central processing unit  
**CQFP:** ceramic quad flat pack  
**CRC:** cyclic redundancy check  
**CSSU:** compare, select, store unit (Viterbi operator)

**D**

**D/A:** digital-to-analog  
**DAB:** direct-address bus  
**DAC:** digital-to-analog converter  
**DASP:** Dallas Application-Specific Products  
**DMOV:** data move  
**DARAM:** dual-access RAM  
**DBMR:** dynamic bit-manipulation register  
**DIE:** DMA interrupt-enable register  
**DIM:** delta-interrupt mask bit  
**DIP:** dual in-line package  
**DMA:** direct memory access  
**DP:** data-page pointer  
**DRAB:** data-read address bus  
**DRAM:** dynamic random-access memory  
**DSI:** digital speech interpolation  
**DSK:** DSP starter kit  
**DSP:** digital signal processor  
**DTAD:** digital tapeless answering device  
**DTMF:** dual-tone multi-frequency ("touch tones")  
**DWAB:** data-write-address bus  
**DWEB:** data-write bus

**E**

**EEPROM:** electrically-erasable programmable read-only memory  
**EMI:** electromagnetic interference  
**EPK:** emulator porting kit  
**EPROM:** erasable programmable read-only memory  
**EV:** event manager  
**EVM:** evaluation module  
**EVRC:** enhanced variable-rate coder

## F

**FIFO:** first-in, first-out  
**FIR:** finite impulse response  
**FMV:** full-motion video  
**FFT:** fast Fourier transform

## G

**GEL:** GO DSP Corporation's extension language  
**GP:** general purpose  
**GPT CON:** general-purpose timer control register  
**GREG:** global memory allocation register  
**GSM:** global system for mobile communications

## H

**HDD:** hard disk drive  
**HLL:** high-level language  
**HOM:** host-only mode  
**HPI:** host-port interface

## I

**ICM:** incoming message  
**IDE:** integrated development environment  
**IFR:** interrupt-flag register  
**I/O:** input/output  
**IIE:** internal interrupt enable  
**IIR:** infinite impulse response  
**IMR:** interrupt-mark register

**IR:** instruction register  
**ISA:** industry-standard architecture  
**ISDN:** Integrated Services Digital Network  
**ISO:** International Standards Organization  
**ISR:** interrupt service routine

**J**

**JLCC:** J-leaded chip carrier  
**JPEG:** Joint Photographic Experts Group  
**JTAG:** Joint Test Action Group (IEEE Standard 1149.1)

**L**

**LAN:** local area network  
**LCCC:** leadless ceramic chip carrier

**M**

**MAC:** multiply and accumulate  
**MACD:** multiply, accumulate, and data move  
**MCU:** microcontroller unit  
**MFLOPS:** million floating-point operations per second  
**MIPS:** million instructions per second  
**MP:** master processor  
**MPEG:** Moving Picture Expert Group  
**MPY:** multiply  
**MUX:** multiplexor  
**MVP:** multimedia video processor

**N**

**NCRF:** New Code Release Form  
**NRZ:** Non-return to zero  
**NTSC:** National Television Standards Committee

**O**

**OCR:** optical character recognition

**OGM:** out-going message

**OTP:** one-time programmable

**P**

**PAB:** program-address bus

**PAL:** phase alternate line

**PAR:** program-address register

**PCB:** printed circuit board

**PC:** personal computer

**PCI:** peripheral component interconnect

**PCM:** pulse code modulation

**PCMCIA:** Personal Computer Memory Card International Association

**PCS:** personal communications system

**PDA:** personal digital assistant

**PDC:** personal digital cellular

**PDM:** parallel debug manager

**PGA:** pin grid array

**PIC:** Product Information Center

**PLCC:** plastic J-leaded chip carrier

**PLL:** phase-locked loop

**PLU:** parallel logic unit

**PM:** processor module

**PMA:** program memory address

**PMST:** processor mode status register

**PP:** parallel processor  
**PPDS:** parallel processing development system  
**PQFP:** plastic quad flat pack  
**PRD:** time period register  
**PREG:** product register  
**PROB:** program-read data bus  
**PROM:** programmable read-only memory  
**PSTN:** Public Switched Telephone Network  
**PWM:** pulse-width modulation

## R

**RAM:** random-access memory  
**ROM:** read only memory  
**RPTC:** repeat counter  
**RSR:** receive shift register  
**RTI:** real-time interrupt

## S

**S/N:** signal-to-noise  
**SAM:** shared access mode  
**SARAM:** single-access RAM  
**SCI:** serial communications interface; serial control interface  
**SCSI:** small computer system interface  
**SDB:** software development board  
**SDRAM:** synchronous dynamic random-access memory  
**SDTR:** synchronous serial-port transmit/receive register  
**SNR:** signal-to-noise ratio

**SOIC:** small outline IC

**SPC:** section program counter; serial port control register

**SPCE:** serial port control extension register

**SPI:** serial-port interface

**SRAM:** static random-access memory

**SRT:** shift register transfer

**SSPCE:** synchronous serial-port control register

**ST:** status register

**T**

**TBC:** test bus controller

**TC:** transfer controller

**TCR:** timer-control register

**TDM:** time division multiplex

**TEC:** Texas Instruments embedded gate array

**TI:** Texas Instruments

**TI & ME:** DSP solutions web site individual page (i.e., Texas Instruments & Me)

**TQFP:** thin quad flat pack

**TR:** temporary register

**TSPC:** time-division-multiplexed serial-port control register

**TTL:** transistor-to-transistor logic

**TTO:** Technical Training Organization

**U**

**UART:** universal asynchronous receiver/transmitter

**URST:** reset asynchronous serial-port bit



**V**

**VC:** video controller

**VLSI:** very-large-scale integration

**VRAM:** video read-access memory

**W**

**WD:** watchdog

**WDCR:** watchdog control register

**WWW:** World Wide Web

**X**

**XDS:** extended development system

**XSR:** transmit shift register

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